19-4802; Rev 0; 7/00

MAXIM

Single/Dual LVDS Line Receivers with Ultra-Low Pulse Skew in SOT23

General Description

The MAX9111/MAX9113 single/dual low-voltage differential signaling (LVDS) receivers are designed for high-speed applications requiring minimum power consumption, space, and noise. Both devices support switching rates exceeding 500Mbps while operating from a single +3.3V supply, and feature ultra-low 300ps (max) pulse skew required for high-resolution imaging applications such as laser printers and digital copiers.

The MAX9111 is a single LVDS receiver, and the MAX9113 is a dual LVDS receiver.

Both devices conform to the EIA/TIA-644 LVDS standard and convert LVDS to LVTTL/CMOS-compatible outputs. A fail-safe feature sets the outputs high when the inputs are undriven and open, terminated, or shorted. The MAX9111/MAX9113 are available in space-saving 8-pin SOT23 and SO packages. Refer to the MAX9110/MAX9112 data sheet for single/dual LVDS line drivers.

Applications

Laser Printers

Digital Copiers

Cellular Phone Base Stations

Telecom Switching Equipment

Network Switches/Routers

LCD Displays

Backplane Interconnect

Clock Distribution

Features

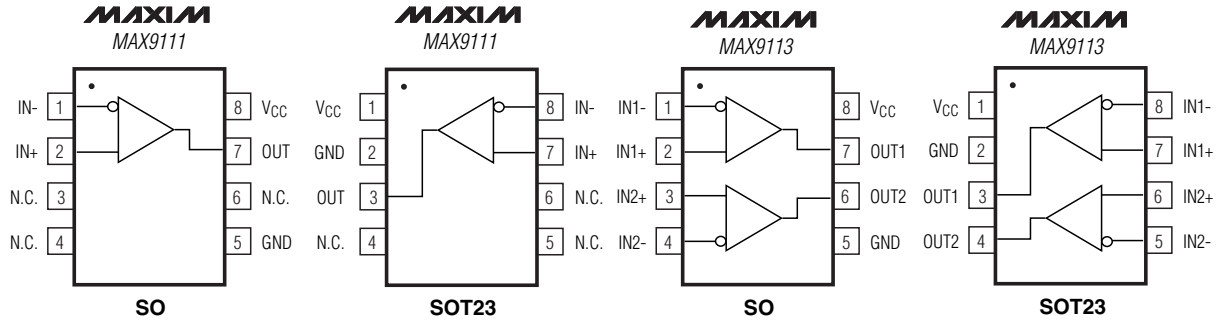
- **Low 300ps (max) Pulse Skew for High-Resolution Imaging and High-Speed Interconnect**
- **Space-Saving 8-Pin SOT23 and SO Packages**
- **Pin-Compatible Upgrades to DS90LV018A and DS90LV028A (SO Packages Only)**
- **Guaranteed 500Mbps Data Rate**
- **Low 29mW Power Dissipation at 3.3V**
- **Conform to EIA/TIA-644 Standard**
- **Single +3.3V Supply**
- **Flow-Through Pinout Simplifies PC Board Layout**
- **Fail-Safe Circuit Sets Output High for Undriven Inputs**
- **High-Impedance LVDS Inputs when Powered Off**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX9111EKA	-40°C to +85°C	8 SOT23	AAEE
MAX9111ESA	-40°C to +85°C	8 SO	—
MAX9113EKA	-40°C to +85°C	8 SOT23	AAED
MAX9113ESA	-40°C to +85°C	8 SO	—

Typical Operating Circuit appears at end of data sheet.

Pin Configurations/Functional Diagrams/Truth Table



(IN_+) - (IN_-)	OUT_
≥ 100mV	H
≤ -100mV	L
OPEN	H
SHORT	H
100Ω PARALLEL TERMINATION (UNDRIVEN)	H

H = LOGIC LEVEL HIGH
L = LOGIC LEVEL LOW

Single/Dual LVDS Line Receivers with Ultra-Low Pulse Skew in SOT23

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4V
IN_ _ to GND .....-0.3V to +3.9V
OUT_ _ to GND.....-0.3V to (V_{CC} + 0.3V)
ESD Protection All Pins
(Human Body Model, IN_+, IN_-) .....±11kV
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 7.52mW/°C above +70°C).....602mW
8-Pin SO (derate 5.88mW°C above +70°C).....471mW
Operating Temperature Ranges
MAX911_E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, magnitude of input voltage, $|V_{ID}|$ = +0.1V to +1.0V, V_{CM} = $|V_{ID}|/2$ to (2.4V - ($|V_{ID}|/2$)), T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Input High Threshold (Note 3)	V_{TH}	V_{CM} = 0.05V, 1.2V, 2.75V at 3.3V				100	mV
Differential Input Low Threshold (Note 3)	V_{TL}	V_{CM} = 0.05V, 1.2V, 2.75V at 3.3V		-100			mV
Differential Input Resistance	R_{DIFF}	V_{CM} = 0.2V or 2.2V, V_{ID} = ±0.4V, V_{CC} = 0 or 3.6V		5	18		kΩ
Output High Voltage (OUT_)	V_{OH}	I_{OH} = -4mA	V_{ID} = +200mV	2.7			V
			Inputs shorted, undriven	2.7			
			100Ω parallel termination, undriven	2.7			
Output Low Voltage (OUT_)	V_{OL}	I_{OL} = 4mA, V_{ID} = -200mV				0.4	
Output Short-Circuit Current	I_{OS}	V_{ID} = +200mV, $V_{OUT\_}$ = 0				-100	mA
No-Load Supply Current	I_{CC}	Inputs open	MAX9111		4.2	6	mA
			MAX9113		8.7	11	

SWITCHING CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Notes 4, 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}	C_L = 15pF, V_{ID} = ±200mV, V_{CM} = 1.2V, Figures 1, 2	1	1.77	2.5	ns
Differential Propagation Delay Low to High	t_{PLHD}		1	1.68	2.5	ns
Differential Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (Note 7)	t_{SKD1}			90	300	ps
Differential Channel-to-Channel Skew; Same Device (MAX9113 only) (Note 8)	t_{SKD2}			140	400	ps
Differential Part-to-Part Skew (Note 9)	t_{SKD3}				1	ns
Differential Part-to-Part Skew (MAX9113 only) (Note 10)	t_{SKD4}				1.5	ns
Rise Time	t_{TLH}			0.6	0.8	ns
Fall Time	t_{THL}			0.6	0.8	ns
Maximum Operating Frequency	f_{MAX}	All channels switching, C_L =15pF, V_{OL} (max) = 0.4V, V_{OH} (min) = 2.7V, 40% < duty cycle < 60% (Note 6)	250	300		MHz

Note 1: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 2: Current into the device is defined as positive. Current out of the devices is defined as negative. All voltages are referenced to ground except V_{TH} and V_{TL}.

Note 3: Guaranteed by design, not production tested.

Note 4: AC parameters are guaranteed by design and characterization.

Note 5: C_L includes probe and test jig capacitance.

Note 6: f_{MAX} generator output conditions: $t_R = t_F$ < 1ns (0% to 100%), 50% duty cycle, V_{OH} = 1.3V, V_{OL} = 1.1V.

Note 7: t_{SKD1} is the magnitude difference of differential propagation delays in a channel. $t_{SKD1} = \lvert t_{PLHD} - t_{PHLD} \rvert$.

Note 8: t_{SKD2} is the magnitude difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of the other channel on the same device.

Note 9: t_{SKD3} is the magnitude difference of any differential propagation delays between devices at the same V_{CC} and within 5°C of each other.

Note 10: t_{SKD4}, is the magnitude difference of any differential propagation delays between devices operating over the rated supply and temperature ranges.

Single/Dual LVDS Line Receivers with Ultra-Low Pulse Skew in SOT23

Test Circuit Diagrams

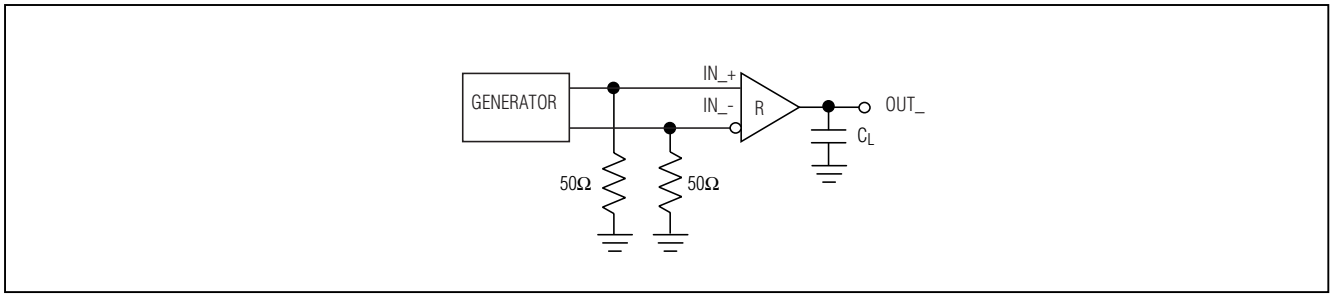


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

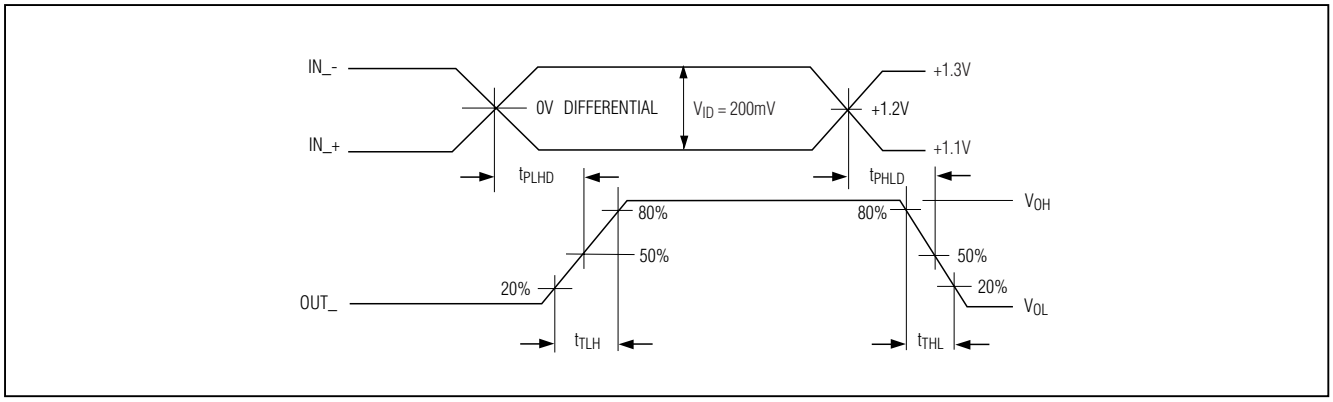
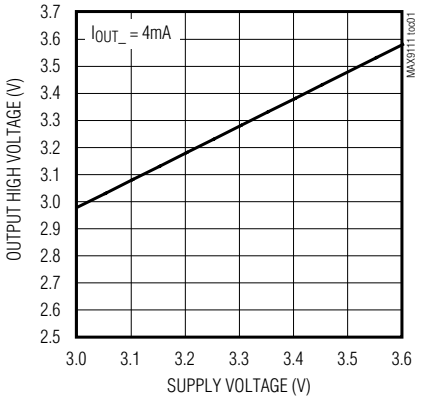


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

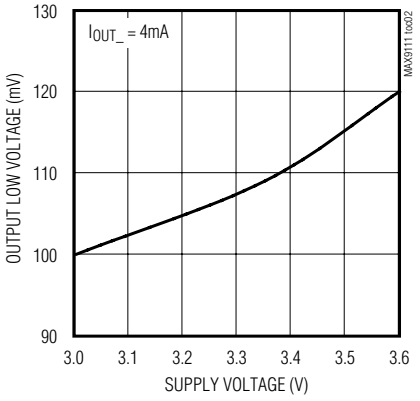
Typical Operating Characteristics

(V_{CC} = 3.3V, $|V_{ID}|$ = 200mV, V_{CM} = 1.2V, f_{IN} = 200MHz, C_L = 15pF, T_A = +25°C and over recommended operating conditions unless otherwise specified.)

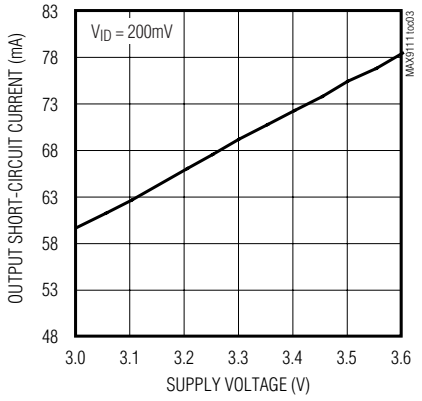
OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



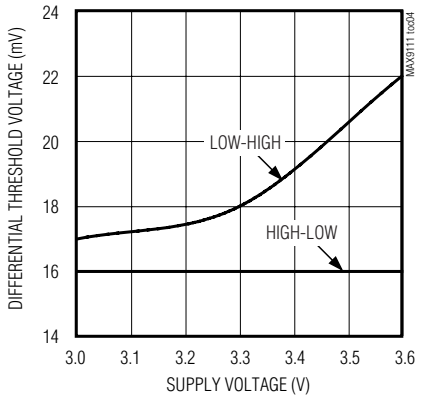
OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



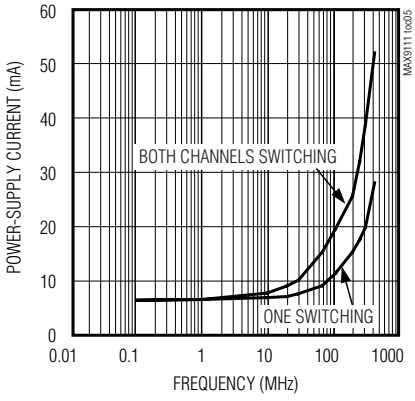
OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE



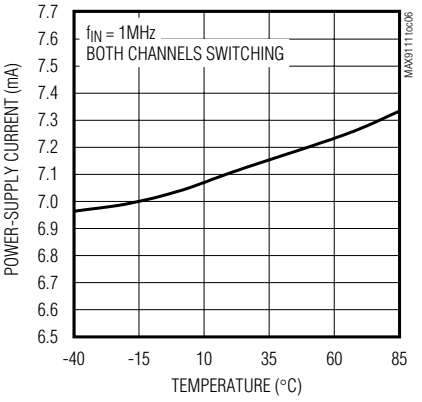
DIFFERENTIAL THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



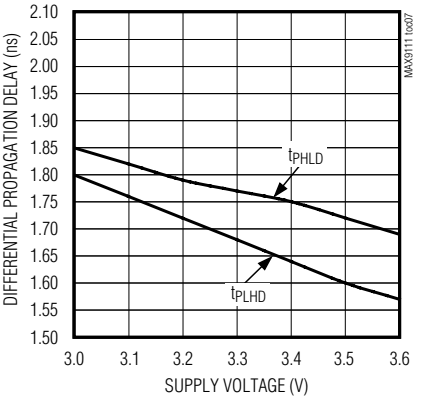
MAX9113 POWER-SUPPLY CURRENT vs. FREQUENCY



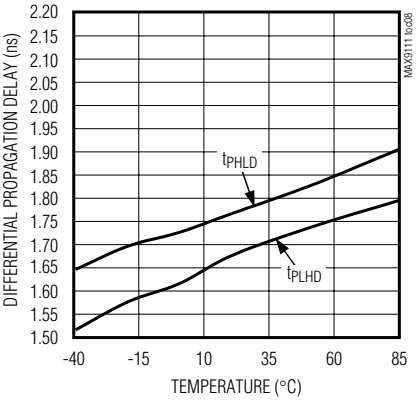
POWER-SUPPLY CURRENT vs. TEMPERATURE



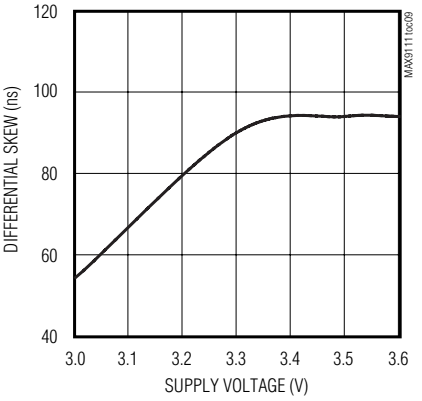
DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



DIFFERENTIAL PULSE SKEW vs. SUPPLY VOLTAGE

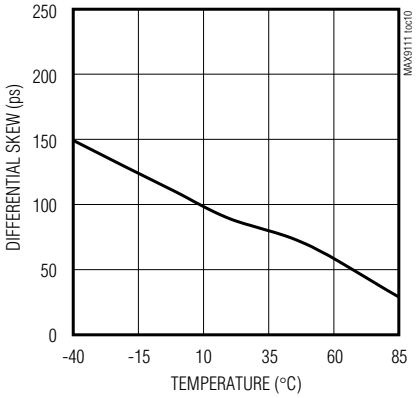


Single/Dual LVDS Line Receivers with Ultra-Low Pulse Skew in SOT23

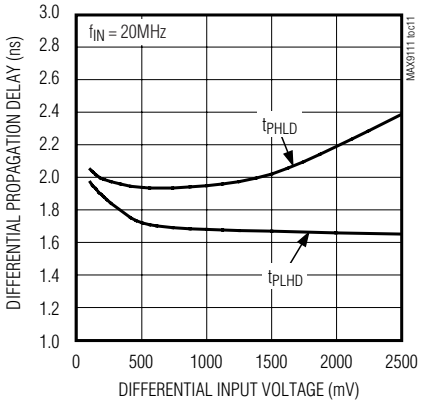
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, $|V_{ID}|$ = 200mV, V_{CM} = 1.2V, f_{IN} = 200MHz, C_L = 15pF, T_A = +25°C and over recommended operating conditions, unless otherwise specified.)

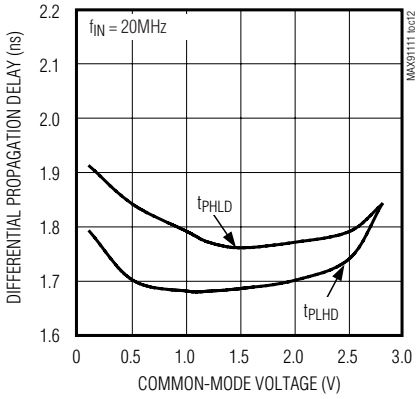
DIFFERENTIAL PULSE SKEW vs. TEMPERATURE



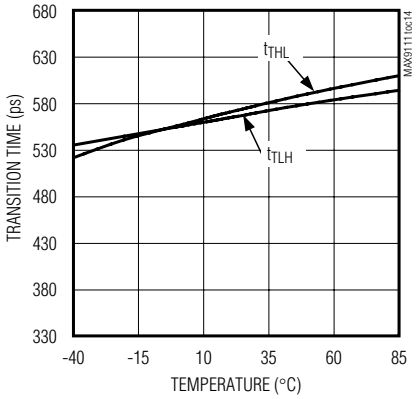
DIFFERENTIAL PROPAGATION DELAY vs. DIFFERENTIAL INPUT VOLTAGE



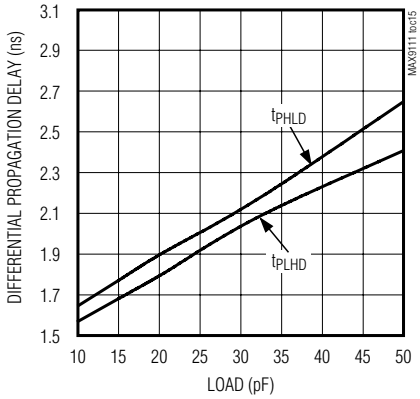
DIFFERENTIAL PROPAGATION DELAY vs. COMMON-MODE VOLTAGE



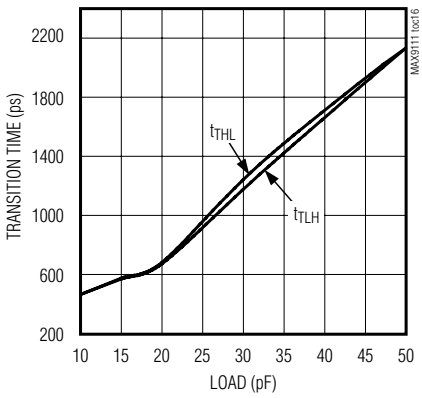
TRANSITION TIME vs. TEMPERATURE



DIFFERENTIAL PROPAGATION DELAY vs. LOAD



TRANSITION TIME vs. LOAD



Pin Description

PIN				NAME	FUNCTION
MAX9111		MAX9113			
SOT23-8	SO-8	SOT23-8	SO-8		
1	8	1	8	V_{CC}	Power Supply
2	5	2	5	GND	Ground
8	1	8	1	IN-/IN1-	Receiver Inverting Differential Input
7	2	7	2	IN+/IN1+	Receiver Noninverting Differential Input
—	—	5	4	IN2-	Receiver Inverting Differential Input
—	—	6	3	IN2+	Receiver Noninverting Differential Input
3	7	3	7	OUT/OUT1	Receiver Output
—	—	4	6	OUT2	Receiver Output
4, 5, 6	3, 4, 6	—	—	N.C.	No Connection. Not internally connected.

Detailed Description

LVDS Inputs

The MAX9111/MAX9113 feature LVDS inputs for interfacing high-speed digital circuitry. The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled impedance media, as defined by the ANSI/EIA/TIA-644 standards. The technology uses low-voltage signals to achieve fast transition times, minimize power dissipation, and noise immunity. Receivers such as the MAX9111/MAX9113 convert LVDS signals to CMOS/LVTTL signals at rates in excess of 500Mbps. The devices are capable of detecting differential signals as low as 100mV and as high as 1V within a 0V to 2.4V input voltage range . The LVDS standard specifies an input voltage range of 0 to 2.4V referenced to ground.

Fail-Safe

The fail-safe feature sets the output to a high state when the inputs are undriven and open, terminated, or shorted. When using one channel in the MAX9113, leave the unused channel open.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The receiver inputs of the MAX9111/MAX9113 have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±11kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down.

ESD protection can be tested in various ways; the receiver inputs of this product family are characterized for protection to the limit of ±11kV using the Human Body Model.

Human Body Model

Figure 3a shows the Human Body Model, and Figure 3b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

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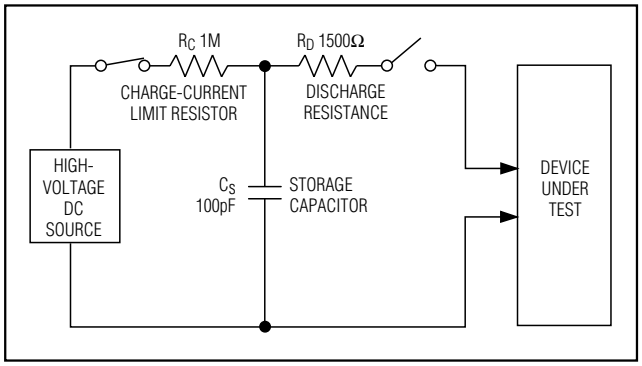


Figure 3a. Human Body ESD Test Modules

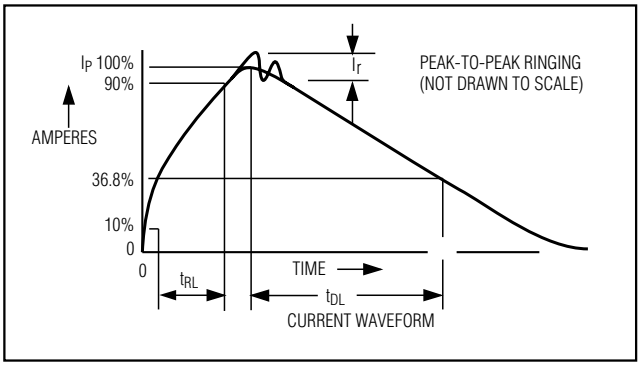


Figure 3b. Human Body Current Waveform

Applications Information

Supply Bypassing

Bypass V_{CC} with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel, as close to the device as possible, with the 0.001µF valued capacitor the closest to the device. For additional supply bypassing, place a 10µF tantalum or ceramic capacitor at the point where power enters the circuit board.

Differential Traces

Output trace characteristics affect the performance of the MAX9111/MAX9113. Use controlled impedance traces to match trace impedance to both transmission medium impedance and the termination resistor. Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have a differential characteristic impedance of about 100Ω. Use cables and connectors that have matched impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

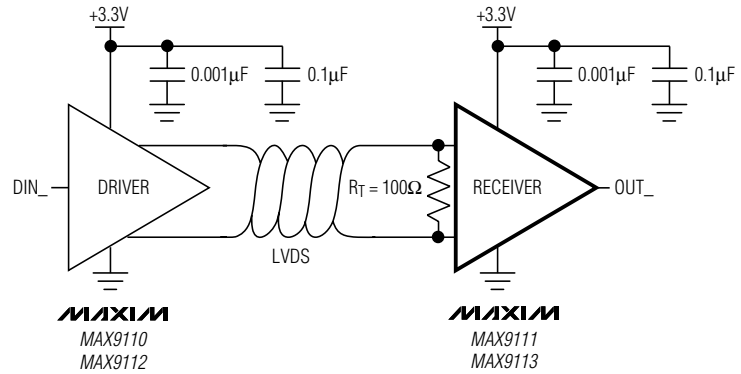
Termination resistors should match the differential characteristic impedance of the transmission line. Because the MAX9111/MAX9113 are current steering devices, an output voltage will not be generated without a termination resistor. Output voltage levels depend upon the value of the termination resistor. Resistance values may range from 75Ω to 150Ω.

Minimize the distance between the termination resistor and receiver inputs. Use a single 1% to 2% surface-mount resistor across the receiver inputs.

Board Layout

For LVDS applications, a four-layer PC board that provides separate power, ground, LVDS signals, and input signals is recommended. Isolate the input and LVDS signals from each other to prevent coupling. For best results, separate the input and LVDS signal planes with the power and ground planes.

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT:

MAX9111: 675

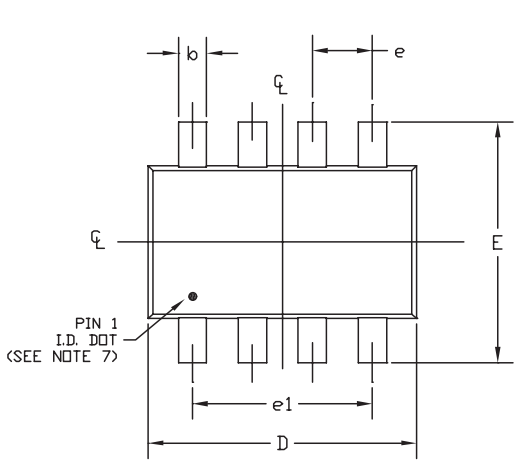
MAX9113: 675

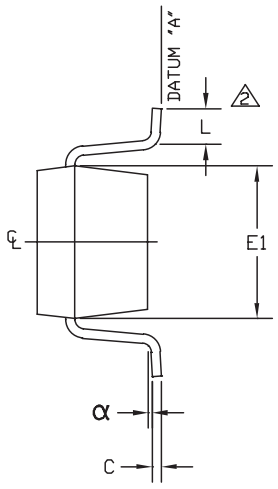
PROCESS: CMOS

Single/Dual LVDS Line Receivers with Ultra-Low Pulse Skew in SOT23

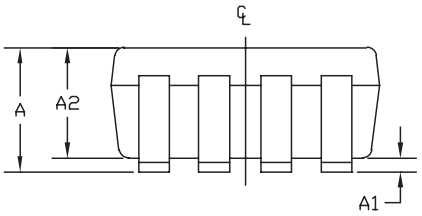
Package Information

SOT23, 8L.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.

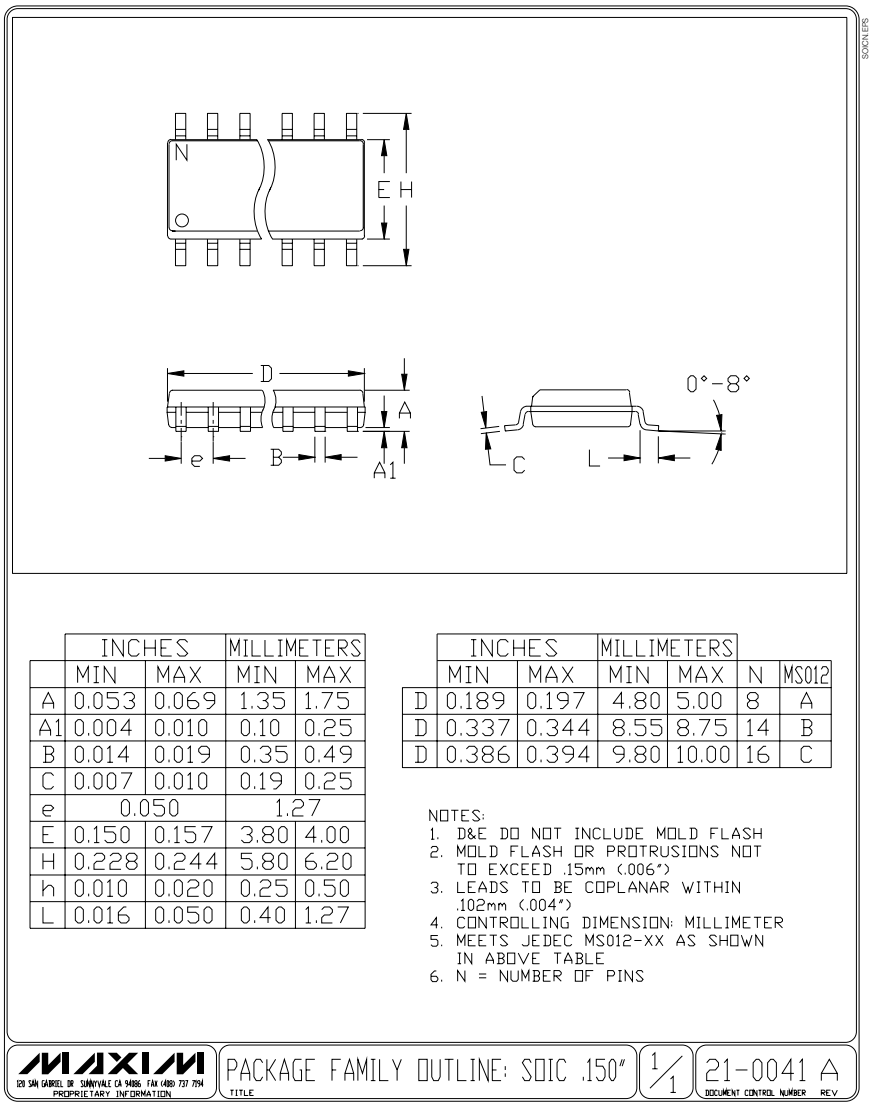
MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SOT 23, 8L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	B	1/1

Single/Dual LVDS Line Receivers with Ultra-Low Pulse Skew in SOT23

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" TITLE

1/1

21-0041 A DOCUMENT CONTROL NUMBER REV

NOTES