19-3784; Rev 0; 8/05

EVALUATION KIT AVAILABLE

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

MAX8751

General Description

The MAX8751 cold-cathode-fluorescent lamp (CCFL) inverter controller is designed to drive multiple CCFLs using the fixed-frequency, full-bridge inverter topology. The MAX8751 operates in resonant mode during striking and switches over to constant-frequency operation after all the lamps are lit. This unique feature ensures reliable striking under all conditions and reduces the transformer stress.

The MAX8751 can drive large power MOSFETs typically used in applications where one power stage drives four or more CCFL lamps in parallel. An internal 5.35V linear regulator powers the MOSFET drivers and most of the internal circuitry. The controller operates over a wide input-voltage range (6V to 28V) with high power to light efficiency. The device also includes safety features that effectively protect against many single-point fault conditions, including lamp-out and short-circuit conditions.

The MAX8751 achieves a 10:1 dimming range by "chopping" the lamp current on and off using the digital pulse-width modulation (DPWM) method. The DPWM frequency can be accurately adjusted with a resistor or synchronized to an external signal. The brightness is controlled by an analog voltage on the CNTL pin.

The MAX8751 is capable of synchronizing and adjusting the phase of the gate drivers and DPWM oscillator. These features allow multiple MAX8751 ICs to be connected in a daisy-chain configuration. The switching frequency and DPWM frequency can be easily adjusted using external resistors, or synchronized with system signals. If the controller loses the external sync signals, it switches over to the internal oscillators and keeps operating. Phase-shift select pins PS1 and PS2 can be used to program up to four different phase shifts, allowing up to five MAX8751s to be used together.

The MAX8751 is available in a low-profile, 32-pin TQFN package and operates over the -40°C to +85°C temperature range.

Applications

LCD TVs
LCD Monitors
Notebook Computers
Automotive Infotainment

Ordering Information

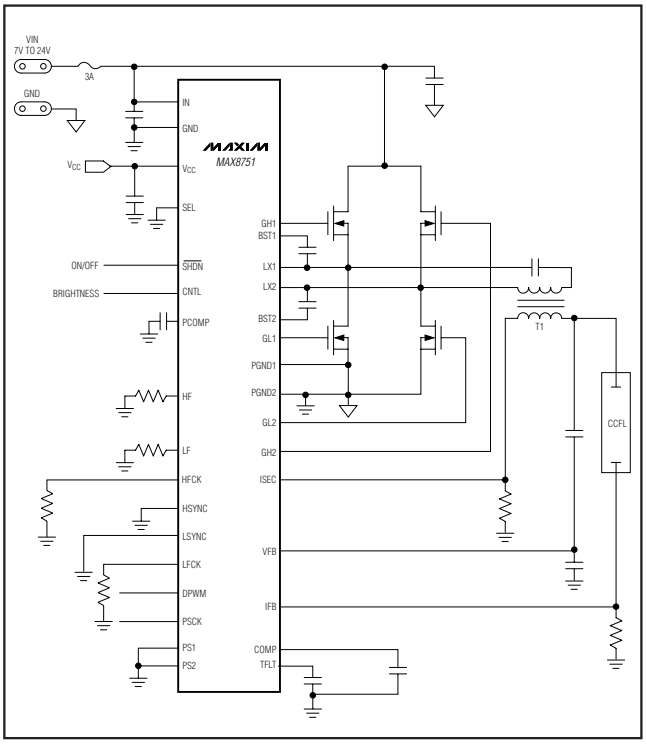
PART	TEMP RANGE	PIN-PACKAGE
MAX8751ETJ	-40°C to +85°C	32 TQFN

Pin Configuration appears at end of data sheet.

Features

- **All n-Type MOSFET Low-Cost, Full-Bridge, Fixed-Frequency Inverter Topology for Highest Efficiency**
- **Resonant-Mode Striking Ensures Startup**
- **Strong Gate Drivers Can Easily Drive Large External MOSFETs for Multilamp Applications**
- **Adjustable DPWM Frequency with Sync and Phase-Shift Capability**
- **10:1 Dimming Range with Accurate Analog Interface**
- **Lamp-Out Detection with Adjustable Timeout**
- **Secondary Current Limit with Adjustable Timeout**
- **Adjustable Secondary Voltage Limiting**
- **Adjustable DPWM Rise and Fall Time**
- **Wide Input Voltage Range (6V to 28V)**
- **32-Pin TQFN Package**

Minimal Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

ABSOLUTE MAXIMUM RATINGS

IN, LX1, LX2 to GND .....-0.3V to +30V
BST1, BST2 to GND .....-0.3V to +36V
BST2 to LX2 .....-0.3V to +6V
V_{CC} to GND .....-0.3V to +6V
GH1 to LX1 .....-0.3V to V_{BST1} + 0.3V
GH2 to LX2 .....-0.3V to V_{BST2} + 0.3V
CNTL, SEL COMP, GL1, GL2, DPWM, HF, LF, HFCK, HSYNC, LSYNC, LFCK, PCOMP, PS1, PSCK, TFLT, PS2, $\overline{SHDN}$ to GND .....-0.3V to V_{CC} + 0.3V
IFB, ISEC, VFB to GND .....-6V to +6V
PGND1, PGND2 to GND .....-0.3V to +3V
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 21.3mW/°C above +70°C) 1702.1mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 24V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input-Voltage Range		6		28	V
IN Quiescent Current	$V_{\overline{SHDN}}$ = 5.5V, V_{IN} = 28V		3.2	6	mA
IN Quiescent Current, Shutdown	$V_{\overline{SHDN}}$ = 0		6	20	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SHDN}}$ = 5.5V, 6V < V_{IN} < 28V, 0 < I_{LOAD} < 20mA	5.20	5.35	5.50	V
V_{CC} Output Voltage, Shutdown	$V_{\overline{SHDN}}$ = 0, no load	3.5	4.6	5.5	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising (leaving lockout)			4.5	V
	V_{CC} falling (entering lockout)	4.0			
V_{CC} Undervoltage Lockout Hysteresis			200		mV
GH1, GH2, GL1, and GL2 On-Resistance, Low State	I_{TEST} = 10mA; V_{CC} = 5.3V		1	3	Ω
GH1, GH2, GL1, and GL2 On-Resistance, High State	I_{TEST} = 10mA; V_{CC} = 5.3V		4	8	Ω
BST1, BST2 Leakage Current	V_{BST1} = 24V, V_{LX1} = 19V; V_{BST2} = 24V, V_{LX2} = 19V			5	µA
Resonant Frequency Range	Not tested	30		80	kHz
Minimum Off-Time		240	360	480	ns
Maximum Off-Time		20	30	40	µs
Current-Limit Threshold; LX1 - GND, LX2 - GND		380	400	420	mV
Zero-Crossing Threshold: LX1 - GND, LX2 - GND		5	10	15	mV
IFB Maximum AC Voltage			±3		V
Current-Limit Leading Edge Blanking		240	360	480	ns
IFB Regulation Point	Internally full-wave rectified	770	790	810	mV
IFB Input Bias Current	0 < V_{IFB} < 2V	-3		+3	µA
	-2V < V_{IFB} < 0	-150			

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 24V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IFB Lamp-Out Threshold	Reject 1µs glitches	730	780	830	mV
IFB-to-COMP Transconductance	1V < V_{COMP} < 2.5V		100		µS
COMP Output Impedance			10		MΩ
COMP Discharge Current During Overvoltage or Overcurrent Fault	V_{IFB} = 800mV, V_{ISEC} = 2.5V		1200		µA
COMP Discharge Current During DPWM Off-Time	CNTL = GND, V_{COMP} = 1.5V		100		µA
ISEC Input Bias Current		-0.3		+0.3	µA
ISEC Overcurrent Threshold		1.18	1.22	1.26	V
VFB Input Bias Current	-4V < V_{VFB} < +4V	-25		+25	µA
VFB Overvoltage Threshold		2.10	2.25	2.40	V
Main Oscillator Frequency	R_{HF} = 100kΩ	52.2	53.8	55.4	kHz
Main Oscillator Frequency Range		20		100	kHz
HF, LF, HFCK, LFCK Input-Low Voltage	Slave mode, V_{CNTL} = V_{CC}			0.8	V
HF, LF, HFCK, LFCK Input-High Voltage	Slave mode, V_{CNTL} = V_{CC}	2.1			V
HF, LF, HFCK, LFCK Input Hysteresis	Slave mode, V_{CNTL} = V_{CC}		100		mV
HF, LF, HFCK, LFCK Input Bias Current	Slave mode, V_{CNTL} = V_{CC}	-1		+1	µA
HF Input-Frequency Range	Slave mode, V_{CNTL} = V_{CC}	20		100	kHz
HF, LF, HFCK, LFCK Input Rise and Fall Time	Slave mode, V_{CNTL} = V_{CC}			200	ns
HSYNC, LSYNC Input-Low Voltage				0.8	V
HSYNC, LSYNC Input-High Voltage		2.1			V
HSYNC, LSYNC Input Hysteresis			100		mV
HSYNC, LSYNC Input Bias Current		-1		+1	µA
HSYNC Input Frequency Range		190		460	kHz
HSYNC, LSYNC Input Rise and Fall Time				200	ns
DPWM Chopping Frequency	R_{LF} = 150kΩ	202	208	214	Hz
DPWM Chopping Frequency Range		80		300	Hz

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 24V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LF Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	80		300	Hz
LSYNC Input Frequency Range	R_{LF} = 150kΩ	120		280	Hz
HFCK Input Frequency Range	Slave mode, V_{CNTL} = V_{CC} (Note 1)	120		600	kHz
HFCK, LFCK, PSCK, DPWM Output On-Resistance	I_{TEST} = 1mA			2.4	kΩ
LFCK Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	10.24		38.40	kHz
CNTL Minimum Duty-Cycle Threshold		0.21	0.23	0.26	V
CNTL Maximum Duty-Cycle Threshold		1.9	2.0	2.1	V
CNTL Input Current	0 < V_{CNTL} < 2V	-0.1		+0.1	V
CNTL Input Threshold	Slave mode	4.2	4.5	4.9	V
DPWM Dimming Resolution	Guaranteed monotonic		7		Bits
SEL, PS1, PS2 Input-Low Voltage				0.8	V
SEL, PS1, PS2 Input-High Voltage		2.1			V
SEL, PS1, PS2 Input Hysteresis			100		mV
$\overline{SHDN}$ Input-Low Voltage				0.8	mV
$\overline{SHDN}$ Input-High Voltage	SEL, PS1, PS2 input-high voltage	2.1			V
SEL, PS1, PS2 Input Bias Current	SEL, PS1, PS2 input hysteresis	-1		+1	µA
$\overline{SHDN}$ Input Bias Current		-1		+1	µA
TFLT Charging Current	V_{ISEC} < 1.25 and V_{IFB} < 790mV, V_{FLT} = 2.0V	0.95	1.00	1.05	µA
	V_{ISEC} < 1.25 and V_{IFB} < 790mV, V_{FLT} = 2.0V		-1		
	V_{ISEC} < 1.25 and V_{IFB} < 790mV, V_{FLT} = 2.0V		126		
TFLT Trip Threshold		3.85	4.00	4.15	V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 24V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input-Voltage Range		6		28	V
IN Quiescent Current	$V_{\overline{SHDN}}$ = 5.5V, V_{IN} = 28V			6	mA
IN Quiescent Current, Shutdown	$V_{\overline{SHDN}}$ = 0			20	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SHDN}}$ = 5.5V, 6V < V_{IN} < 28V, 0 < I_{LOAD} < 20mA	5.20		5.50	V
V_{CC} Output Voltage, Shutdown	$V_{\overline{SHDN}}$ = 0, no load	3.50		5.50	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} rising (leaving lockout)			4.5	V
	V_{CC} falling (entering lockout)	4.0			
GH1, GH2, GL1, and GL2 On-Resistance, Low State	I_{TEST} = 10mA, V_{CC} = 5.3V			3	Ω
GH1, GH2, GL1, and GL2 On-Resistance, High State	I_{TEST} = 10mA, V_{CC} = 5.3V			8	Ω
Minimum Off-Time		240		480	ns
Maximum Off-Time		20		40	µs
Current-Limit Threshold: LX1 - GND, LX2 - GND		380		420	mV
Zero-Crossing Threshold: LX1 - GND, LX2 - GND		5		15	mV
Current-Limit Leading-Edge Blanking		240		480	ns
IFB Lamp-Out Threshold	Reject 1µs glitches	730		830	mV
IFB Regulation Point		755		820	mV
ISEC Overcurrent Threshold		1.16		1.26	V
VFB Overvoltage Threshold		2.10		2.40	V
Main Oscillator Frequency	R_{HF} = 100kΩ	51.7		55.9	kHz

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 24V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

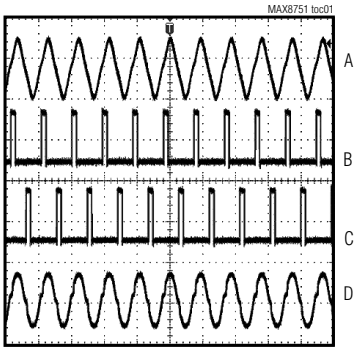
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HF Input-Frequency Range	Slave mode, V_{CNTL} = V_{CC}	20		100	kHz
HSYNC Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	190		460	kHz
HFCK Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	120		600	kHz
DPWM Chopping Frequency	R_{LF} = 150kΩ	202		215	Hz
LF Input Frequency Range	Slave mode, V_{CNTL} = V_{CC}	80		300	Hz
LSYNC Input Frequency Range	R_{LF} = 150kΩ	120		280	Hz
CNTL Minimum Duty Cycle Threshold		0.21		0.26	V
CNTL Maximum Duty Cycle Threshold		1.9		2.1	V
CNTL Input Threshold	Slave mode	4.2		4.9	mV

Note 1: Actual switching frequency is 1/6 of the HFCK.
Note 2: -40°C specifications are guaranteed by design, not production tested.

Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

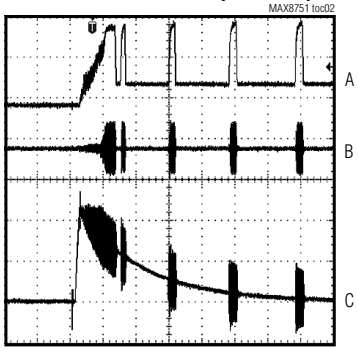
NORMAL OPERATION



20µs/div

A: VFB, 1V/div
B: LX1, 10V/div
C: LX2, 10V/div
D: IFB, 2V/div

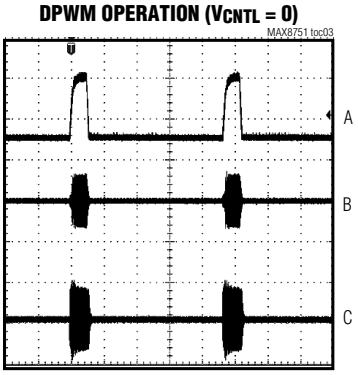
MINIMUM BRIGHTNESS STARTUP WAVEFORM (V_{CNTL} = 0)



2ms/div

A: COMP, 500mV/div
B: IFB, 2V/div
C: VFB, 1V/div

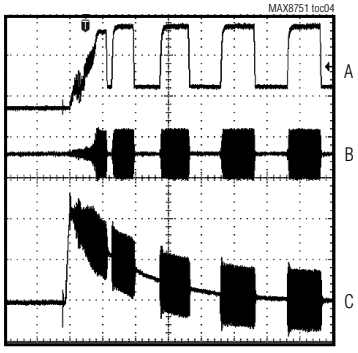
MINIMUM BRIGHTNESS DPWM OPERATION (V_{CNTL} = 0)



1ms/s

A: COMP, 500mV/div
B: IFB, 2V/div
C: VFB, 1V/div

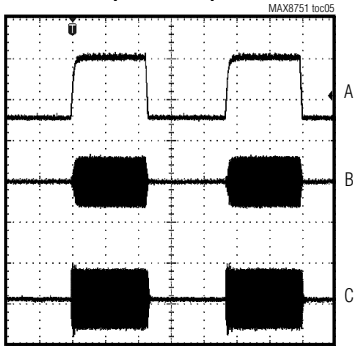
50% BRIGHTNESS STARTUP WAVEFORM



2ms/div

A: COMP, 500mV/div
B: IFB, 2V/div
C: VFB, 1V/div

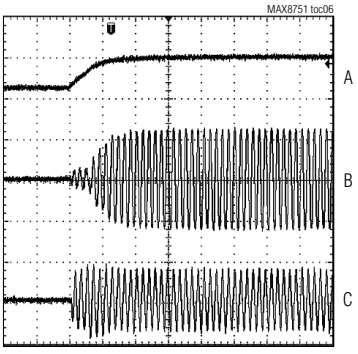
50% BRIGHTNESS DWPM WAVEFORM (V_{CNTL} = 1V)



1ms/div

A: COMP, 500mV/div
B: IFB, 2V/div
C: VFB, 1V/div

DPWM SOFT-START



100µs/div

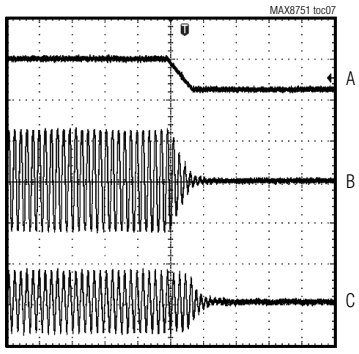
A: COMP, 1V/div
B: IFB, 1V/div
C: VFB, 1V/div

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Typical Operating Characteristics (continued)

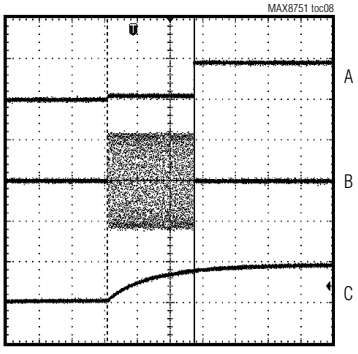
(Circuit of Figure 1. V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

DPWM SOFT-START



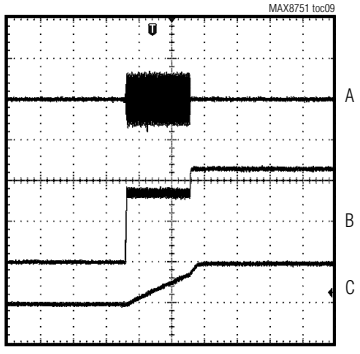
A: COMP, 1V/div
B: IFB, 1V/div
C: VFB, 1V/div

LAMP-OUT VOLTAGE LIMITING AND TIMEOUT



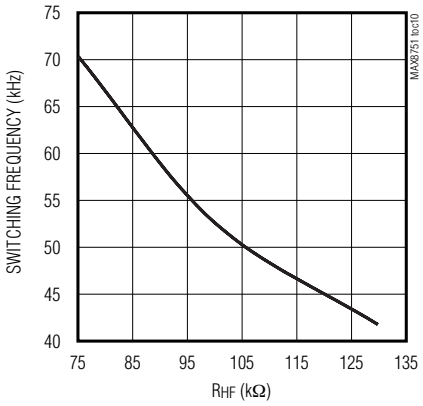
A: COMP, 5V/div
B: VFB, 2V/div
C: TFLT, 5V/div

SECONDARY SHORT-CIRCUIT PROTECTOR AND TIMEOUT

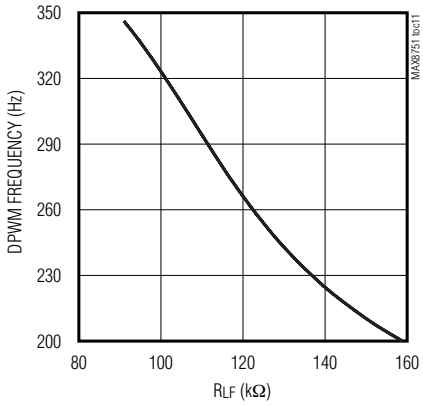


A: ISEC, 2V/div
B: COMP, 2V/div
C: TFLT, 5V/div

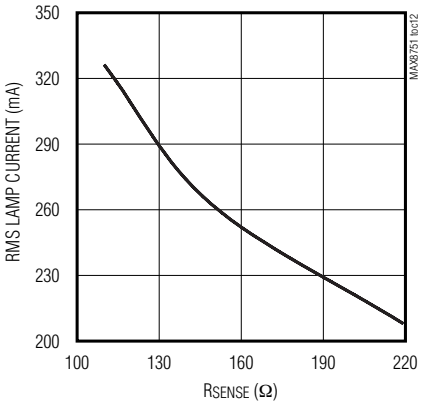
SWITCHING FREQUENCY vs. R_{HF}



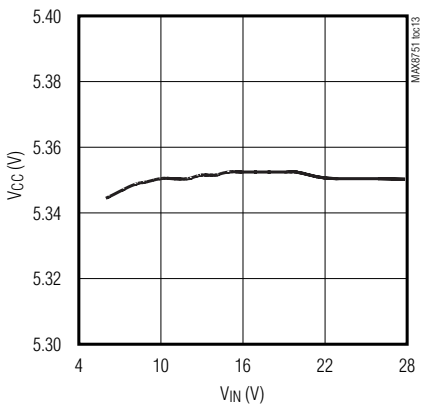
DPWM FREQUENCY vs. R_{LF}



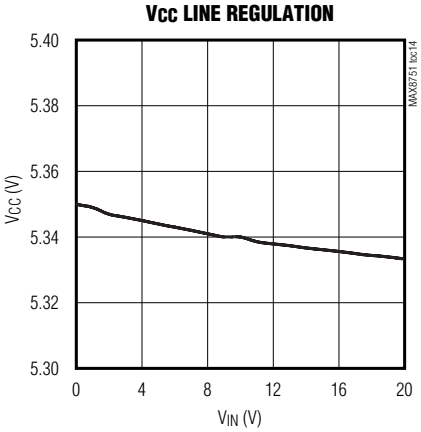
RMS LAMP CURRENT vs. R_{SENSE}



V_{CC} LINE REGULATION



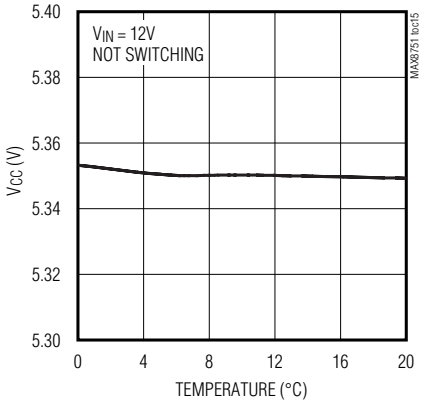
V_{CC} LINE REGULATION



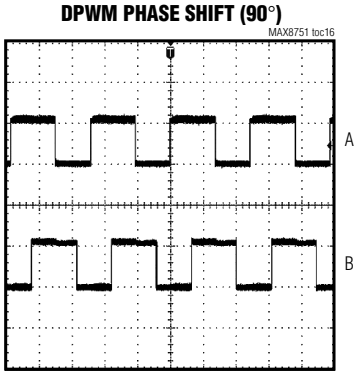
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

VCC vs. TEMPERATURE



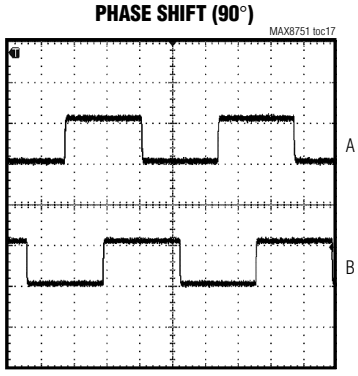
DPWM PHASE SHIFT (90°)



2ms/div

A: MASTER DPWM, 5V/div
B: SLAVE DPWM, 5V/div

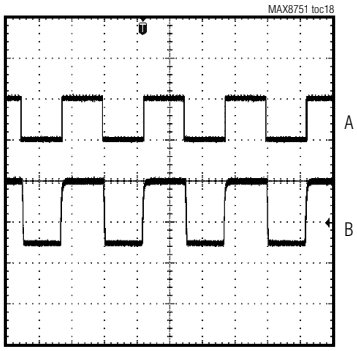
SWITCHING FREQUENCY PHASE SHIFT (90°)



4µs/div

A: MASTER PSCK, 5V/div
B: SLAVE PSCK, 5V/div

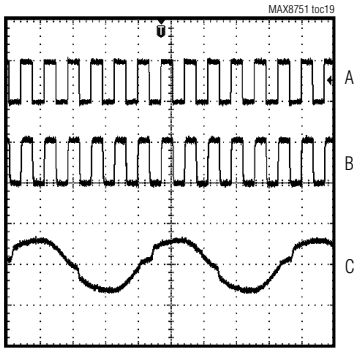
LF SYNCHRONIZATION



2ms/div

A: LSYNC, 5V/div
B: COMP, 500mV/div

HF SYNCHRONIZATION



4µs/div

A: HSYNC, 5V/div
B: HFCIC, 5V/div
C: IFB, 2V/div

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Pin Description

PIN	NAME	FUNCTION
1	VFB	Transformer Secondary Voltage-Feedback Input. VFB pin sets secondary overvoltage limit by using a capacitive voltage-divider between the high voltage of the CCFL lamp and GND. When the peak voltage on VFB exceeds the internal overvoltage threshold, the controller turns on an internal current sink, discharging the COMP capacitor, limiting the secondary voltage. See the *Transformer Secondary Voltage Limiting* section for details.
2	TFLT	Fault Timer-Adjustment Pin. A fault condition sets an internal current source to charge a capacitor connected between TFLT and GND. Connect a capacitor from TFLT to GND to set the timeout period for open-lamp fault and secondary short-circuit faults. See the *Lamp-Out Protection* section for details.
3	CNTL	Brightness Control Input. The usable brightness control range is from 0 to 2V. V_{CNTL} = 0 represents minimum brightness (10% DPWM duty cycle), V_{CNTL} = 2V represents full brightness (100% DPWM duty cycle). When V_{CNTL} is between 2V and 3V, the brightness is still 100%. The MAX8751 enters into slave mode when CNTL is connected to V_{CC}. See the *DPWM Dimming Control* section for details.
4	$\overline{SHDN}$	Shutdown Control Input. The MAX8751 shuts down when $\overline{SHDN}$ is pulled to GND.
5	LSYNC	DPWM Sync Input. DPWM frequency can be synchronized with an external signal on LSYNC. When SEL is connected to V_{CC}, the duty cycle of the LSYNC signal determines the brightness.
6	LFCK	Internal DPWM Oscillator Clock Output. LFCK becomes a logic-level input when CNTL is connected to V_{CC}.
7	DPWM	DPWM Signal Output. The DPWM output is used to control the DPWM frequency of the slave IC in master-slave operation. See the *Slave Operation (HFCK, LFCK, PSCK, DPWM)* section for details.
8	PSCK	Phase-Shift Clock Output. See the *Slave Operation (HFCK, LFCK, PSCK, DPWM)* and *Phase Shift (PS1, PS2)* sections for details.
9	HFCK	Main Switching Oscillator Clock Output. HFCK is a logic-level input when CNTL is connected to V_{CC}.
10	HSYNC	Main Switching Frequency Sync Input. Switching frequency can be synchronized with an external signal on HSYNC.
11	SEL	Brightness Control Select Input. Brightness can be adjusted with an analog voltage on CNTL or with an external sync signal. Connecting SEL to V_{CC} enables analog control input. Connect SEL to V_{CC} to enable brightness control using external sync signal.
12	LF	Frequency Adjustment Pin for Internal DPWM Oscillator. Connect a resistor from LF to GND to set the internal DPWM oscillator frequency. f_{DPWM} = 208Hz × 150kΩ / R_{LF}. LF becomes a logic-level input when CNTL is connected to V_{CC}. See the *DPWM Dimming Control* section for details.
13	HF	Frequency Adjustment Pin for Main Switching Oscillator. Connect a resistor from HF to GND to set the main oscillator frequency. f_{SW} = 54kHz × 100kΩ / R_{HF}. HF is a logic-level input when CNTL is connected to V_{CC}.
14	PS1	Phase-Shift Select Input for Slave. For details, see the *Slave Operation (HFCK, LFCK, PSCK, DPWM)* section.
15	PGND2	Power Ground. PGND is the return for the GL2 gate driver.
16	GL2	Gate-Driver Output for Low-Side MOSFET NL2
17	BST2	High-Side Gate Driver GH2 Supply Input. The MAX8751 includes an integrated boost diode. Connect a 0.1µF capacitor between LX2 and BST2 to complete the bootstrap circuit.

Pin Description (continued)

PIN	NAME	DESCRIPTION
18	GH2	Gate-Driver Output for High-Side MOSFET NH2
19	LX2	Gate-Driver Return for GH2. LX2 is the input to the primary current-limit and zero-crossing comparators. The controller senses the voltage across the low-side MOSFET NL2 (LX2 - GND) for primary overcurrent condition and zero-crossing detection.
20	IN	Supply Input. Input to the internal 5.3V linear regulator that powers the device. Bypass IN to GND with a 0.1µF ceramic capacitor.
21	V_{CC}	5.3V/20mA Linear Regulator Output. Supply voltage for the device including the low-side gate drivers GL1 and GL2. Bypass V_{CC} with a 1.0µF ceramic capacitor to GND.
22	LX1	Gate Driver Return for GH1. LX1 is the input to the primary current-limit and zero-crossing comparators. The controller senses the voltage across the low-side MOSFET NL1 (LX1 - GND) for primary overcurrent condition and zero-crossing detection.
23	GH1	Gate Driver Output for High-Side MOSFET NH1
24	BST1	High-Side Gate-Driver GH1 Supply Input. The MAX8751 includes an integrated boost diode. Connect a 0.1µF capacitor between LX1 and BST1 to complete the bootstrap circuit.
25	GL1	Gate-Driver Output for Low-Side MOSFET NL1
26	PGND1	Power Ground. PGND is the return for the GL1 gate driver.
27	GND	System Ground
28	PCOMP	Compensation Node of the Phase-Lock Loop. Connect a 0.1µF capacitor between PCOMP and GND to compensate the PLL.
29	COMP	Transconductance Error-Amplifier Output. A compensation capacitor of 0.01µF connected between COMP and GND stabilizes the controller. The rise and fall time of the lamp-current envelope in DPWM operation is also determined by the COMP capacitor.
30	IFB	Lamp Current-Feedback Input. The IFB sense signal is internally full-wave rectified. The average value of the rectified signal is regulated to 790mV (typ) by controlling the on-time of the high-side MOSFET. An open-lamp fault is generated if the IFB is continuously below 790mV (typ) for a period set by TFLT. See the *Lamp-Out Protection* and *Setting the Fault-Delay Time* sections for details.
31	PS2	Phase-Shift Select Input for Slave. For details, see the *Slave Operation (HFCK, LFCK, PSCK, DPWM)* section.
32	ISEC	Transformer Secondary Current-Feedback Input. When the average voltage on ISEC exceeds the internal overcurrent threshold, the controller turns on an internal current sink, discharging the COMP capacitor. An RC current-sense network connected between the low-voltage end of the transformer secondary and the ground allows setting the maximum secondary current during short-circuit fault.
—	PAD	Exposed Backside Pad. Connect PAD to GND.

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

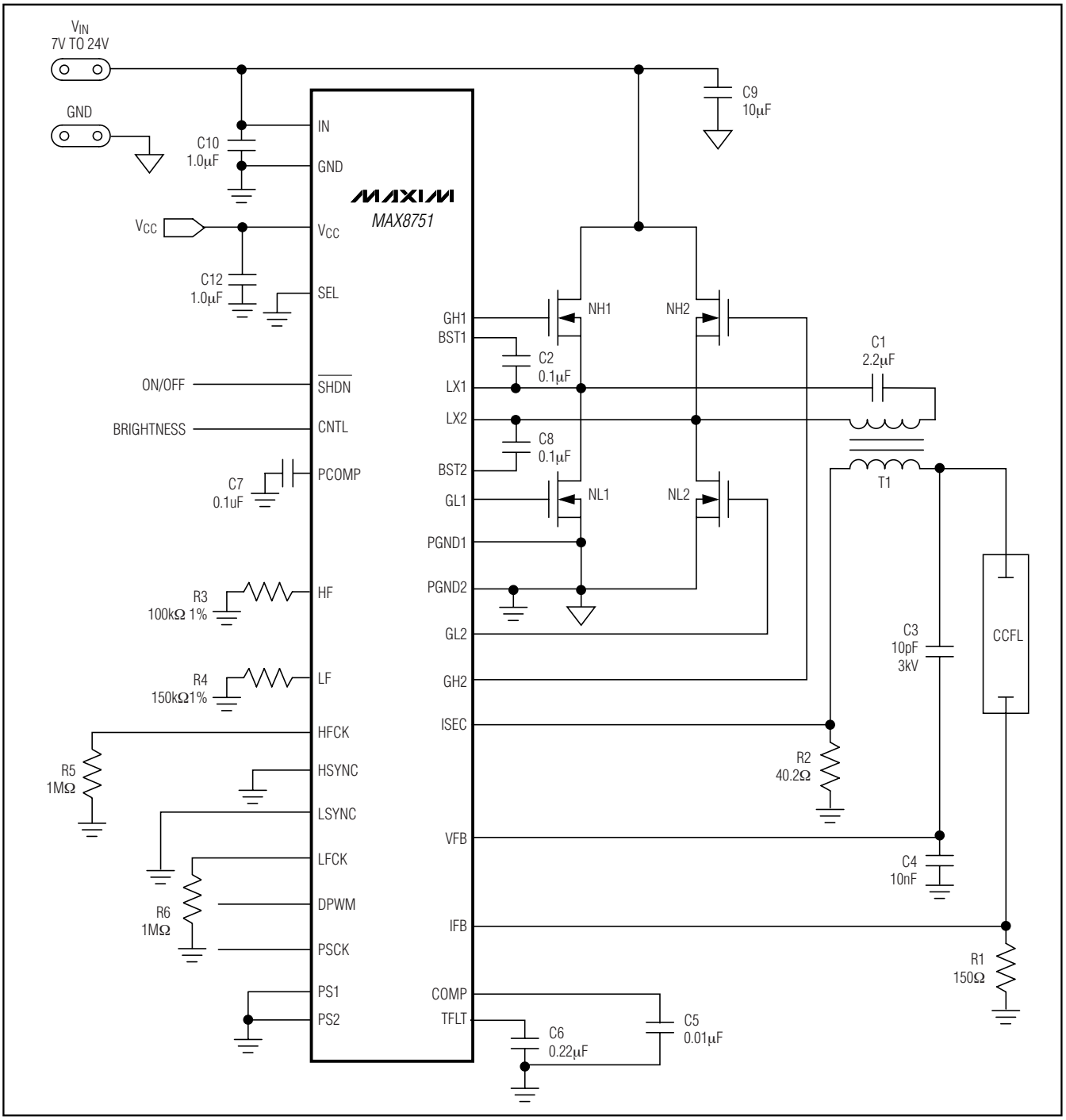


Figure 1. Stand-Alone Typical Operating Circuit

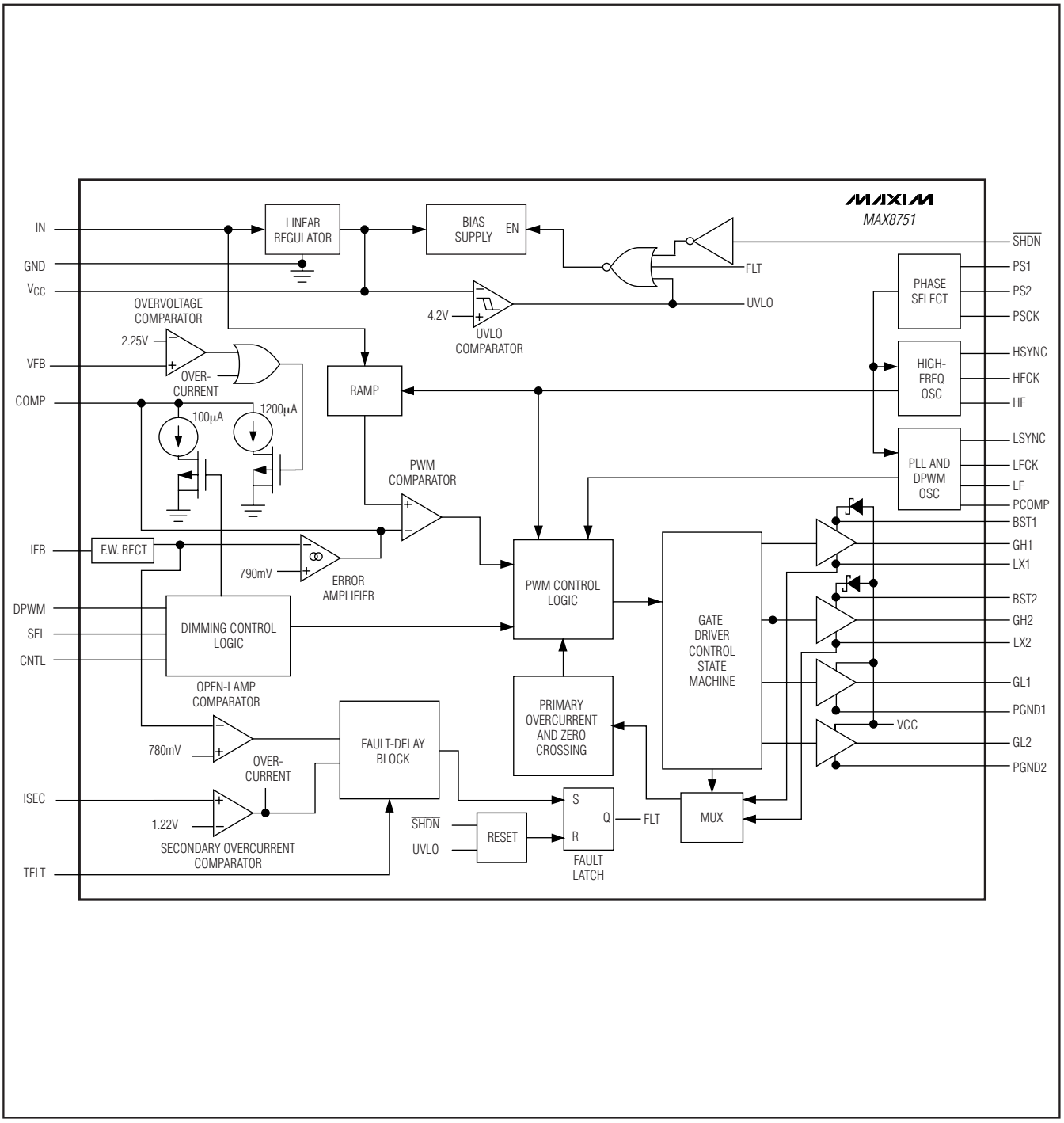


Figure 2. Functional Diagram

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Detailed Description

Figure 1 shows the *Stand-Alone Typical Operating Circuit* and Figure 2 shows the *Functional Diagram* of the MAX8751. The circuit in Figure 1 consists of a full-bridge inverter, which converts unregulated DC input voltage into a nearly sinusoidal high-frequency, AC output for powering CCFLs. The MAX8751 is biased from an internal 5.35V linear regulator with UVLO comparator that ensures stable operation and clean startup characteristics. The MAX8751 includes several layers of fault-protection circuitry, consisting of comparators for detecting primary-side current limit, secondary-side overvoltage, secondary short circuit, and open-lamp faults. A logic block arbitrates the comparator outputs by making sure that a given fault persists for a minimum duration before registering the fault condition. A separate block provides dimming control based upon analog or DPWM inputs. Finally, a dedicated logic circuit provides synchronization and phase-control functions for daisy-chaining up to five MAX8751s without phase overlap.

The MAX8751 operates in resonant mode during striking and switches over to constant-frequency operation after the IFB voltage rises above the open-lamp threshold. Reliable striking of all lamps is ensured by using individual transformer secondary winding for each lamp, or by using ballast capacitors if multiple lamps are driven by single transformer secondary. The constant-frequency architecture supported by the MAX8751 can be synchronized and phase shifted for daisy-chained applications. Multiple lamps can also be driven in parallel within a single stage. The MAX8751 has sufficient gate drive strength to drive the large-power MOSFETs needed when one power stage drives four or more CCFL lamps in parallel.

The MAX8751 provides accurate lamp-current regulation. A primary-side current sense provides cycle-by-cycle current limit and zero-crossing detection, while the lamp current is sensed with a separate loop that provides fine adjustment of the lamp current with an external resistor. The MAX8751 controls lamp brightness by turning the CCFL on and off using a DPWM method, while maintaining approximately constant lamp current. The brightness set point can be adjusted with an analog voltage on the CNTL pin, or with an external PWM signal.

The MAX8751 has a single compensation input (COMP), which also establishes the soft-start and soft-stop timing characteristics. Control logic changes the available drive current at COMP based on the operating mode to adjust the inverter's dynamic behavior.

Constant-Frequency Operation

The MAX8751 operates in constant-frequency mode in normal operation. There are two ways to set the switching frequency:

1) The switching frequency can be set with an external resistor connected between HF and GND. The switching frequency is given by the following equation:

$$f_{SW} = 54kHz \times \frac{100k\Omega}{R_{HF}}$$

The adjustable range of the switching frequency is between 20kHz and 100kHz (R_{HF} is between 270kΩ and 54kΩ).

2) The switching frequency can be synchronized by an external high-frequency signal. Connect HF to GND through a 100kΩ resistor and connect HSYNC to the external high-frequency signal. The resulting switching frequency (f_{SW}) is 1/6 the frequency of the external signal (f_{SYNC}):

$$f_{SW} = \frac{f_{SYNC}}{6}$$

The frequency range of the external signal should be between 120kHz and 600kHz, resulting in a switching frequency range between 20kHz and 100kHz.

Figure 3 is the timing diagram of constant-frequency operation, showing the primary current, internal oscillator, and gate signals. At the beginning of the positive half cycle, switches NH1 and NL2 are ON (see Figure 1), and the primary current ramps up. The controller turns off NH1 when the primary current reaches it peak, which is set by the COMP voltage. The primary current continues to flow through the freewheeling body diode of NL1. Next, the low-side switch NL1 is turned on under zero-voltage switching (ZVS) conditions. Now the primary current starts ramping down. The falling edge of the internal oscillator turns off NL2 and turns on NH2, starting the negative half cycle. The fixed-frequency operation continues with the inverter controlling the full-bridge MOSFETs to produce near the sinusoidal lamp-current waveform.

Resonant Startup

The MAX8751 operates in resonant mode during startup. In the resonant mode, the switching frequency is synchronized with the natural resonant frequency of the resonant tank circuit. The synchronization and phase-shift functions are disabled during startup. Figure 4 is the timing diagram of the resonant operation showing the primary current and gate signals. In the resonant

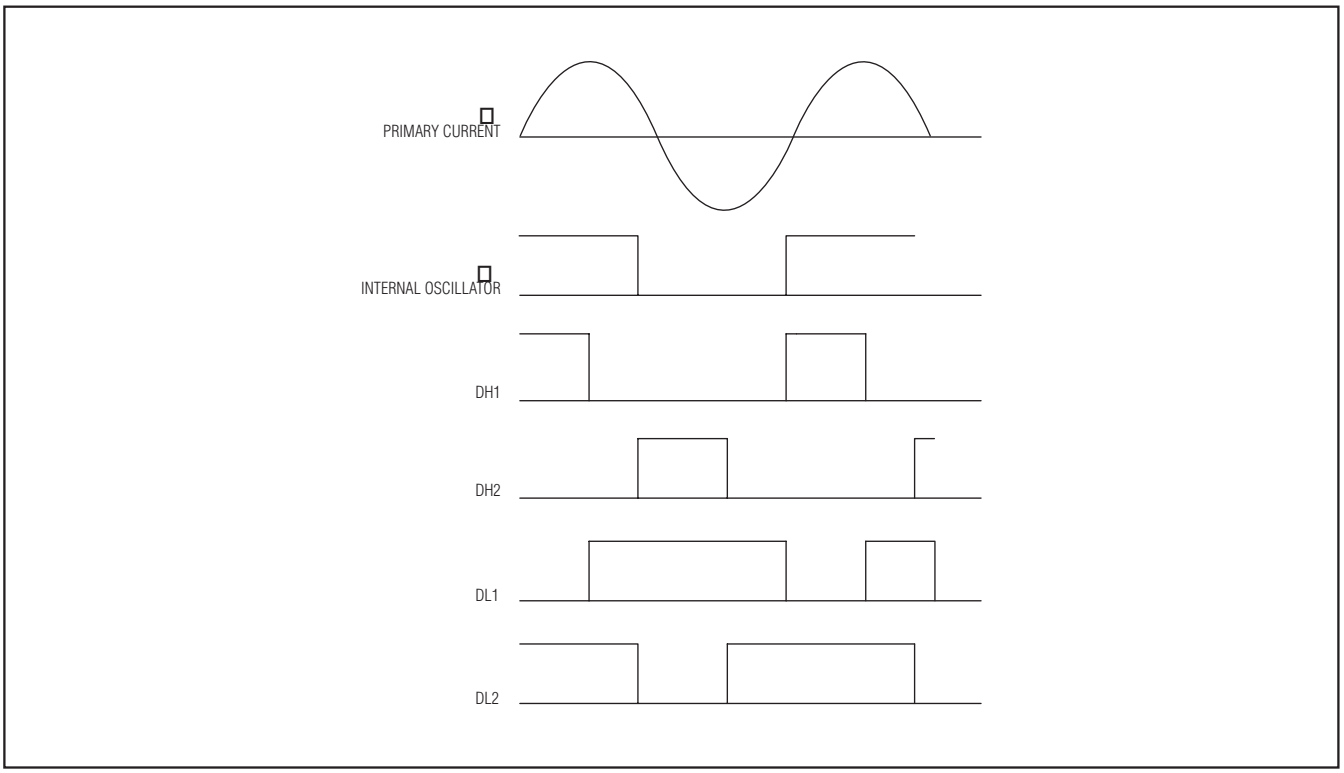


Figure 3. Fixed-Frequency Timing Diagram

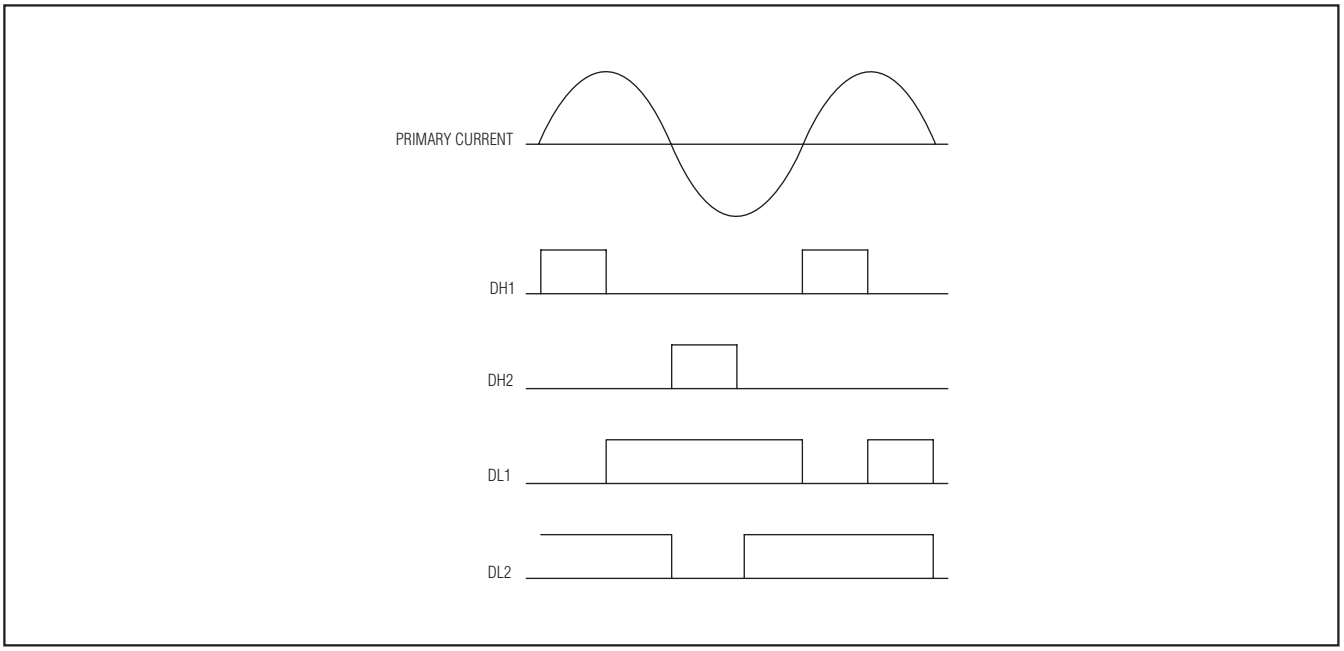


Figure 4. Resonant Operation Timing Diagram

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

mode, at the beginning of the positive half cycle, NH1 and NL2 turn on and the primary current starts ramping up. The controller turns off NH1 as the primary current reaches its peak value. The primary current continues to flow in the same direction, which forward biases the body diode of NL1, ramping down the primary current. When the primary current reaches zero, NL2 is turned off and NH2 is turned on, starting the negative half cycle.

Lamp-Current Regulation

The MAX8751 uses a lamp-current control loop to regulate the current delivered to the CCFL. The heart of the control loop is a transconductance error amplifier in Figure 2. The AC lamp current is sensed with a sense resistor connected in series with the low-voltage terminal of the lamp. The voltage across this resistor is fed to the IFB input and is internally full-wave rectified. The transconductance error amplifier compares the rectified IFB voltage with a 790mV (typ) internal reference to generate an error current. The error current charges and discharges a capacitor connected between the error amplifier's output (COMP) and ground to create an error voltage (V_{COMP}). V_{COMP} is then compared with an internal ramp signal to control the high-side MOSFET switch on-time (t_{ON}).

Transformer Secondary Voltage Limiting

The MAX8751 reduces the voltage stress on the transformer's secondary winding by limiting the secondary voltage during startup and open-lamp condition. The AC voltage across the transformer secondary winding is sensed through a capacitive voltage-divider. The voltage across the low-side capacitor of the divider is fed to the VFB pin of the MAX8751. An overvoltage comparator compares the VFB voltage with 2.25V (typ) internal threshold. If the sensed voltage exceeds the overvoltage threshold, the MAX8751 turns on an internal 1200µA current source, which discharges the COMP capacitor. The high-side MOSFET's on-time shortens as the COMP voltage decreases, hence reducing the transformer's secondary peak voltage below the threshold set by the capacitive voltage-divider.

Lamp Startup

A CCFL is a gas-discharge lamp that is normally driven in the avalanche mode. To start ionization in a nonionized lamp, the applied voltage (striking voltage) must be increased to the level required for the start of avalanche. For example, the normal running voltage of a typical CCFL is approximately $650V_{RMS}$, but the striking voltage can be as high as $1800V_{RMS}$.

The MAX8751's unique resonant startup method ensures reliable striking. Before the lamp is ionized, the lamp impedance is infinite. The transformer secondary leakage inductance and the high-voltage parallel capacitor determine the unloaded resonant frequency. Since the unloaded resonant circuit has a high Q, the inverter keeps increasing the secondary voltage until either the lamp is struck or the controller activates the secondary overvoltage protection.

Upon power-up, V_{COMP} slowly rises, increasing the duty cycle of the high-side MOSFET switches and providing a measure of soft-start. In addition, the MAX8751 pulls up V_{FB} to the overvoltage threshold (2.25V, typ) immediately after the device is enabled. The DC voltage on V_{FB} is gradually discharged through an internal resistor during startup. This feature is equivalent to slowly raising the overvoltage threshold during startup, so it further improves the soft-start behavior. The MAX8751 automatically switches over to constant-frequency operation after the IFB voltage rises above open-lamp threshold.

Feed-Forward Control and Dropout Operation

The MAX8751 is designed to maintain tight control of the lamp current under all transient conditions. The feed-forward control instantaneously adjusts the on-time for changes in input voltage (V_{IN}). This feature provides immunity to input-voltage variations and simplifies loop compensation over wide-input voltage ranges. The feed-forward control also improves the line regulation for short DPWM on-times and makes startup transients less dependent on the input voltage.

Feed-forward control is implemented by increasing the internal voltage ramp rate for higher V_{IN}. This has the effect of varying t_{ON} as a function of the input voltage while maintaining almost the same signal levels at V_{COMP}. Since the required voltage change across the compensation capacitor is minimal, the controller's response to input voltage change is essentially instantaneous.

DPWM Dimming Control

The MAX8751 controls the brightness of the CCFL by "chopping" the lamp current on and off using a low-frequency (between 80Hz and 300Hz) DPWM signal either from the internal oscillator or from an external signal source. In the DPWM operation, COMP controls the rise and fall of the lamp current. At the beginning of the DPWM on-cycle, the lamp current is zero; V_{COMP} linearly rises due to charging from transconductance error amplifier, and t_{ON} increases gradually, increasing the lamp current slowly, providing soft-start. The lamp current stabilizes after it reaches the regulation point. At

the end of the DPWM on-cycle, the dimming control logic turns on a 100µA internal current source, thus discharging the COMP capacitor linearly, gradually decreasing t_{ON} and bringing lamp current to zero, thus providing soft-start. The dimming control for the CCFL is provided by changing the duty ratio of the low-frequency DPWM signal.

Using the Internal Oscillator

When the MAX8751 is not using an external synchronization signal, the DPWM signal is generated using an internal oscillator. The frequency of the internal DPWM oscillator is adjustable through a resistor connected between LF and GND. The DPWM frequency is given by the following equation:

$$f_{DPWM} = \frac{208Hz \times 150k\Omega}{R_{LF}}$$

The adjustable range of the DPWM frequency is between 80Hz and 300Hz (R_{LF} is between 390kΩ and 104kΩ).

The CCFL brightness is proportional to the DPWM duty cycle, which can be adjusted from 10% to 100% through the CNTL pin. CNTL is an analog input with a usable input voltage range between 0 and 2000mV, which is digitized to select one of 128 brightness levels. As shown in Figure 5, the MAX8751 ignores the first 13 steps, and the first 13 steps (V_{CNTL} between 0 and 203mV) all represent 10% brightness. When V_{CNTL} is above 203mV, a 15.625mV change on CNTL results in a 0.78% change in the DPWM duty cycle. When V_{CNTL} is equal to or above 2000mV, the DPWM duty cycle is always 100%.

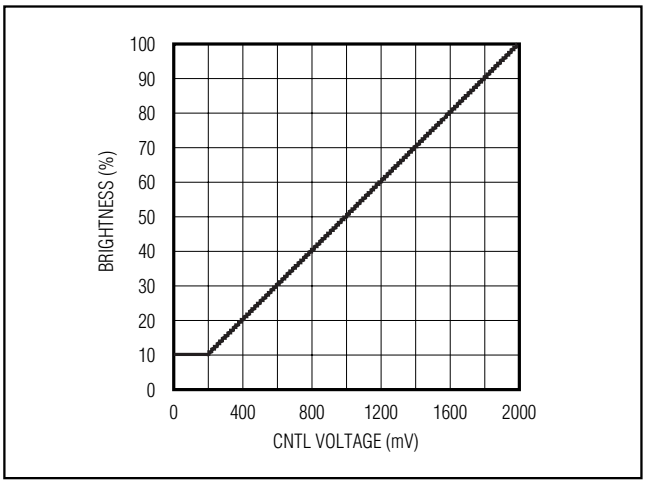


Figure 5. Brightness vs. CNTL Voltage

Using the External DPWM Signal

To use the external DPWM signal to control the brightness, connect SEL to V_{CC} and connect LSYNC to the external signal source. The frequency range of the external signal is within ±40% of the internal oscillator frequency set by R_{LF}. In this mode, the brightness control input CNTL is disabled, and the brightness is proportional to the duty cycle of the external signal. When the duty cycle of the external signal is 100%, the CCFL reaches full brightness. If the duty cycle of the external signal is less than 10%, the CCFL brightness stays at 10%.

Lamp-Out Protection

For safety, the IFB pin on MAX8751 monitors the lamp current to detect faulty or open CCFL lamps. As described in the *Lamp-Current Regulation* section, the voltage on IFB is internally full-wave rectified. If the rectified IFB voltage is below 790mV, the MAX8751 charges the TFLT capacitor with a 1µA current source. The fault latch is set if the voltage on TFLT exceeds 4V. Unlike normal shutdown mode, the linear regulator out (V_{CC}) remains at 5.35V. Toggling $\overline{SHDN}$ or cycling the input power reactivates the device.

During the fault delay period, the current-control loop tries to maintain the lamp-current regulation by increasing the on-time of high-side MOSFETs. Because the lamp impedance is very high when it is open, the transformer secondary rises as a result of the high-Q factor of the resonant tank. Once the secondary voltage exceeds the overvoltage threshold, the MAX8751 turns on a 1200µA internal current source that discharges the COMP capacitor. The on-time of the high-side MOSFETs is reduced, lowering the secondary voltage, as the COMP voltage decreases. Therefore, the peak voltage of the transformer secondary winding never exceeds the limit during the lamp-out delay period.

Primary Overcurrent Protection

The MAX8751 provides cycle-by-cycle primary overcurrent protection. A current-sense amplifier monitors the drain-to-source voltages of both the high-side and low-side switches when the switches are conducting. If the voltage exceeds the internal current-limit threshold (400mV typ), the regulator turns off the high-side switch at the opposite side of the primary to prevent the transformer primary current from increasing further.

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Secondary Current Limit (ISEC)

The secondary current limit provides fail-safe protection in case of short circuit or leakage from the high-voltage terminal to ground. ISEC monitors the voltage across a sense resistor placed between the transformer's low-voltage secondary terminal and ground. The ISEC voltage is continuously compared to the ISEC regulation threshold (1.22V, typ). Any time the ISEC voltage exceeds the threshold, a controlled current is drawn from COMP to reduce the on-time of the bridge's high-side switches. At the same time, the MAX8751 charges the TFLT capacitor with a 126µA current. The MAX8751 latches off when the voltage on TFLT exceeds 4V.

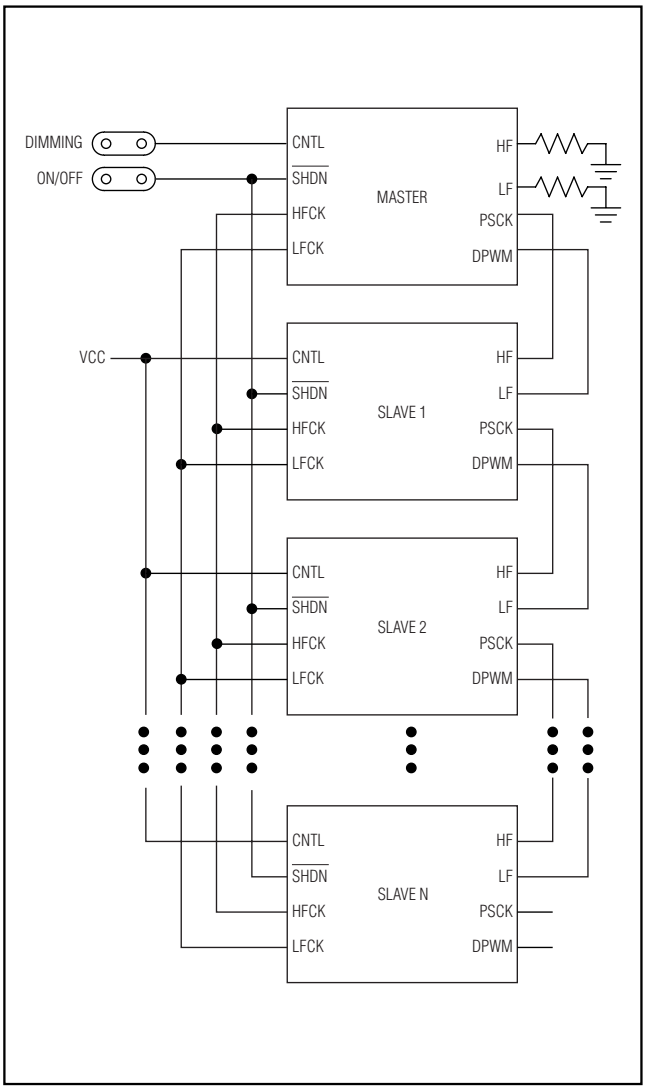


Figure 6. Master-Slave Operation

Unlike the normal shutdown mode, the linear regulator output (V_{CC}) remains at 5.35V. Toggling $\overline{SHDN}$ or cycling the input power reactivates the device.

Slave Operation (HFCK, LFCK, PSCK, DPWM)

The MAX8751 supports master-slave operation. Up to five MAX8751s can be connected in a daisy-chain configuration as shown in Figure 6. The same device can be used either as a master IC or as a slave IC. Each MAX8751 is the master of the next IC in the chain and at the same time, it is also the slave of the previous IC in the chain.

Connecting CNTL to V_{CC} enables the slave mode. In the slave mode, the switching frequency and DPWM frequency are synchronized with the previous MAX8751 in the chain. To synchronize the switching frequency, connect the HFCK pins of the slave IC and master IC together, and connect the PSCK pin of the master IC to the HF pin of the slave IC. To synchronize the DPWM frequency, connect the LFCK pins of the slave IC and master IC together, and connect the DPWM pin of the master IC to the LF pin of the slave IC. The CNTL brightness control is disabled in the slave mode. The master directly controls the brightness setting of the slave by connecting the DPWM pin of master to LF pin of slave.

Phase Shift (PS1, PS2)

The MAX8751 provides phase shift for both the DPWM operation and switching of MOSFETS when connected in a daisy-chain configuration. This phase shift reduces input ripple current, hence significantly reducing input RMS current. This reduction of input RMS current reduces the input capacitor requirement, hence the size of capacitor. The phase shift can be programmed using two logic input pins (PS1 and PS2). These two pins combined together give four choices of phase shift: 72°, 90°, 120°, and 180°. The selection of the phase shift is based on the number of MAX8751s used in the daisy-chain. Use the following equation to determine the appropriate phase shift:

$$\text{Phase shift} = 360° / \text{number of phases}$$

Table 1 gives the suggested selection of phase shift for different number of phases. All master and slave ICs should use the same setting for PS1 and PS2.

Table 2 summarizes the MAX8751's operation in all modes.

Table 1. Phase-Shift Setting

PIN SETTING		PHASE SHIFT IN DEGREES					NO. OF PHASES
PS2	PS1	MASTER	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4	
X	X	0	N/A	N/A	N/A	N/A	1
GND	GND	0	180	N/A	N/A	NA	2
GND	V_{CC}	0	120	240	N/A	N/A	3
V_{CC}	GND	0	90	180	270	N/A	4
V_{CC}	V_{CC}	0	72	144	216	288	5

X = Don't care.

Linear Regulator Output (V_{CC})

The internal linear regulator steps down the DC input voltage to 5.3V (typ). The linear regulator supplies power to the internal control circuitry of the MAX8751. V_{CC} powers the MOSFET gate drivers. The V_{CC} voltage drops to 4.5V in shutdown.

UVLO

The MAX8751 includes an undervoltage lockout (UVLO) circuit. The UVLO circuit monitors the V_{CC} voltage. When V_{CC} is below 4.2V (typ), the MAX8751 disables both high-side and low-side gate drivers and resets the fault latch.

Low-Power Shutdown

When the MAX8751 is placed in shutdown, all functions of the IC are turned off except for the 5.3V linear regulator. In shutdown, the linear regulator output voltage drops to about 4.5V and the supply current is 6µA (typ). While in shutdown, the fault latch is reset. The device can be placed into shutdown by pulling $\overline{SHDN}$ to its logic low level.

Applications Information

MOSFETs

The MAX8751 requires four external n-channel power MOSFETs to form a full-bridge inverter circuit to drive the transformer primary. Since the positive half-cycle and negative half-cycle are symmetrical, the same type of MOSFET should be used for the high-side and low-side switches. When selecting the MOSFET, focus on the voltage rating, current rating, on-resistance ($R_{DS(ON)}$), total gate charge, and power dissipation.

Select a MOSFET with a voltage rating at least 25% higher than the maximum input voltage of the inverter. For example, if the maximum input voltage is 24V, the voltage rating of the MOSFET should be 30V or higher. The current rating of the MOSFET should be higher than the peak primary current at the minimum input voltage and full brightness. Use the following equation to estimate the primary peak current I_{PEAK_PRI}:

$$I_{PEAK\_PRI} = \frac{\sqrt{2} \times P_{OUT\_MAX}}{V_{IN\_MIN} \times \eta}$$

where P_{OUT_MAX} is the maximum output power, V_{IN_MIN} is the minimum input voltage, and is the estimated efficiency at the minimum input voltage. Assuming the full bridge drives four CCFLs and the maximum output power of each lamp is 4.5W, the total maximum output power is 18W. If the minimum input voltage is 8V and the estimated efficiency is 75% at that input, the peak primary current is approximately 4.3A. Therefore, power MOSFETs with a DC current rating of 5A or greater are sufficient.

Since the regulator senses the on-state, drain-to-source voltage of both MOSFETs to detect the transformer primary current, the lower the MOSFET $R_{DS(ON)}$, the higher the current limit is. Therefore, the user should select n-channel MOSFETs with low $R_{DS(ON)}$ to minimize conduction loss, and keep the primary current limit at a reasonable level. Use the following equation to estimate the maximum and minimum values of the primary current limit:

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Table 2. Operation Summary

PIN	MASTER MODE USING INTERNAL OSCILLATORS	MASTER MODE USING EXTERNAL SYNC SIGNAL (SYNC ONLY)	MASTER MODE USING EXTERNAL SYNC SIGNAL (SYNC AND DIMMING)	SLAVE MODE
CNTL	An analog voltage on CNTL sets the brightness.	An analog voltage on CNTL sets the brightness.	CNTL control is disabled. The external signal controls the brightness. Connect CNTL to an analog voltage in case the external sync signal is lost.	Connect CNTL to V_{CC}.
SEL	Connect SEL to GND.	Connect SEL to GND.	Connect SEL to V_{CC}.	Don't care.
HF	Connect a resistor to GND to set the switching frequency.	The internal oscillator is not active. Connect a resistor to GND in case the external sync signal is lost.	The internal oscillator is not active. Connect a resistor to GND in case the external sync signal is lost.	Connect to the PSCK pin of its master controller.
LF	Connect a resistor between LF and GND to set DPWM frequency.	The internal oscillator is not active. Connect a resistor to GND in case the external sync signal is lost.	The internal oscillator is not active. Connect a resistor to GND in case the external sync signal is lost.	Connect to the DPWM pin of its master controller.
HFCK	Connect to the HFCK pin of its slave controller. Connect 1MΩ resistor to GND. See Note 1.	Connect to the HFCK pin of its slave controller. Connect 1MΩ resistor to GND. See Note 1.	Connect to the HFCK pin of its slave controller. Connect 1MΩ resistor to GND. See Note 1.	Connect to the HFCK pin of its master controller. Connect 1MΩ resistor to GND. See Note 1.
LFCK	Connect to the LFCK pin of its slave controller. Connect 1MΩ resistor to GND. See Note 1.	Connect to the LFCK pin of its slave controller. Connect 1MΩ resistor to GND. See Note 1.	Connect to the LFCK pin of its slave controller. Connect 1MΩ resistor to GND. See Note 1.	Connect to the LFCK pin of its master controller. Connect 1MΩ resistor to GND. See Note 1.
HSYNC	Not used. Connect to GND.	Connect to a high-frequency external signal to sync the switching frequency.	Connect to a high-frequency external signal to sync the switching frequency.	Not used. Connect to GND.
LSYNC	Not used. Connect to GND.	Connect a low-frequency external signal to sync the DPWM frequency.	Connect a low-frequency external signal to sync the DPWM frequency. The duty cycle of the external signal determines the brightness.	Not used. Connect to GND.
PSCK	Connect to the HF pin of its slave controller.	Connect to the HF pin of its slave controller.	Connect to the HF pin of its slave controller.	Connect to the HF pin of its slave controller.
DPWM	Connect to the LF pin of its slave controller.	Connect to the LF pin of its slave controller.	Connect to the LF pin of its slave controller.	Connect to the LF pin of its slave controller.

Note 1: *1MΩ resistor at HFCK and LPCK is added to define the state of the pins in Shutdown mode.*

$$I_{LIM\_MIN} = \frac{380mV}{R_{DS(ON)\_MAX}}$$

$$I_{LIM\_MAX} = \frac{420mV}{R_{DS(ON)\_MIN}}$$

MOSFETs must be able to dissipate the conduction losses plus the switching losses at both V_{IN_MIN} and V_{IN_MAX}. Calculate both terms. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of the MOSFETs. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider choosing MOSFETs with lower parasitic capacitance. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the conduction losses equal the switching losses.

Calculate the total conduction power dissipation of the two MOSFETs using the following equation:

$$PD_{CONDUCT} = I_{PRI}^2 \times R_{DS(ON)}$$

where I_{PRI} is the primary current calculated using the following equation:

$$I_{PRI} = \frac{P_{OUT\_MAX}}{\eta \times V_{IN}}$$

The low-side MOSFETs turn on with ZVS. If the switching frequency is close to resonant frequency, turn-on power loss associated with high-side MOSFETs can be ignored. However, the current is at peak when the MOSFET is turned off. Calculate the turn-off switching power dissipation of the MOSFET using the following equation:

$$PD_{SWITCH} = \frac{\sqrt{2} \times C_{RSS} \times V_{IN}^2 \times f_{SW} \times I_{PRI}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of the MOSFETs and I_{GATE} is the peak gate-drive sink current when the MOSFET is being turned off.

Setting the Lamp Current

The MAX8751 senses the lamp current flowing through resistor R1 (Figure 1) connected between the low-voltage terminal of the lamp and ground. The voltage across R1 is fed to IFB and is internally full-wave rectified. The MAX8751 controls the desired lamp current by regulating the average of the rectified IFB voltage. To set the RMS lamp current, determine R1 as follows:

$$R1 = \frac{\pi \times 790mV}{2\sqrt{2} \times I_{LAMP(RMS)}}$$

where $I_{LAMP(RMS)}$ is the desired RMS lamp current and 790mV is the typical value of the IFB regulation point specified in the *Electrical Characteristics* table. To set the RMS lamp current to 6mA, the value of R1 should be 148Ω. The closest standard 1% resistors are 147Ω and 150Ω. The precise shape of the lamp-current waveform depends on lamp parasitics. The resulting waveform is an imperfect sinusoid waveform, which has an RMS value that is not easy to predict. A high-frequency true RMS current meter (such as Yokogawa 2016) should be used to measure the RMS current and make final adjustments to R1. Insert this meter between the sense resistor and the lamp's low-voltage terminal to measure the actual RMS current.

Setting the Secondary Voltage Limit

The MAX8751 limits the transformer secondary voltage during startup and lamp-out faults. The secondary voltage is sensed through the capacitive voltage-divider formed by C3 and C4 (Figure 1). The voltage of VFB is proportional to the CCFL voltage. The selection of the parallel resonant capacitor C1 is described in the *Selecting the Resonant Components* section. Smaller values for C3 result in higher efficiency due to lower circulating current. If C3 is too small, the resonant operation is affected by the panel parasitic capacitance. Therefore, C3 is usually chosen to be between 10pF and 18pF. After the value of C3 is set, select C4 based on the desired maximum RMS secondary voltage $V_{LAMP(RMS)\_MAX}$:

$$C4 = \frac{\sqrt{2} \times V_{LAMP(RMS)\_MAX}}{2.32V} \times C3$$

where the 2.34V is the typical value of the VFB peak voltage when the lamp is open. To set the maximum RMS secondary voltage to 1800V with C3 selected to be 12pF, C4 must be less than or equal to 13nF.

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Setting the Secondary Current Limit

The MAX8751 limits the secondary current even if the IFB sense resistor is shorted or transformer secondary current finds its way to ground without passing through R1. ISEC monitors the voltage across the sense resistor R2 connected between the low-voltage terminal of the transformer secondary winding and ground. Determine the value of R2 using the following equation:

$$R2 = \frac{1.26V}{\sqrt{2} \times I_{SEC(RMS)\_MAX}}$$

where $I_{SEC(RMS)\_MAX}$ is the desired maximum RMS transformer secondary current during fault conditions, and 1.26V is the typical value of the ISEC peak voltage-when the secondary is shorted. To set the maximum RMS secondary current in the circuit of Figure 1 to 22mA, set R2 = 40.2Ω.

Transformer Design and Resonant Component Selection

The transformer is the most important component of the resonant tank circuit. The first step in designing the transformer is to determine the transformer turns ratio. The ratio must be high enough to support the CCFL operating voltage at the minimum supply voltage. The transformer turns ratio N can be calculated as follows:

$$N \geq \frac{V_{LAMP(RMS)}}{0.90 \times V_{IN(MIN)}}$$

where $V_{LAMP(RMS)}$ is the maximum RMS lamp voltage in normal operation, and $V_{IN(MIN)}$ is the minimum DC input voltage. If the maximum RMS lamp voltage in normal operation is 800V and the minimum DC input voltage is 7V, the turns ratio should be greater than 120 turns.

The next step to design the resonant tank for CCFL is to design the resonant frequency of the tank close to the switching frequency set by the HF resistor. The resonant frequency is determined by: the primary winding series capacitor Cs, the secondary parallel capacitor Cp, the transformer secondary leakage inductance L, and the CCFL lamp operating resistance R_L.

The simplified CCFL inverter circuit is shown in Figure 7(a). The full-bridge power stage is simplified and represented as a square-wave AC source. The resonant tank circuit can be further simplified to Figure 7(b) by removing the transformer. C_S' is the capacitance of the primary capacitive divider reflected to the secondary and N is the transformer turns ratio.

Figure 8 shows the frequency response of the resonant tank's voltage gain under different load conditions. The primary series capacitor is 1µF, the secondary parallel capacitor is 15pF, the transformer turns ratio is 1:93, and the secondary leakage inductance is 260mH. Notice that there are two peaks, f_S and f_P, in the frequency response. The first peak, f_S, is the series resonant peak determined by the secondary leakage inductance (L) and the series capacitor reflected to the secondary (Cs'):

$$f_S = \frac{1}{2\pi\sqrt{LCs'}}$$

The second peak, f_P, is the parallel resonant peak determined by the secondary leakage inductance (L), the parallel capacitor (C_P), and the series capacitance reflected to the secondary (C'_S):

$$f_P = \frac{1}{2\pi\sqrt{L\frac{Cs'C_P}{Cs' + C_P}}}$$

The actual resonant frequency is between these two resonant peaks. When the lamp is off, the operating point of the resonant tank is close to the parallel resonant peak due to the lamp's infinite impedance. The circuit displays the characteristics of a parallel-loaded resonant converter. While in parallel-loaded resonant operation, the inverter behaves like a voltage source to generate the necessary striking voltage. Theoretically, the output voltage of the resonant converter increases until the lamp is ionized or until it reaches the IC's secondary voltage limit. Once the lamp is ionized, the equivalent-load resistance decreases rapidly and the operating point moves toward the series-resonant peak. While in series-resonant operation, the inverter behaves like a current source.

The leakage inductance of the CCFL transformer is an important parameter in the resonant tank design. The leakage inductance values can have large tolerance and significant variations among different batches. It is best to work directly with transformer vendors on leakage inductance requirements. The series capacitor Cs sets the minimum operating frequency, which is approximately two times the series resonant peak frequency. The series capacitor Cs can be chosen as below:

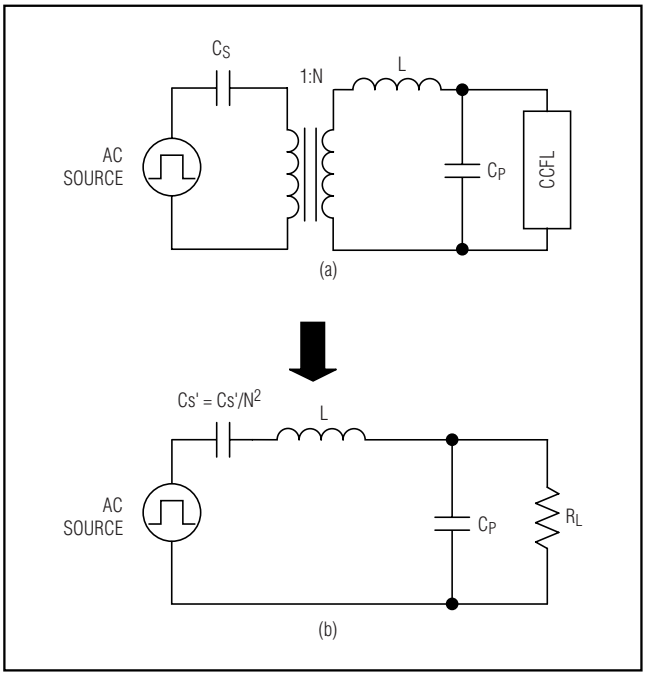


Figure 7. Simplified CCFL Inverte r Circuit

$$CS \leq \frac{N^2}{4\pi^2 \times f^2_{MIN} \times L}$$

where f_{MIN} is the minimum operating frequency range. In the circuit of Figure 1, the transformer's turns ratio is 120 and its secondary leakage inductance is 200mH. To set the minimum resonant frequency to 30kHz, use 2.2µF capacitor for C_S.

The parallel capacitor CP sets the maximum operating frequency, which is also the parallel resonant peak frequency. The capacitance CP can be chosen as below:

$$C_P > \frac{C_S}{4\pi^2 \times f^2_{MAX} \times L \times C_S - N^2}$$

In the circuit of Figure 1, to set the maximum resonant frequency to 95kHz; use 15pF for C_P.

The transformer core saturation should also be considered when selecting the operating frequency. The primary winding should have enough turns to prevent transformer saturation under all operating conditions. Use the following expression to calculate the minimum number of turns N1 of the primary winding:

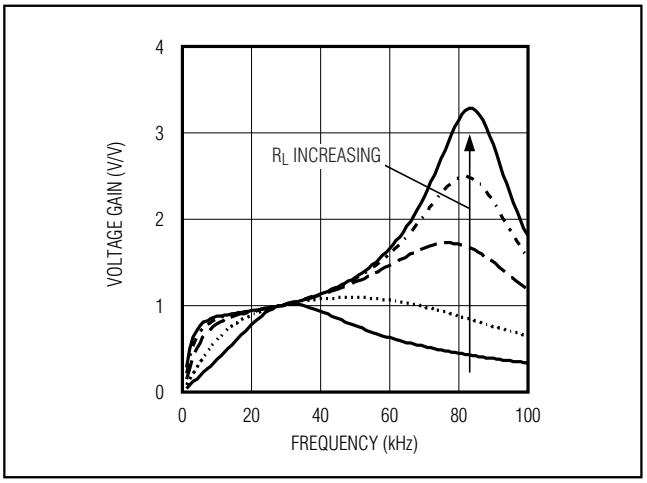


Figure 8. Frequency Response of the Resonant Tank

$$N1 > \frac{D_{MAX} \times V_{IN(MAX)}}{B_S \times S \times f_{MIN}}$$

where D_{MAX} is the maximum duty cycle (approximately 0.4) of the high-side switch, $V_{IN(MAX)}$ is the maximum DC input voltage, B_S is the saturation flux density of the core, and S is the minimal cross-section area of the core.

COMP Capacitor Selection

The COMP capacitor sets the speed of the current-regulation loop that is used during startup, maintaining lamp-current regulation, and during transients caused by changing the input voltage. To maintain stable operation, the COMP capacitor (C_{COMP}) needs to be at least 3.3nF.

As discussed in the *DPWM Dimming Control* section, the COMP capacitor also limits the dynamics of the lamp-current envelope in DPWM operation. At the end of the DPWM ON cycle, the MAX8751 turns on a 100µA internal current source to linearly discharge the COMP capacitor. Use the following equation to set the fall time:

$$C_{COMP} = \frac{100\mu A \times t_{FALL}}{V_{COMP}}$$

where t_{FALL} is the fall time of the lamp-current envelope and V_{COMP} is the dynamic COMP voltage determined by resonant tank. At the beginning of the DPWM ON cycle, the COMP capacitor is charged by transconductance error amplifier, so the charge current is not constant. Because the average charge current is around

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

30µA, the rise time is about three times longer than the fall time.

Setting the Fault Delay Time

The TFLT capacitor determines the delay time for both the open-lamp fault and secondary short-circuit fault. The MAX8751 charges the TFLT capacitor with a 1µA current source during an open-lamp fault and charges the TFLT capacitor with a 126µA current source during a secondary short-circuit fault. Therefore, the secondary short-circuit fault delay time is approximately 100 times shorter than that of the open-lamp fault. The MAX8751 sets the fault latch when the TFLT voltage reaches 4V. Use the following equations to calculate the open-lamp fault delay (T_{OPEN_LAMP}) and secondary short-circuit fault delay (T_{SEC_SHORT}):

$$T_{OPEN\_LAMP} = \frac{C_{TFLT} \times 4V}{1\mu A}$$

$$T_{SEC\_SHORT} = \frac{C_{TFLT} \times 4V}{126\mu A}$$

Bootstrap Capacitors

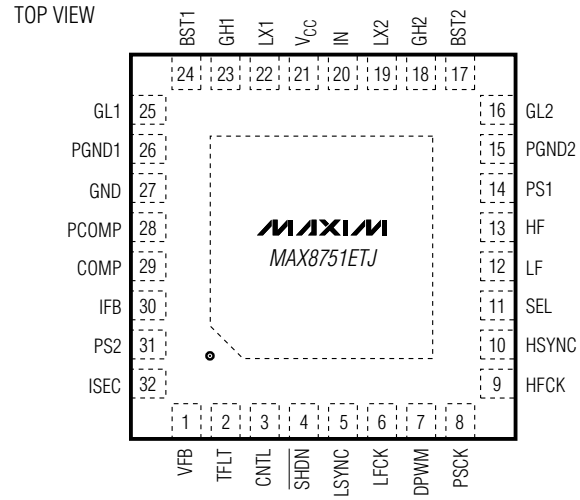
The high-side gate drivers are powered using two bootstrap circuits. The MAX8751 integrates the bootstrap diodes so only two 0.1µF bootstrap capacitors are needed. Connect the capacitors between LX1 and BST1 and between LX2 and BST2 to complete the bootstrap circuits.

Layout Guidelines

Careful PC board layout is important to achieve stable operation. The high-voltage section and the switching section of the circuit require particular attention. The high-voltage sections of the layout need to be well separated from the control circuit. Follow these guidelines for good PC board layout.

1) Keep the high-current paths short and wide, especially at the ground terminals. This is essential for stable, jitter-free operation and high efficiency.
2) Use a star-ground configuration for power and analog grounds. The power and analog grounds should be completely isolated—meeting only at the center of the star. The center should be placed at the analog ground pin (GND). Using separate copper islands for these grounds can simplify this task. Quiet analog ground is used for V_{CC}, COMP, HF, LF, and TFLT.
3) Route high-speed switching nodes away from sensitive analog areas (V_{CC}, COMP, HF, LF, and TFLT). Make all pin-strap control input connections to analog ground or V_{CC}.
4) Mount the decoupling capacitor from V_{CC} to GND as close as possible to the IC with dedicated traces that are not shared with other signal paths.
5) The current-sense paths for LX_ to GND must be made using Kelvin-sense connections to guarantee the current-limit accuracy. With 8-pin MOSFETs, this is best done by routing power to the MOSFETs from the outside using the top copper layer, while connecting GND and LX_ inside (underneath) the 8-pin SO package.
6) Ensure the feedback connections are short and direct. To the extent possible, IFB, VFB, and ISEC connections should be far away from the high-voltage traces and the transformer.
7) To the extent possible, high-voltage trace clearance on the transformer's secondary should be widely separated. The high-voltage traces should also be separated from adjacent ground planes to prevent lossy capacitive coupling.
8) The traces to the capacitive voltage-divider on the transformer's secondary need to be widely separated to prevent arcing. Moving these traces to opposite sides of the board can be beneficial in some cases.

Pin Configuration



TQFN 5mm x 5mm

Chip Information

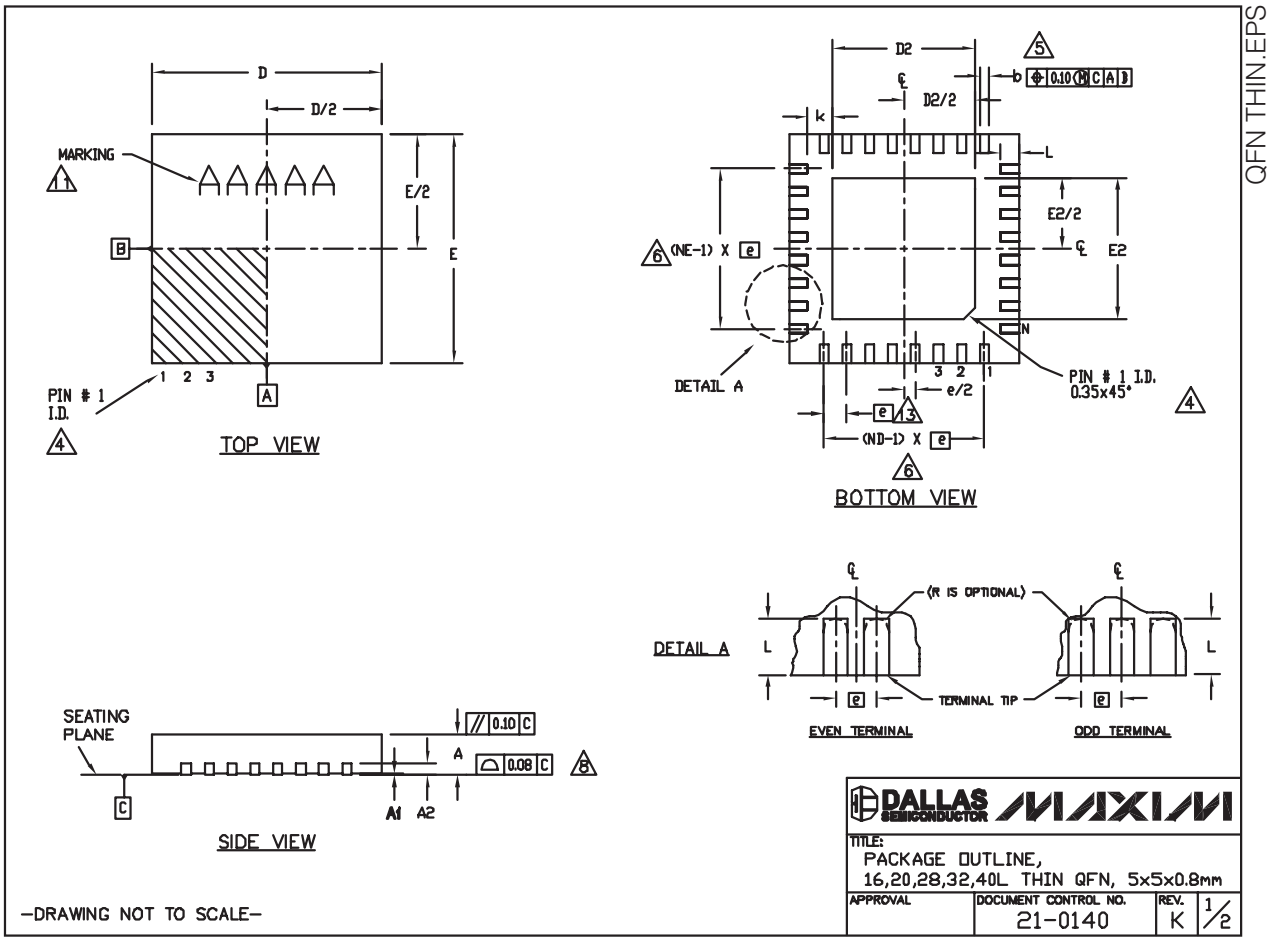
TRANSISTOR COUNT: 7743

PROCESS: BiCMOS

Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Fixed-Frequency, Full-Bridge CCFL Inverter Controller

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	K	1/2