Advanced Product Information
August 1999 *(1 of 4)*

1.85 to 1.91 GHz 3.2V, 28 dBm, PCS 50 Ohm Linear Power Module

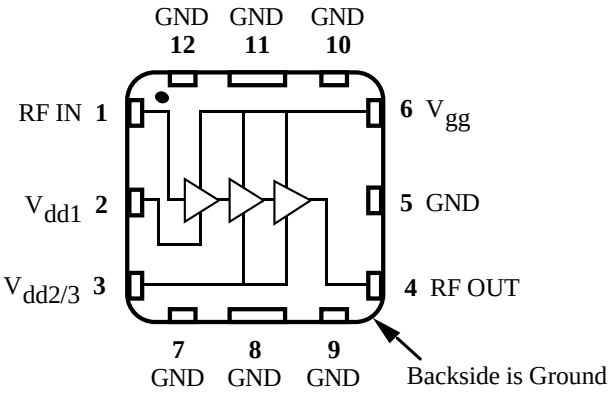
Features

- ❑ Operation as Low as 3.2V
- ❑ 35% Linear Power Added Efficiency
- ❑ +28 dBm Output Power (IS-98 CDMA Mode)
- ❑ 30 dB Gain at Operating Output Power
- ❑ Tested Under Digital Modulation
- ❑ New 50 Ohm Power Module Package
- ❑ PHEMT Material Technology
- ❑ Fixed Gate Bias

Applications

- ❑ PCS Handsets
- ❑ PCS Base Stations
- ❑ Wireless Local Loop Subscriber Units
- ❑ cdmaOne Handsets

Functional Block Diagram



Description

The CPM1530-PM is a 50 ohm, matched, linear power amplifier module intended for use in PCS handsets and wireless local loop subscriber units. The amplifier meets the requirements of PCS-1900 or IS-98 (CDMA) systems. It is a member of Celeritek's new ***True▲Triangle***™ family of 3V power amplifier modules.

The CPM1530-PM is packaged in a low-cost, space efficient, matched module that provides excellent electrical stability and low thermal resistance. The part requires no external matching and a fixed negative voltage significantly reducing space and cost and enhancing ease of use.

This device is unconditionally stable under all source and load impedances.

Absolute Maximum Ratings

Parameter	Rating	Parameter	Rating	Parameter	Rating
Drain Voltage (+V_d)	+5.5 V*	Power Dissipation	5 W	Operating Temperature	-40°C to +90°C
Drain Current (I_d)	1.8 A	Thermal Resistance	20°C/W	Channel Temperature	150°C
RF Input Power	3 dBm*	Storage Temperature	-65°C to +150°C	Soldering Temperature	260°C for 5 Sec.
DC Gate Voltage (-V_g)	-3.0 V*				

* Max (+V_d) and (-V_g) under linear operation. Max potential difference across the device at 1dB gain compression point ($2V_d$ + |-V_g|) not to exceed the minimum breakdown voltage (V_{br}) of +12V.

Recommended Operating Conditions

Parameter	Typ	Units	Parameter	Typ	Units
Drain Voltage (+V_d)	3.2 to 4.1	Volts	Operating Temperature (PC Board)	-30 to +80	°C
Gate Voltage (V_{gg}) (Fixed and regulated)	-2.5	Volts			

Application Information

The CPM1530-PM is a three stage amplifier that requires positive and negative supply voltages for proper operation. It is essential when turning on the device that the negative supply be applied before the positive supply. When turning the device off, the positive supply should be removed before the negative supply is removed.

The CPM1530-PM can be operated over a range of supply voltages and bias points. It is important that the maximum power dissipation of the package be observed at all times and that the maximum voltage across the device is not exceeded.

Circuit Design Considerations

Biasing A negative gate voltage is necessary to set the bias currents of the three FET stages in the CPM1530-PM. This is accomplished via a fixed -2.5 V to pin 6. The positive supply voltages are applied to pins 2 and 3. Bypass decoupling is provided on-board.

The recommended DC by-pass capacitance and low-pass in-line inductance are shown in the evaluation board on Page 4.

Inadequate by-pass capacitance and inductance around the DC supply lines can compromise the adjacent channel power ratio (ACPR), reduce power gain and/or create oscillations.

Supply Ramping To obtain power ramping, gate supply control is recommended.

Mode Switching If further efficiency is required at lower power levels, then an adjustment of the fixed Vgg can be made.

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Electrical Characteristics

Unless otherwise specified, the following specifications are guaranteed at room temperature with drain voltage ($+V_d$) = 3.7 V.

Parameter	Condition	Min	Typ	Max	Units
Frequency Range		1.85		1.91	GHz
Gain	@ Digital power output	28	30		dB
Gain Ripple*	1850-1910 MHz			1.5	dB
Gain Variation	Over supply voltage		2		dB/V
	Over temperature		0.03		dB/°C
Power Output	Meets IS-98 CDMA mask		+28		dBm
Harmonics	2nd @ Digital power output, no output trapping, Po=+28.0 dBm		-30		dBc
	3rd @ Digital power output, no output trapping, Po=+28.0 dBm		-40		dBc
Noise Power in Receive Band	30 kHz bandwidth		-94		dBm
Linearity (ACPR)	CDMA modulation @ +28.0 dBm Pout, 1.25 MHz offset	-45			dBc/30KHz
Spurious Signal	VSWR = 3:1 in-band, VSWR = 10:1 out-of-band			-80	dBc
Noise Figure			3.0		dB
Input Return Loss			10		dB
Efficiency (Vdd = 3.2 V)	Pout = +16.0 dBm - CDMA	5	7		%
	Pout = +28.0 dBm - CDMA	32	35		%
Positive Supply Current (I_d)	Pout IS-98 CDMA (27 dBm)		470		mA
Quiescent Current (I_q)	No RF CDMA mode		130		mA
Negative Supply Current ($-I_g$)	Includes internal resistor divider		1.1	2.0	mA
Negative Supply Voltage ($-V_{gg}$)	Fixed and regulated		-2.5		V

* Specifications guaranteed over the temperature range of -20°C to +80°C

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Modulation When biased as specified, the CPM1530-PM will achieve the required adjacent channel response for the digital PCS system specified. Celeritek tests each product under digital modulation to ensure correlation to customer applications.

Thermal

1. The ground pad on the backside of the CPM1530-PM must be soldered to the ground plane.
2. All 12 leads of the package must be soldered to the appropriate electrical connection.

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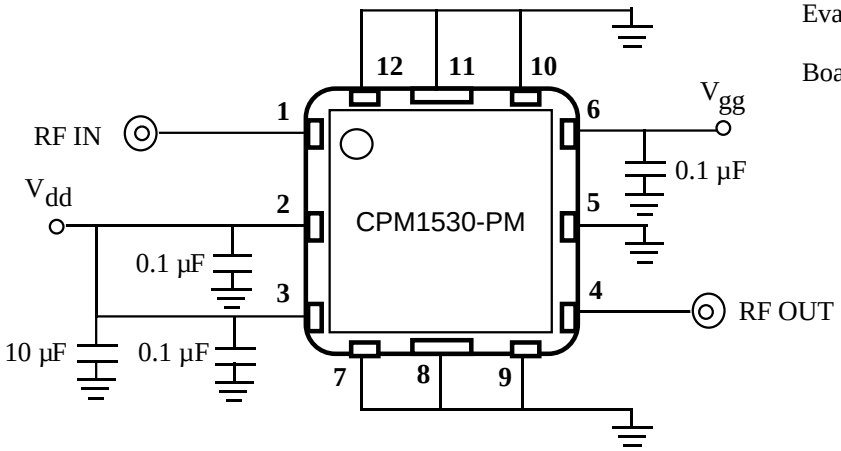
Recommended Application Circuit

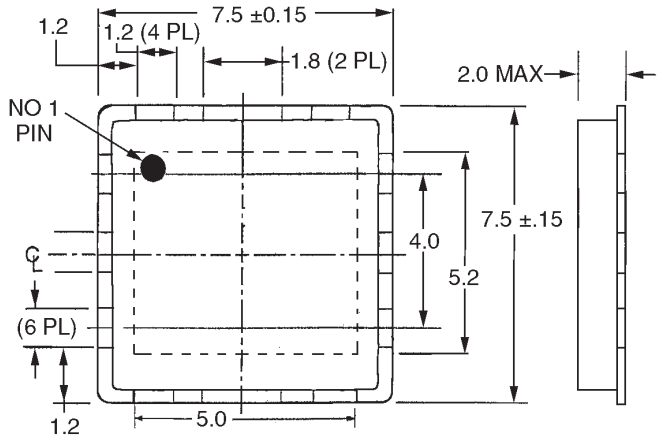
Note: This schematic represents the topology of the application circuit recommended by Celeritek.



Evaluation Board Schematic

Board substrate:
ER = 4.60
Thickness = 0.031 in.

Physical Dimensions



DIMENSIONS IN MILLIMETERS

Ordering Information

The CPM1530-PM is available in a surface mount 50 ohm matched module and devices are available in tube or tape and reel.

Part Number for Ordering	Package
CPM1530-PM-00S0	**PM-12 CDMA surface mount power package in tube**
CPM1530-PM-00ST	**PM-12 CDMA surface mount power package in tape and reel**
PB-CPM1530-PM-00S0	**Evaluation Board with SMA connectors for CPM1530-PM-00S0 tested CDMA**

Notes

CELERITEK

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