19-0796; Rev 0; 4/07

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

General Description

The MAX8664 dual-output PWM controller is a low-cost, high-performance solution for systems requiring dual power supplies. It provides two individual outputs that operate 180° out-of-phase to minimize input current ripple, and therefore, capacitance requirements. Built-in drivers are capable of driving external MOSFETs to deliver up to 25A output current from each channel. The MAX8664 operates from a 4.5V to 28V input voltage source and generates output voltages from 0.6V up to 90% of the input voltage on each channel. Total output regulation error is less than ±0.8% over load, line, and temperature.

The MAX8664 operates with a constant switching frequency adjustable from 100kHz to 1MHz. Built-in boost diodes reduce external component count. Digital soft-start eliminates input inrush current during startup. The second output has an optional external REFIN2, facilitating tracking supply applications. Each output is capable of sourcing and sinking current, making the device a great solution for DDR applications.

The MAX8664 employs Maxim's proprietary peak voltage-mode control architecture that provides superior transient response during either load or line transients. This architecture is easily stabilized using two resistors and one capacitor for any type of output capacitors. Fast transient response requires less output capacitance, consequently reducing total system cost. The MAX8664B latches off both controllers during a fault condition, while the MAX8664A allows one controller to continue to function when there is a fault in the other controller.

Applications

Desktop and Notebook PCs

Graphic Cards

ASIC/CPU/DSP Power Supplies

Set-Top Box Power Supply

Printer Power Supply

Network Power Supply

POL Power Supply

Pin Configuration appears at end of data sheet.

Features

- **±0.8% Output Accuracy Over Load and Line**
- **Operates from a Single 4.5V to 28V Supply**
- **Simple Compensation for Any Type of Output Capacitor**
- **Internal 6.5V Regulator for Gate Drive**
- **Integrated Boost Diodes**
- **Adjustable Output from 0.6V to 0.9 x V_{IN}**
- **Digital Soft-Start Reduces Inrush Current**
- **100kHz to 1MHz Adjustable Switching**
- **180° Out-of-Phase Operation Reduces Input Ripple Current**
- **Overcurrent and Overvoltage Protection**
- **External Reference Input for Second Controller**
- **Prebiased Startup Operation**

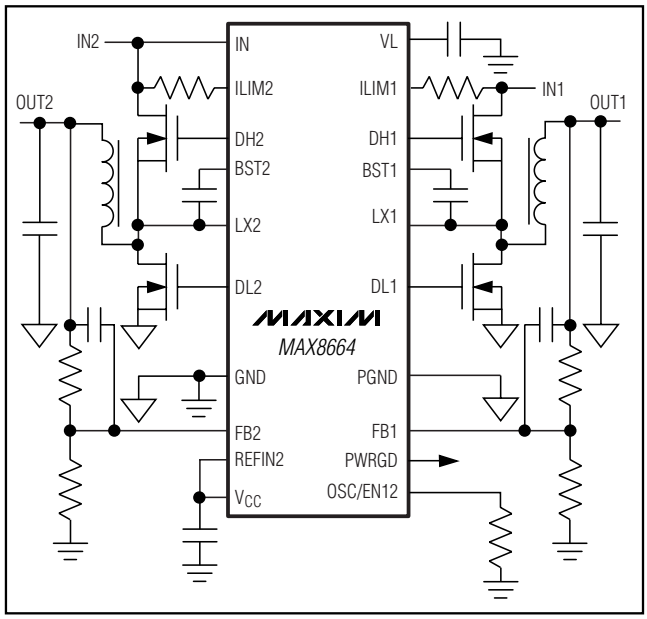
Ordering Information

PART	PIN-PACKAGE	PKG CODE	FAULT ACTION
MAX8664AEEP+	20 QSOP	E20-1	Independent
MAX8664BEEP+	20 QSOP	E20-1	Joint

Note: *This device operates over the -40°C to +85°C operating temperature range.*

+Denotes lead-free package.

Typical Operating Circuit



Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V
VL to GND.....-0.3 to +8V
IN, BST_ to VL .....-0.3V to +30V
V_{CC}, FB_, PWRGD to GND.....-0.3V to +6V
VL to V_{CC} .....-2V to +8V
PGND to GND .....-0.3V to +0.6V
DL_ to PGND.....-0.3V to (V_{VL} + 0.3V)
DH_ to PGND.....-0.3V to ($V_{BST\_}$ + 0.3V)
BST_ to GND.....-0.3V to 38V
BST_ to LX.....-0.3V to +8V
LX_ to PGND .....-1V (-2.5V for < 50ns transient) to +30V
DH_ to LX_.....-0.3V to ($V_{BST\_}$ + 0.3V)
ILIM_ to GND .....-0.3V to (V_{IN} + 0.3V)
ILIM_ to LX_.....-0.6V to +30V
OSC/EN12, REFIN2 to GND .....-0.3V to (V_{VCC} + 0.3V)
VL Continuous Current .....125mA$_{RMS}$
V_{CC} Continuous Current.....10mA$_{RMS}$
Continuous Power Dissipation (T_A = +70°C) (Note 1)
20-Pin QSOP (derate 11.0mW/°C above +70°C).....884mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package mounted on a multilayer PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, $R_{OSC/EN12}$ to GND = 56.1kΩ, REFIN2 = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES						
IN Supply Voltage			7.2		28.0	V
	IN = VL = V_{CC}		4.5		5.5	
VL Output Voltage	7.2V < V_{IN} < 28V, 0 < I_{VL} < 60mA		6.10	6.6	6.75	V
V_{CC} Output Voltage	7.2V < V_{IN} < 28V, 0 < I_{CC} < 5mA		4.5	5.0	5.5	V
V_{CC} Undervoltage Lockout (UVLO)	Rising		3.4	3.5	3.6	V
	Hysteresis			350		mV
Standby Supply Current	OSC/EN12 not connected	V_{IN} = 12V, I_{IN}		0.095	0.2	mA
		V_{CC} = V_{IN} = V_{VL} = 5V, I_{IN} + I_{VL} + I_{VCC}		0.08	0.2	
Operating Supply Current	No switching, $V_{FB\_}$ = 0.65V	V_{IN} = 12V, I_{IN}		1.4	2.5	mA
		V_{CC} = V_{IN} = V_{VL} = 5V, I_{IN} + I_{VL}+ I_{VCC}		1.1	1.8	
REGULATOR SPECIFICATIONS						
Reference Accuracy	T_A = 0°C to +85°C		0.5955	0.600	0.6045	V
	T_A = -40°C to +85°C		0.5930	0.600	0.6070	
FB_ Regulation Accuracy	V_{REFIN2} = V_{VCC}	T_A = 0°C to +85°C	0.5952	0.600	0.6048	V
		T_A = -40°C to +85°C	0.5925	0.600	0.6075	
	V_{REFIN2} = 1.000V		0.995	1.000	1.005	
REFIN2 to Internal Reference Switchover Threshold	Not to be switched during operation		2	V_{VCC} - 0.7	V_{VCC} - 0.3	V
REFIN2 Maximum Program Voltage				1.3		V
REFIN2 Disable Threshold				50		mV
FB Input Bias Current	V_{FB} = 0.5V			3		nA
REFIN2 Bias Current	V_{REFIN2} = 0.65V			3		nA
FB Propagation Delay	FB rising to DH falling			90		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, $R_{OSC/EN12}$ to GND = 56.1kΩ, REFIN2 = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PROTECTION FEATURES						
Overvoltage Protection (OVP) Threshold	V_{FB1} rising			0.75		V
	V_{FB2} rising, $V_{REFIN2} \le 1.3V$			REFIN2 + 0.15		
Power-Good (PWRGD) Threshold	V_{REFIN2} = V_{VCC}, $V_{FB\_}$ rising, MAX8664B		0.500	0.525	0.550	V
	V_{FB1} rising, MAX8664A					
	Hysteresis			5		%
High-Side Current-Sense Program Current (Note 3)	T_A = +85°C			60		µA
	T_A = +25°C		44	50	60	
ILIM Leakage	T_A = +25°C			0.1	1.0	µA
	T_A = +85°C			0.1		
High-Side Current-Sense Overcurrent Trip Adjustment Range			0.05		0.40	V
Internal Soft-Start Time	$R_{OSC/EN12}$ = 56.1kΩ, 400kHz			2.5		ms
REFIN2 Internal Pulldown Resistance	Engaged momentarily at startup			10	20	Ω
Thermal-Shutdown Threshold	Junction temperature			+160		°C
DRIVER SPECIFICATIONS						
DH_ Driver Resistance	Sourcing current, I_{DH} = -50mA	V_{VL} = 6.5V		1.35	2.1	Ω
		V_{IN} = V_{VL} = V_{VCC} = 5V		1.55		
	Sinking current, I_{DH} = 50mA	V_{VL} = 6.5V		0.9	1.4	
		V_{IN} = V_{VL} = V_{VCC} = 5V		1.0		
DL_ Driver Resistance	Sourcing current, I_{DL} = -50mA	V_{VL} = 6.5V		1.3	2	Ω
		V_{IN} = V_{VL} = V_{VCC} = 5V		1.5		
	Sinking current, I_{DL} = 50mA	V_{VL} = 6.5V		0.6	1.1	
		V_{IN} = V_{VL} = V_{VCC} = 5V		0.7		
Dead Time for Low-Side to High-Side Transition	DL_ falling to DH_ rising	V_{VL} = 6.5V	13	25	43	ns
		V_{VL} = 5V		28		
DH_ Minimum On-Time			70	108	149	ns
BST Current	V_{BST} - V_{LX} = 7V, V_{LX} = 28V, $V_{FB\_}$ = 0.55V			1.25	2.3	mA
	OSC/EN12 not connected			0.001		µA
Internal Boost Switch Resistance				6		Ω
PWM CLOCK OSCILLATOR						
PWM Clock-Frequency Accuracy			-15		+15	%
PWM Clock-Frequency Adjustment Range	$R_{OSC/EN12}$ = 226kΩ to 22.6kΩ		100		1000	kHz
OSC/EN12 Disable Current				1.5	2.5	µA

Note 2: Specifications at -40°C are guaranteed by design and not production tested.
Note 3: This current linearly compensates for the MOSFET temperature coefficient.

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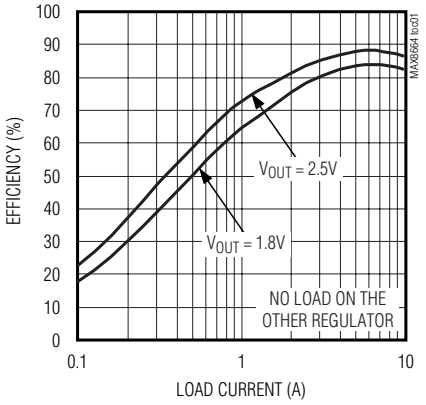
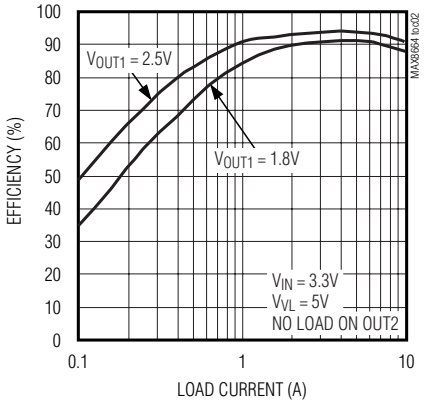
Typical Operating Characteristics

(Circuit of Figure 2, 600kHz, V_{IN} = 12V, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, T_A = +25°C, unless otherwise noted.)

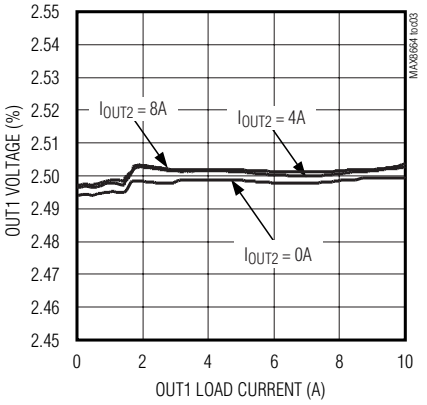
EFFICIENCY vs. LOAD CURRENT (600kHz, FIGURE 2)



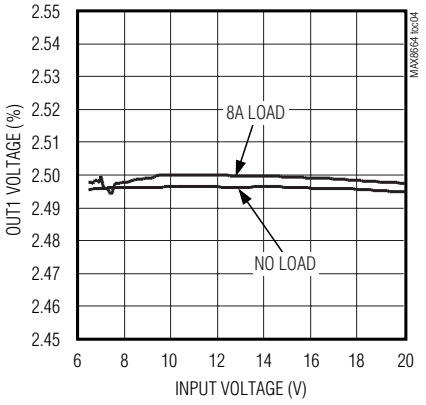
EFFICIENCY vs. LOAD CURRENT (1MHz, FIGURE 4)



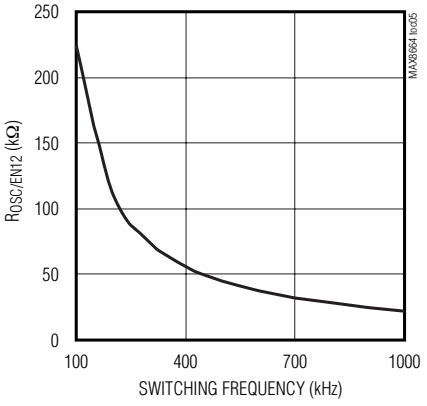
LOAD REGULATION (600kHz, FIGURE 2)



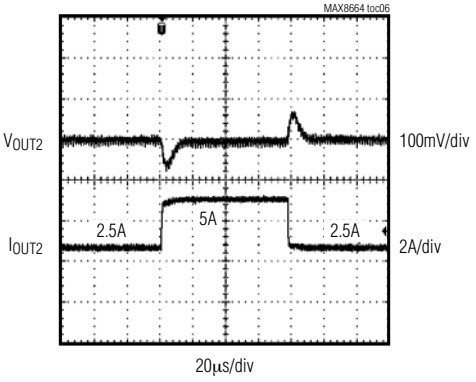
LINE REGULATION (600kHz, FIGURE 2)



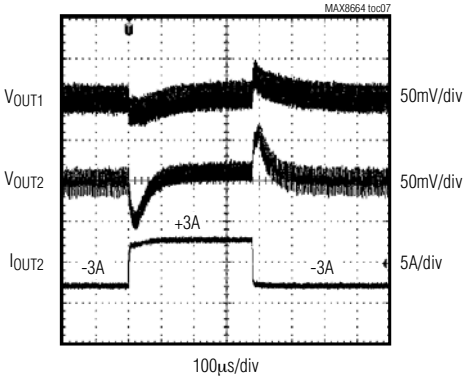
ROSC/EN12 vs. SWITCHING FRQUENCY



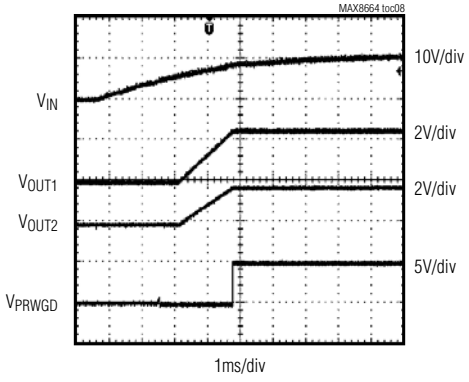
OUT1 LOAD TRANSIENT (FIGURE 2)



LOAD TRANSIENT -3A TO +3A TO -3A (FIGURE 3)



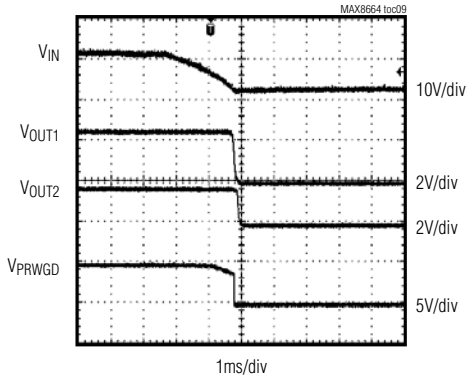
POWER-UP WAVEFORMS



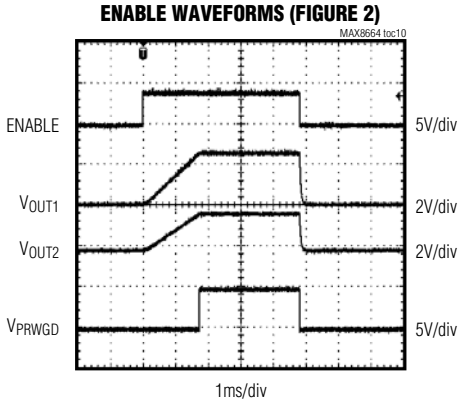
Typical Operating Characteristics (continued)

(Circuit of Figure 2, 600kHz, V_{IN} = 12V, V_{OUT1} = 2.5V, V_{OUT2} = 1.8V, T_A = +25°C, unless otherwise noted.)

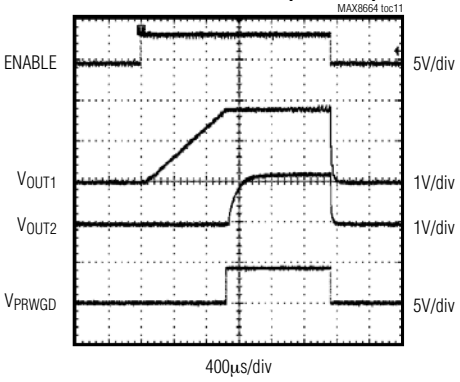
POWER-DOWN WAVEFORMS



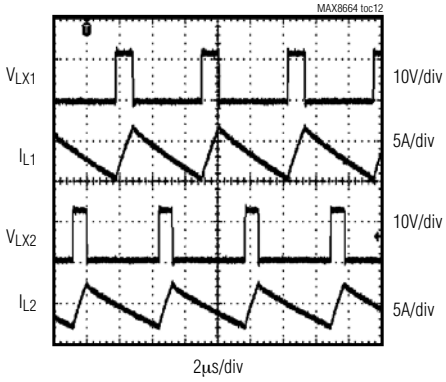
ENABLE WAVEFORMS (FIGURE 2)



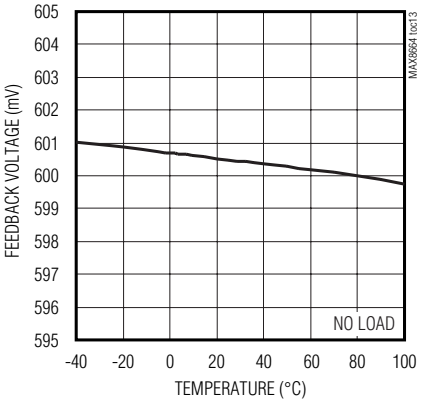
ENABLE WAVEFORMS (FIGURE 4)



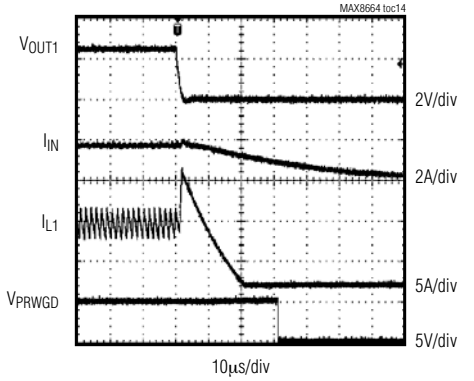
SWITCHING WAVEFORMS



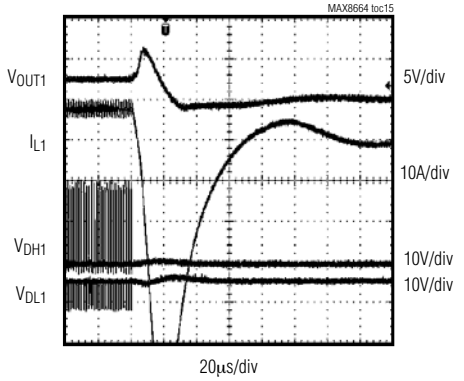
FEEDBACK VOLTAGE vs. TEMPERATURE



SHORT-CIRCUIT WAVEFORMS



OVERVOLTAGE PROTECTION



Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

Pin Description

PIN	NAME	FUNCTION
1	DH1	High-Side MOSFET Driver Output for Controller 1. Connect DH1 to the gate of the high-side MOSFET. DH1 is low in shutdown and UVLO.
2	LX1	External Inductor Connection for Controller 1. Connect LX1 to the switching node of the MOSFETs and inductor. Make sure LX1 is close to the source of the high-side MOSFET(s) to form a Kelvin connection for high-side current sensing. LX1 is high impedance during monotonic startup and shutdown.
3	BST1	Boost Capacitor Connection for the High-Side MOSFET Driver for Controller 1. Connect a 0.22µF ceramic capacitor from BST1 to LX1.
4	DL1	Low-Side MOSFET Driver Output for Controller 1. Connect DL1 to the gate of the low-side MOSFET(s) for controller 1. DL1 is low in shutdown and UVLO.
5	VL	Low-Side Gate Drive Supply and Output of the 6.5V Linear Regulator. Connect a 4.7µF ceramic capacitor from VL to PGND. When using a 4.5V to 5.5V supply, connect VL to IN. VL is the input to the V_{CC} supply. Do not load VL when IC is disabled.
6	PGND	Power Ground. Connect to the power ground plane. Connect power and analog grounds at a single point near the output capacitor's ground.
7	DL2	Low-Side MOSFET Driver Output for Controller 2. Connect DL2 to the gate of the low-side MOSFET(s) for controller 2. DL2 is low in shutdown and UVLO.
8	BST2	Boost Capacitor Connection for the High-Side MOSFET Driver for Controller 2. Connect a 0.22µF ceramic capacitor from BST2 to LX2.
9	LX2	External Inductor Connection for Controller 2. Connect LX2 to the switching node of the MOSFETs and inductor. Make sure LX2 is close to the source of the high-side MOSFET(s) to form a Kelvin connection for high-side current sensing. LX2 is high impedance during monotonic startup and shutdown.
10	DH2	High-Side MOSFET Driver Output for Controller 2. Connect DH2 to the gate of the high-side MOSFET(s) for controller 2. DH2 is low in shutdown and UVLO.
11	ILIM2	Current-Limit Set for Controller 2. Connect a resistor from the drain of the high-side MOSFET(s) to ILIM2. See the *Setting the Overcurrent Threshold* section.
12	FB2	Feedback Input for Controller 2. Connect FB2 to the center of a resistor-divider connected between the output of controller 2 and GND to set the desired output voltage. V_{FB2} regulates to V_{REFIN2} or the internal 0.6V reference. To use the internal reference, connect REFIN2 to V_{CC}.
13	REFIN2	External Reference Input for Controller 2. To use the internal 0.6V reference, connect REFIN2 to V_{CC}. To use an external reference, connect REFIN2 through a resistor (> 1kΩ) to a reference voltage between 0V and 1.3V. An RC lowpass filter is recommended when using an external reference and soft-start is not provided by the external reference. For tracking applications, connect REFIN2 to the center of a resistor voltage-divider between the output of controller 1 and GND (see Figure 3). Connect REFIN2 to GND to disable controller 2.
14	OSC/EN12	Switching Frequency Set Input. Connect a 22.6kΩ to 226kΩ resistor from OSC/EN12 to GND to set the switching frequency between 1000kHz and 100kHz. Connect a switch in series with this resistor for enable/shutdown control. When the switch is open, the IC enters low-power shutdown mode. In shutdown, OSC/EN12 is internally driven to approximately 800mV.
15	IN	Internal 6.5V Linear Regulator Input. Connect IN to a 7.2V to 28V supply, and connect a 0.47µF or larger ceramic capacitor from IN to PGND. When using a 4.5V to 5.5V supply, connect IN to VL.
16	GND	Analog Ground. Connect to the analog ground plane. Connect the analog and power ground planes at a single point near the output capacitor's ground.

Pin Description (continued)

PIN	NAME	FUNCTION
17	V_{CC}	Internal Analog Supply. V_{CC} regulates to 1.5V below V_{VL}. Connect a 1µF ceramic capacitor from V_{CC} to GND. When using a 4.5V to 5.5V supply, connect a 10Ω resistor from V_{CC} to IN. V_{CC} is used to power the IC's internal circuitry.
18	PWRGD	Open-Drain Power-Good Output. PWRGD is high impedance when controllers 1 and 2 (using the internal reference) are in regulation. PWRGD is low if the outputs are out of regulation, if there is a fault condition, or if the IC is shut down. PWRGD does not reflect the status of output 2 in the MAX8664A or when REFIN2 is connected to an external reference in the MAX8664B.
19	FB1	Feedback Input for Controller 1. Connect FB1 to the center of a resistor-divider connected between the output of controller 1 and GND to set the desired output voltage. V_{FB1} regulates to 0.6V.
20	ILIM1	Current-Limit Set for Controller 1. Connect a resistor from the drain of the high-side MOSFET(s) to ILIM1. See the *Setting the Overcurrent Threshold* section.

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

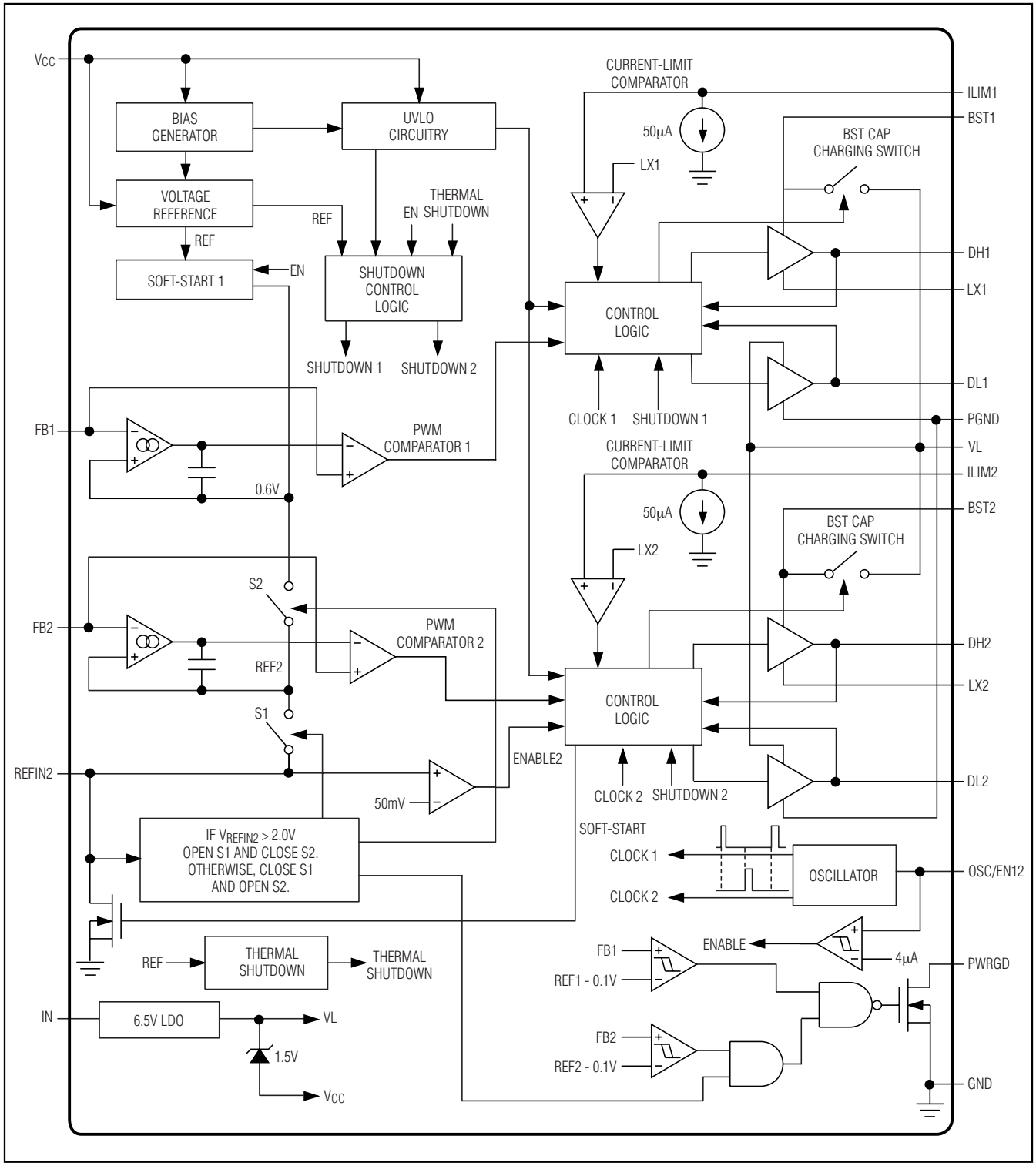


Figure 1. Functional Diagram

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

Detailed Description

The MAX8664 dual-output PWM controller is a low-cost solution for dual power-supply systems. It provides two individual outputs that operate 180° out-of-phase to minimize input capacitance requirements. Built-in drivers are capable of driving external MOSFETs to deliver up to 25A of current from each output. The MAX8664 operates from a 4.5V to a 5.5V or a 7.2V to 28V input and generates output voltages from 0.6V up to 90% of the input voltage on each channel. Total output error is less than ±0.8% over load, line, and temperature.

The MAX8664 operates with a constant switching frequency adjustable from 100kHz to 1MHz. Built-in boost diodes reduce external component count. Digital soft-start eliminates input inrush current during startup. The second output has an optional REFIN2 input that takes an external reference voltage, facilitating tracking supply applications. Each output is capable of sourcing and sinking current. Internal 6.5V and 5V linear regulators provide power for gate drive and internal IC functions. The MAX8664 has built-in protection against output overvoltage, overcurrent, and thermal faults. The MAX8664B latches off both controllers during a fault condition, while the MAX8664A allows one controller to continue to function when there is a fault in the other controller.

The MAX8664 employs Maxim's proprietary peak-voltage mode control architecture that provides superior transient response during either load or line transients. This architecture is easily stabilized using two resistors and one capacitor for any type of output capacitors. Fast transient response requires less output capacitance, consequently reducing total system cost.

DC-DC Controller Architecture

The peak-voltage mode PWM control scheme ensures stable operation, simple compensation for any output capacitor, and fast transient response. An on-chip integrator removes any DC error due to the ripple voltage. This control scheme is simple: when the output voltage falls below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch at the rising edge of the following clock cycle. This switch remains on until the minimum on-time expires and the output voltage is in regulation or the current-limit threshold is exceeded. At this point, the low-side synchronous rectifier turns on and remains on until the rising edge of the first clock cycle after the output voltage falls below the regulation threshold.

Internal Linear Regulators

The internal VL low-dropout linear regulator of the MAX8664A and MAX8664B provides the 6.5V supply used for the gate drive. Connect a 4.7µF ceramic capacitor from VL to PGND. When using a 4.5V to 5.5V input supply, connect VL directly to IN.

The 5V supply used to power IC functions (V_{CC}) is generated by an internal 1.5V shunt regulator from VL. Connect a 2.2µF ceramic capacitor from V_{CC} to GND. When using a 4.5V to 5.5V input supply, connect V_{CC} to IN through a 10Ω resistor.

High-Side Gate-Drive Supply (BST_)

The gate-drive voltage for the high-side MOSFETs is generated using a flying capacitor boost circuit. The capacitor between BST_ and LX_ is charged to the VL voltage through the integrated BST_ diode during the low-side MOSFET on-time. When the low-side MOSFET is switched off, the BST_ voltage is shifted above the LX_ voltage to provide the necessary turn-on voltage (V_{GS}) for the high-side MOSFET. The controller closes a switch between BST_ and DH_ to turn the high-side MOSFET on.

Voltage Reference

An internal 0.6V reference sets the feedback regulation voltage. Controller 1 always uses the internal reference. An external reference input is provided for controller 2. To use the external reference, connect a 0 to 1.3V supply to REFIN2. This facilitates tracking applications. To use the internal 0.6V reference for controller 2, connect REFIN2 to V_{CC}.

Undervoltage Lockout (UVLO)

When the V_{CC} supply voltage drops below the UVLO threshold (3.15V falling typ), the undervoltage lockout (UVLO) circuitry inhibits the switching of both controllers, and forces the DL and DH gate drivers low. When V_{CC} rises above the UVLO threshold (3.5V rising typ), the controllers begin the startup sequence and resume normal operation.

Output Overcurrent Protection

When the MAX8664 detects an overcurrent condition, DH is immediately pulled low. If the overcurrent condition persists for four consecutive cycles, the controller latches off and both DH_ and DL_ are pulled low. During soft-start, when FB_ is less than 300mV, the controller latches off on the first overcurrent condition. The protection circuit detects an overcurrent condition by sensing the drain-source voltage across the high-side MOSFET(s).

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

The threshold that trips overcurrent protection is set by a resistor connected from ILIM_ to the drain of the high-side MOSFET(s). ILIM_ sinks 50µA (typ) through this resistor. When the drain-source voltage exceeds the voltage drop across this resistor during the high-side MOSFET(s) on-time, an overcurrent fault is triggered. To prevent glitches from falsely tripping the overcurrent protection, connect a filter capacitor (0.01µF typically) in parallel with the overcurrent-setting resistor.

Output Overvoltage Protection (OVP)

During an overvoltage event on one or both of its outputs, the MAX8664 latches off the controller. This occurs when the feedback voltage exceeds its normal regulation voltage by 150mV for 10µs. In this state, the low-side MOSFET(s) are on and the high-side MOSFET(s) are off to discharge the output. To clear the latch, cycle EN or the input power.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8664. When the junction temperature exceeds +160°C, an internal thermal sensor shuts down the device, pulling DH_ and DL_ low for both controllers. To restart the controller, cycle EN or input power.

Power-Good Output (PWRGD)

PWRGD is an open-drain output that is pulled low when the output voltage rises above the PWRGD upper threshold or falls below the PWRGD falling threshold. PWRGD is held low in shutdown, when V_{CC} is below the UVLO threshold, during soft-start, and during fault conditions. PWRGD does not reflect the status of controller 2 in the MAX8664A, or when REFIN2 is connected to an external reference with either version. See Table 1 for PWRGD operation of the circuits of Figures 2–5 during fault conditions. For logic-level output voltages, connect an external pullup resistor between PWRGD and the logic power supply. A 100kΩ resistor works well in most applications.

Fault-Shutdown Modes

When an overvoltage or overcurrent fault occurs on one controller of the MAX8664A, the second controller continues to operate. With the MAX8664B, a fault in one controller latches off both controllers automatically, and PWRGD is pulled low. See Table 1 for the fault-shutdown modes of the circuits shown in Figures 2–5.

Table 1. Fault Shutdown Modes for Circuits of Figures 2–5

CIRCUIT	MAX8664A (INDEPENDENT)		MAX8664B (JOINT)	
	CONTROLLER 1 FAULT	CONTROLLER 2 FAULT	CONTROLLER 1 FAULT	CONTROLLER 2 FAULT
Figure 2, Figure 5 (Independent)	Controller 2 remains on. PWRGD is pulled low.	Controller 1 remains on. PWRGD remains high.	Controller 2 is shut down. PWRGD is pulled low.	Controller 1 is shut down. PWRGD is pulled low.
Figure 3 (Tracking)	Controller 2 shuts down. PWRGD is pulled low.	Controller 1 remains on. PWRGD remains high.	Controller 2 is shut down. PWRGD is pulled low.	Controller 1 is shut down. PWRGD is pulled low.
Figure 4 (Sequenced)	Controller 2 shuts down. PWRGD is pulled low.	Controller 1 remains on. PWRGD remains high.	Controller 2 is shut down. PWRGD is pulled low.	Controller 1 is shut down. PWRGD is pulled low.

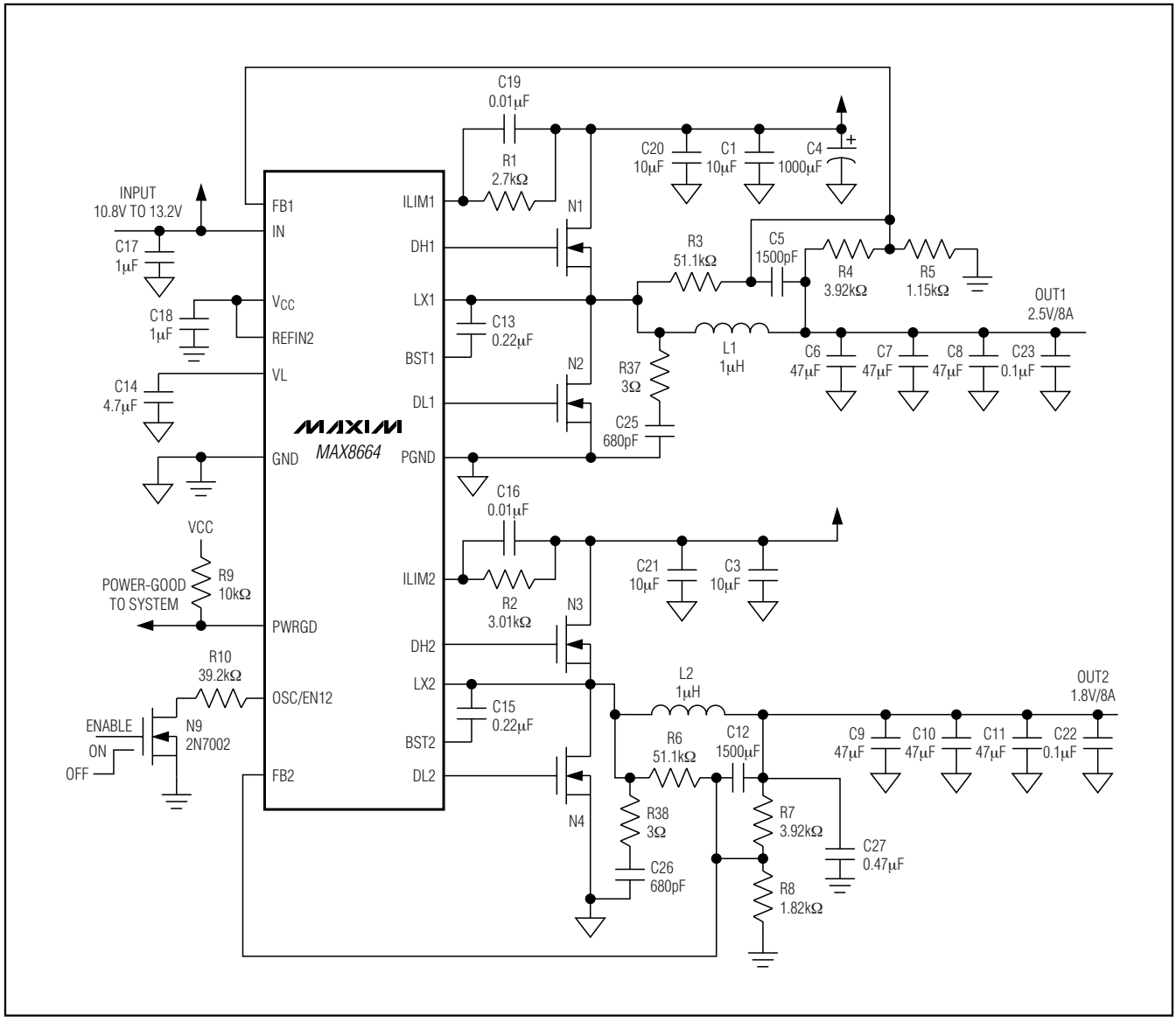


Figure 2. Low-Cost, 600kHz Typical Application Circuit

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

Table 2. Component List for Figure 2

DESIGNATION	QTY	DESCRIPTION
C1, C3, C20, C21	4	10µF ±20%, 16V X5R ceramic capacitors (1206)
C4	1	1000µF ±20%, 16V electrolytic capacitor (8mm diameter, 20mm height)
C5, C12	2	1500pF, 50V C0G ceramic capacitors (0603)
C6–C11	6	47µF ±20%, 6.3V X5R ceramic capacitors (1206)
C13, C15	2	0.22µF ±10%, 25V X7R ceramic capacitors (0603)
C14	1	4.7µF ±10%, 6.3V X5R ceramic capacitor (0805)
C16, C19	2	0.01µF ±10%, 50V X7R ceramic capacitors (0603)
C17	1	1µF ±20%, 16V X5R ceramic capacitor (0603)
C18	1	1µF ±20%, 6.3V X5R ceramic capacitor (0603)
C22, C23	2	0.1µF ±20%, 16V X7R ceramic capacitors (0603)
C25, C26	2	680pF, 50V C0G ceramic capacitors (0603)
C27	1	0.47µF ±10%, 16V ceramic capacitor (0603)
L1, L2	2	1µH inductors TOKO FDV0630-1R0M
N1–N4	4	n-channel MOSFETs (8-pin SO) International Rectifier IRF7821
N9	1	n-channel MOSFET (SOT23) Central 2N7002
R1	1	2.74kΩ ±1% resistor (0603)
R2	1	301kΩ ±1% resistor (0603)
R3, R6	2	51.1kΩ ±1% resistors (0603)
R4, R7	2	3.92kΩ ±1% resistors (0603)
R5	1	1.15kΩ ±1% resistor (0603)
R8	1	1.82kΩ ±1% resistor (0603)
R9	1	10kΩ ±5% resistor (0603)
R10	1	39.2kΩ ±1% resistor (0603)
R37, R38	2	3Ω ±5% resistors (0805)
U1	1	MAX8664 (20-pin QSOP)

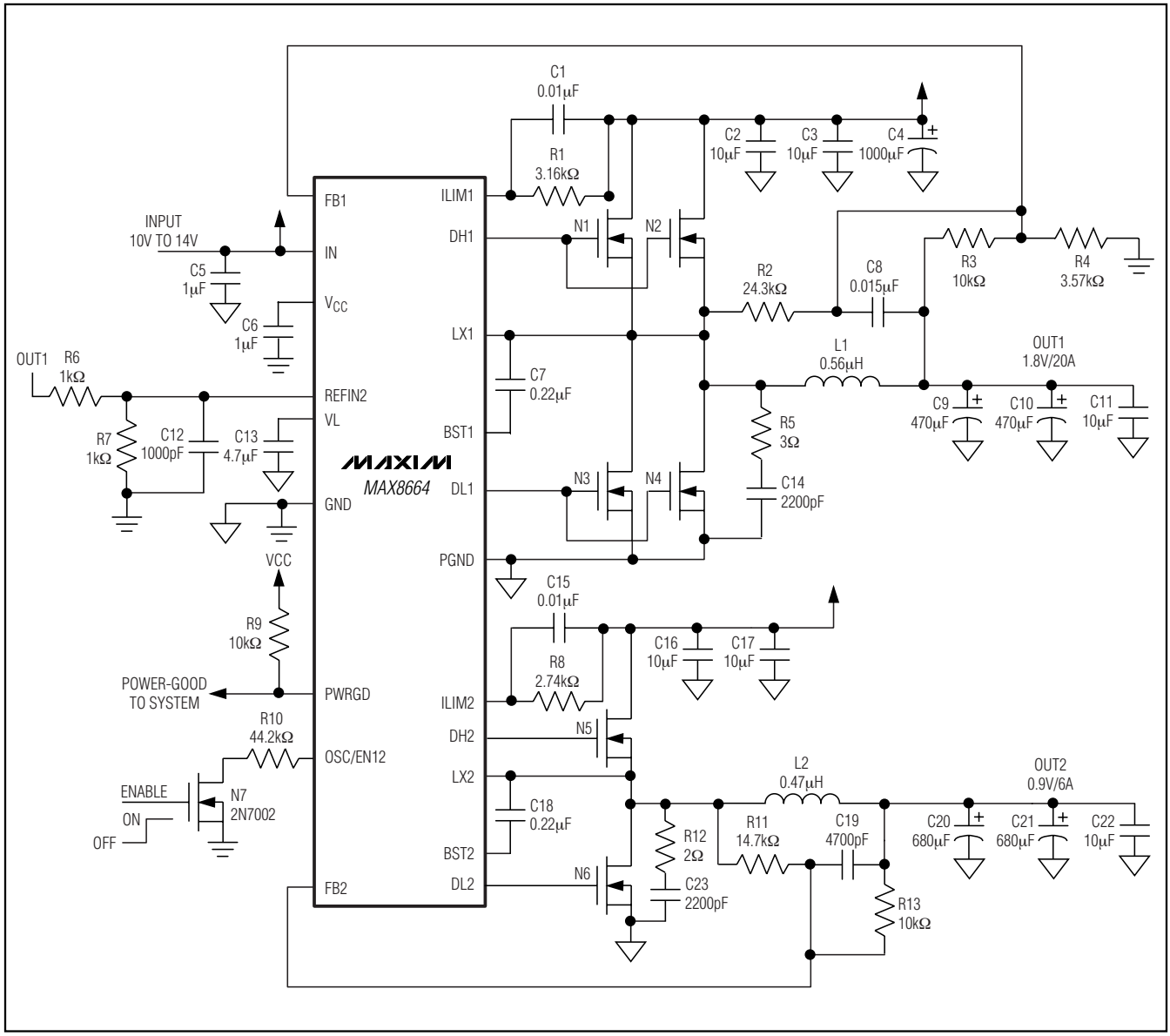


Figure 3. 500kHz Tracking Circuit for DDR2 Applications

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

Table 3. Component List for Figure 3

DESIGNATION	QTY	DESCRIPTION
C1, C15	2	0.01µF, 10V X7R ceramic capacitors
C2, C3, C16, C17	4	10µF, 16V X5R ceramic capacitors
C4	1	1000µF/16V aluminum electrolytic capacitor Rubycon 16MBZ1000M
C5	1	1µF, 16V X5R ceramic capacitor
C6	1	1µF, 10V X5R ceramic capacitor
C7, C18	2	0.22µF, 10V X7R ceramic capacitors
C8	1	0.015µF, 10V X7R ceramic capacitor
C9, C10	2	470µF, 2.5V POS capacitors Sanyo 2R5TPD470M6
C11, C22	2	10µF, 6.3V X5R ceramic capacitors
C12	1	1000pF, 10V X7R ceramic capacitor
C13	1	4.7µF, 10V X5R ceramic capacitor
C14, C23	2	2200pF, 25V X7R capacitors
C19	1	4700pF, 10V X7R capacitor
C20, C21	2	680µF, 2.5V POS capacitors Sanyo 2R5TPD680M6
L1	1	0.56µH, 4.6mΩ inductor Panasonic ETQP4LR56WFL
L2	1	0.47µH, 1.2mΩ inductor TOKO FDV0603-R47M
N1, N2	2	n-channel MOSFETs IRLR7821 (D-Pak)
N3, N4	2	n-channel MOSFETs IRLR3907Z (D-Pak)
N5	1	n-channel MOSFET IRF7807Z (8-pin SO)
N6	1	n-channel MOSFET IRF7821 (8-pin SO)
N7	1	n-channel MOSFET 2N7002 (SOT23)
R1	1	3.16kΩ ±1% resistor (0402 or 0603)
R2	1	24.3kΩ ±1% resistor (0402 or 0603)
R3, R13	2	10kΩ ±1% resistors (0402 or 0603)
R4	1	3.57kΩ ±5% resistor (0402 or 0603)
R5	1	3.0Ω ±5% resistor (0603)
R6, R7	2	1kΩ ±1% resistors (0402 or 0603)
R8	1	2.74kΩ ±1% resistor (0402 or 0603)
R9	1	10kΩ ±5% resistor (0402 or 0603)
R10	1	44.2kΩ ±1% resistor (0402 or 0603)
R11	1	14.7kΩ ±1% resistor (0402 or 0603)
R12	1	2.0Ω ±5% resistor (0402 or 0603)

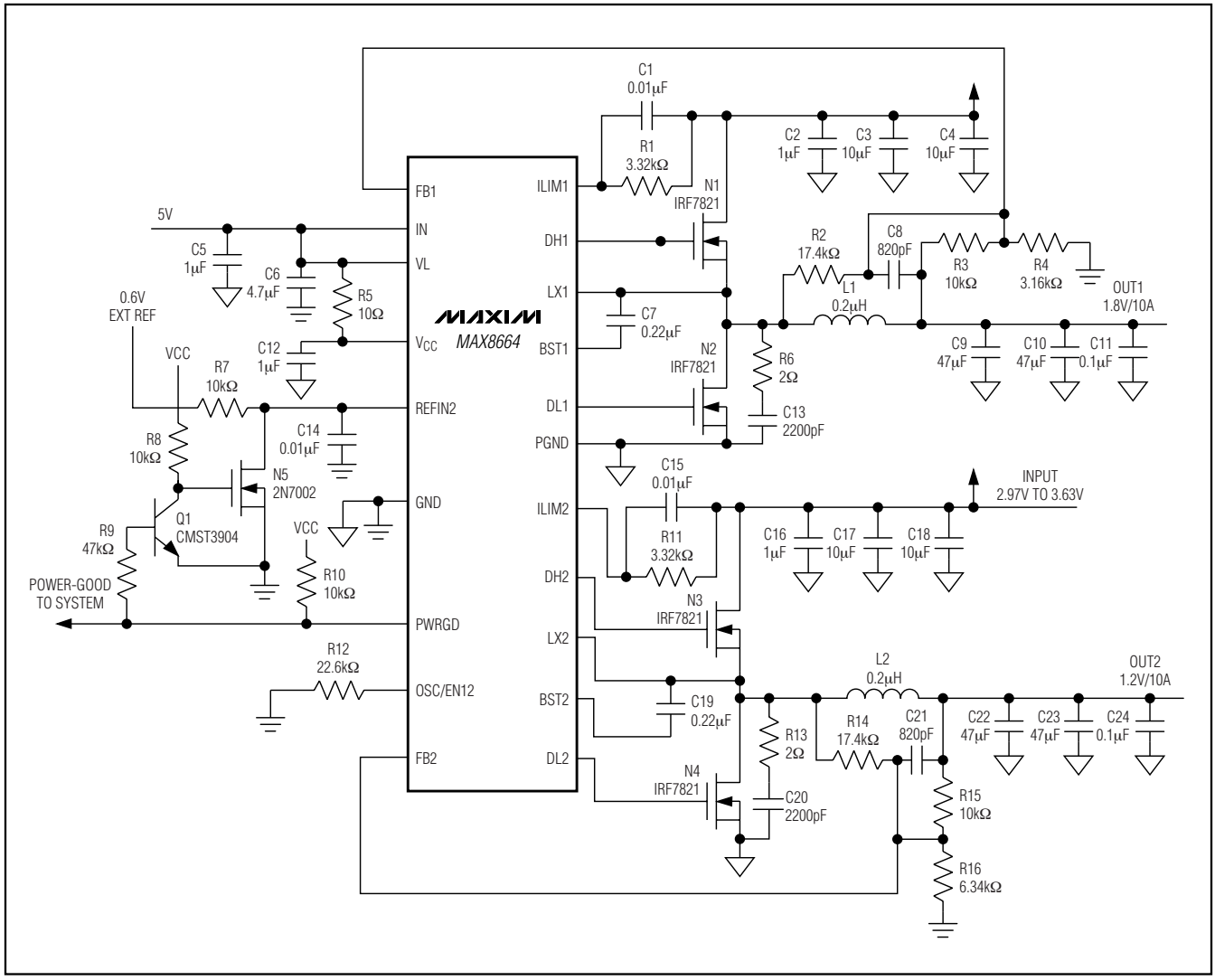


Figure 4. 1MHz Application Circuit with All Ceramic Capacitors and Sequenced Outputs

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Table 4. Component List for Figure 4

DESIGNATION	QTY	DESCRIPTION
C1, C14, C15	2	0.01µF, 10V X7R ceramic capacitors
C2, C16	2	1µF, 6.3V X5R ceramic capacitors
C3, C4, C17, C18	4	10µF, 6.3V X5R ceramic capacitors
C5, C12	2	1µF, 10V X5R ceramic capacitors
C6	1	4.7µF, 10V X5R ceramic capacitor
C7, C19	2	0.22µF, 10V X7R ceramic capacitors
C8, C21	2	820pF,10V X7R ceramic capacitors
C9, C10, C22, C23	4	47µF, 6.3V X5R ceramic capacitors
C11, C24	2	0.1µF, 10V X7R ceramic capacitors
C13, C20	2	2200pF, 25V X7R ceramic capacitors

DESIGNATION	QTY	DESCRIPTION
L1, L2	2	0.2µH, 2.4mΩ inductors TOKO FDV0603-R20M
N1–N4	4	n-channel MOSFETs IRF7821 (8-pin SO)
N5	1	n-channel MOSFET 2N7002 (SOT23)
Q1	1	Transistor, bipolar, npn Central CMST3904
R1, R11	2	3.32kΩ ±1% resistors (0402 or 0603)
R2, R14	2	17.4kΩ ±1% resistors (0402 or 0603)
R3, R15	2	10kΩ ±1% resistors (0402 or 0603)
R4	1	3.16kΩ ±1% resistor (0402 or 0603)
R5	1	10.0Ω ±5% resistor (0402 or 0603)
R6, R13	2	2.0Ω ±5% resistors (0603)
R7, R8, R10	3	10kΩ ±5% resistors (0402 or 0603)
R9	1	47kΩ ±5% resistor (0402 or 0603)
R12	1	22.6kΩ ±1% resistor (0402 or 0603)
R16	1	6.34kΩ ±1% resistor (0402 or 0603)

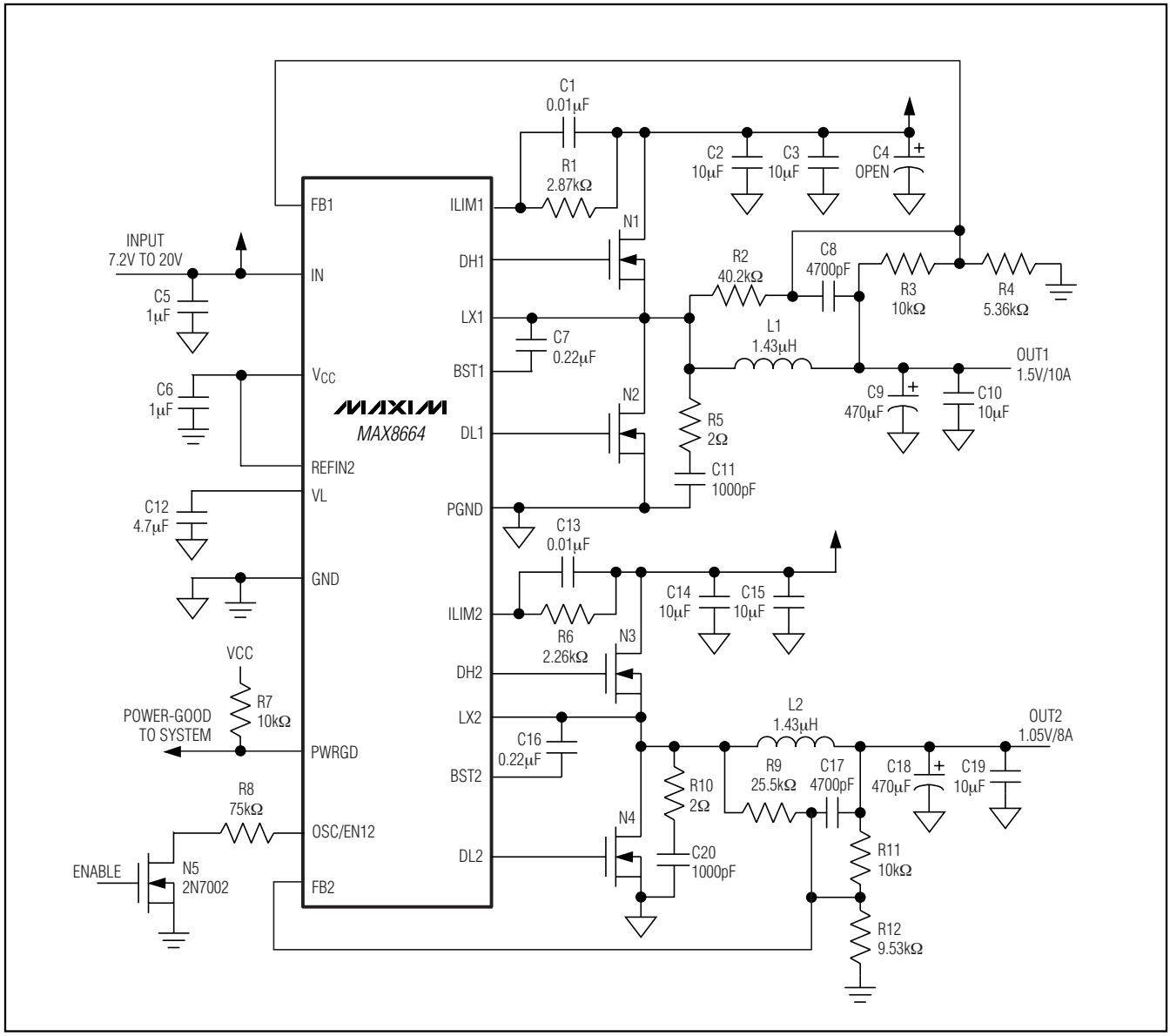

Figure 5. 300kHz Circuit with 7.2V to 20V Input

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

Table 5. Component List for Figure 5

DESIGNATION	QTY	DESCRIPTION
C1, C13	2	0.01µF, 10V X7R ceramic capacitors
C2, C3, C14, C15	4	10µF, 25V X5R ceramic capacitors
C5	1	1µF, 25V X5R ceramic capacitor
C6	1	1µF, 10V X5R ceramic capacitor
C7, C16	2	0.22µF, 10V X7R ceramic capacitors
C8, C17	2	4700pF, 10V X7R ceramic capacitors
C9, C18	2	470µF/2.5V POSCAP capacitors Sanyo 2R5TPD470M6
C10, C19	2	10µF, 6.3V X5R ceramic capacitors
C11, C20	2	1000pF, 25V X7R ceramic capacitors
C12	1	4.7µF, 10V X5R ceramic capacitor
L1, L2	2	1.43µH, 4.52mΩ inductors Panasonic ETQP3H1E4BFA
N1–N4	4	n-channel MOSFETs IRF7821 (8-pin SOs)
N5	1	n-channel MOSFET 2N7002 (SOT23)
R1	1	2.87kΩ ±1% resistor (0402 or 0603)
R2	1	40.2kΩ ±1% resistor (0402 or 0603)
R3, R11	2	10kΩ ±1% resistors (0402 or 0603)
R4	1	5.36kΩ ±1% resistor (0402 or 0603)
R5, R10	2	2.0Ω ±5% resistors (1206)
R6	1	2.26kΩ ±1% resistor (0402 or 0603)
R7	1	10kΩ ±5% resistor (0402 or 0603)
R8	1	75kΩ ±1% resistor (0402 or 0603)
R9	1	25.5kΩ ±1% resistor (0402 or 0603)
R12	1	9.53kΩ ±1% resistor (0402 or 0603)

Power-Up and Sequencing

The MAX8664 features an OSC/EN12 input that is used both for setting the switching frequency and as an enable input for both controllers. A resistor from OSC/EN12 to GND sets the switching frequency, and when OSC/EN12 is high impedance, both controllers enter low-power shutdown mode. This is easily achieved with a transistor between the resistor and GND. Figure 6a shows the startup configuration with independent outputs. With REFIN2 connected to V_{CC}, both controllers use the internal reference.

For tracking applications, connect REFIN2 to the center of a resistive voltage-divider between the output of controller 1 and GND. See Figure 6b. In this application, the output of regulator 2 tracks the output voltage of controller 1. The voltage-divider resistors set the V_{OUT2}/V_{OUT1} ratio. A typical tracking application is for the VTT supply of DDR memory.

Figure 6c shows one method of sequencing the outputs. Output 1 rises first. When PWRGD goes high, the transistors allow the external reference to drive REFIN2 and output 2 rises. The circuit in Figure 6d functions similarly, except the enable signal is supplied externally instead of being driven by the PWRGD signal.

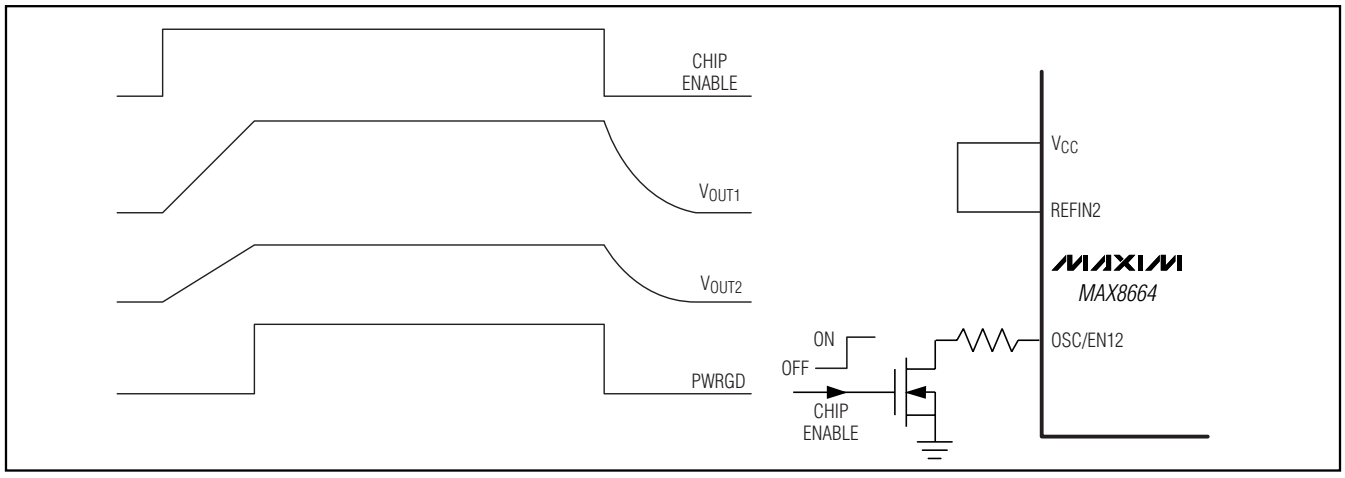

Figure 6a. Two Independent Output Startup and Shutdown Waveforms

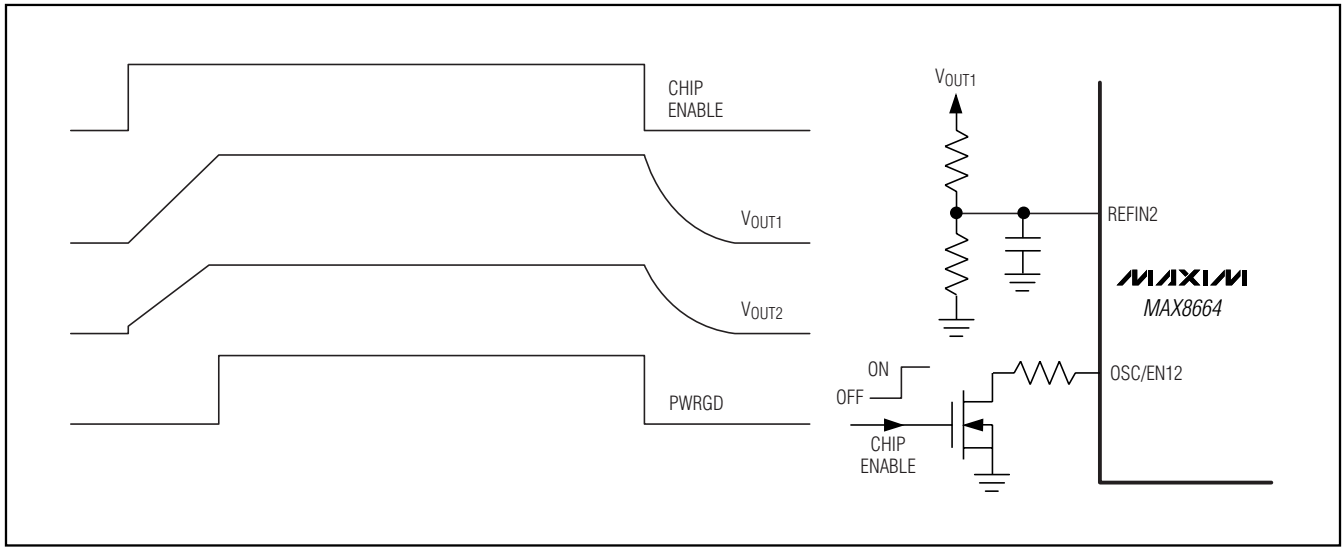

Figure 6b. Ratiometric Tracking Startup and Shutdown Waveforms

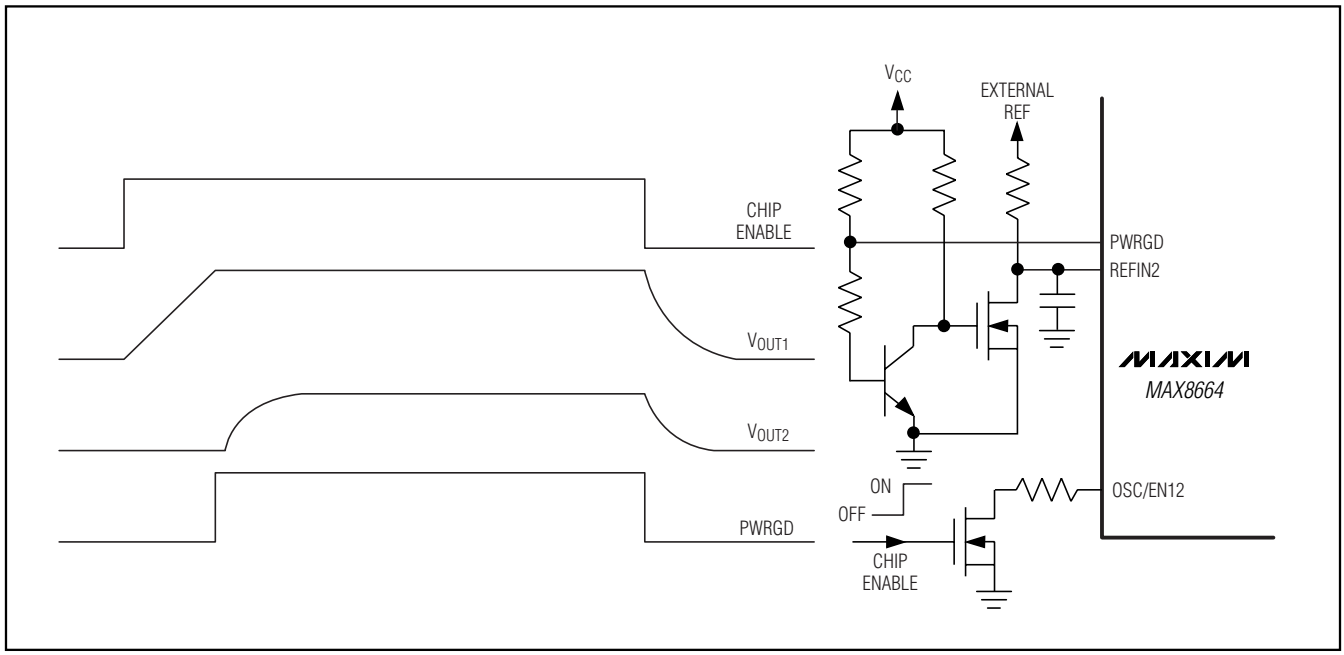

Figure 6c. Sequencing Startup and Shutdown Waveforms

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

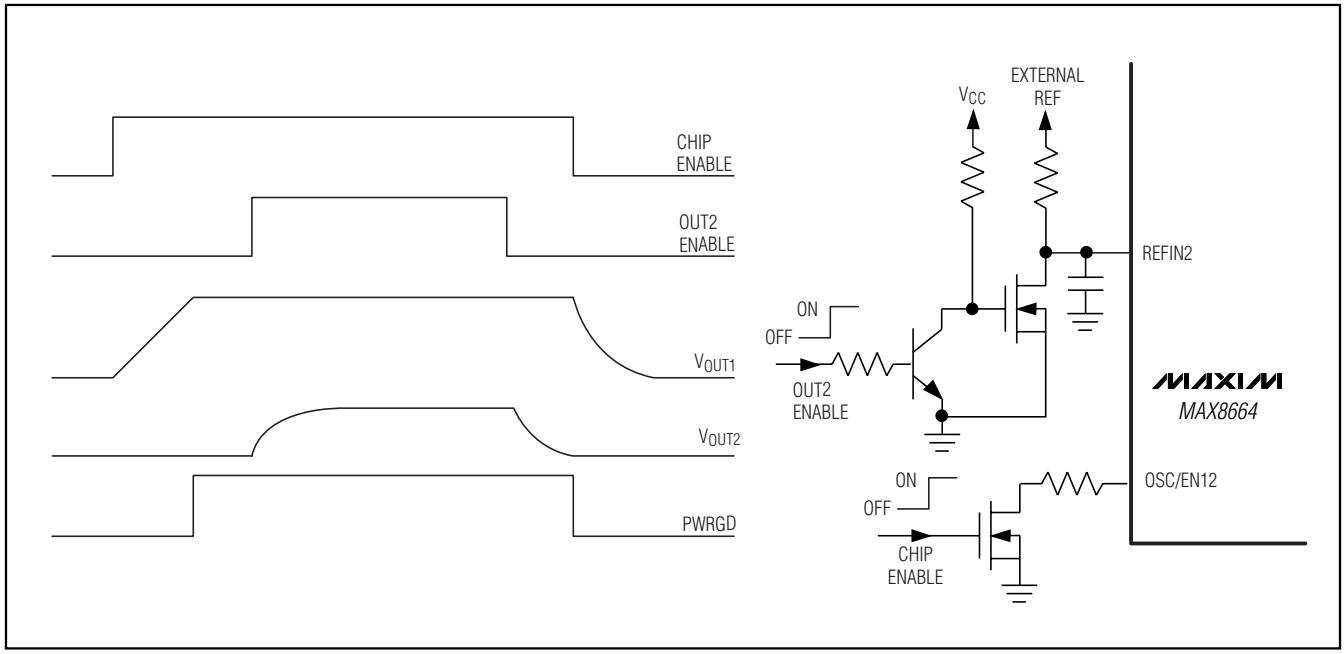

Figure 6d. Sequencing Startup and Shutdown Waveforms with System Enable 2 Signal

Design Procedure

Setting the Switching Frequency

Connect a resistor from OSC/EN12 to GND to set the switching frequency between 100kHz and 1000kHz. Calculate the resistor value (R10 in Figures 2–5) as follows:

$$R10 = \frac{2.24 \times 10^{10}(Hz)}{f_S}(\Omega)$$

Inductor Selection

There are several parameters that must be examined when determining which inductor is to be used. Input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor-current ripple to maximum DC load current ($I_{LOAD(MAX)}$). A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple. A good compromise between size and efficiency is an LIR of 0.3. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. Choose a standard value inductor close to the calculated value. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. This is especially true if the inductance is increased without also increasing the physical size of the inductor. Find a low-loss inductor having the lowest possible DC resistance that fits the allotted dimensions. The chosen inductor's saturation current rating must exceed the peak inductor current determined as:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements. These parameters affect the overall stability, output voltage ripple, and transient response. The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's ESR, and ESL caused by the current into and out of the capacitor. The maximum output voltage ripple is estimated as follows:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple as a consequence of the ESR, ESL, and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN}}{L + ESL} \times ESL$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

where I_{P-P} is the peak-to-peak inductor current:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

These equations are suitable for initial capacitor selection, but final values should be chosen based on a prototype or evaluation circuit. As a general rule, a smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value and input voltage, the output-voltage ripple decreases with larger inductance, and increases with higher input voltages. Ceramic, tantalum, or aluminum polymer electrolytic capacitors are recommended. The aluminum electrolytic capacitor is the least expensive; however, it has higher ESR and ESL. To compensate for this, use a ceramic capacitor in parallel to reduce the switching ripple and noise. For reliable and safe operation, ensure that the capacitor's voltage and ripple-current ratings exceed the calculated values.

The response to a load transient depends on the selected output capacitors. After a load transient, the output voltage instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output voltage deviates further depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on its closed-loop bandwidth. With a higher bandwidth, the response time is faster, thus preventing the output voltage from further deviation from its regulating value.

Setting the Output Voltages and Voltage Positioning

Figure 7 shows the feedback network used on the MAX8664. With this configuration, a portion of the feedback signal is sensed on the switched side of the inductor (LX), and the output voltage droops slightly as the load current is increased due to the DC resistance of the inductor (DCR). This allows the load regulation to be set to match the voltage droop during a load transient (voltage positioning), reducing the peak-to-peak output voltage deviation during a load transient, and reducing the output capacitance requirements.

To set the magnitude of the voltage positioning, select a value for R2 in the 8kΩ to 24kΩ range, then calculate the value of R1 as follows:

$$R1 = R2 \times \left(\frac{I_{OUT(MAX)} \times DCR}{\Delta V_{OUT(MAX)}} - 1 \right)$$

where $I_{OUT(MAX)}$ is the maximum output current and $\Delta V_{OUT(MAX)}$ is the maximum allowable droop in the output voltage at full load.

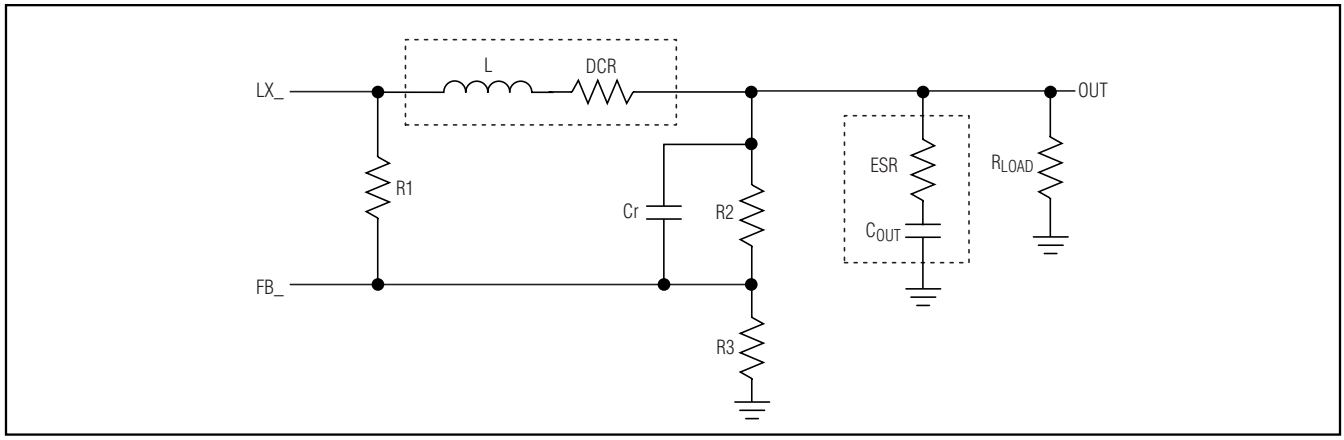

Figure 7. Feedback Network

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To set the no-load output voltage (V_{OUT}), calculate the value of R3 as follows:

$$R3 = \left(\frac{V_{FB}}{V_{OUT} - V_{FB}}\right)\left(\frac{R1 \times R2}{R1 + R2}\right)$$

where V_{FB} is the feedback regulation voltage (0.6V when using the internal reference or V_{REFIN2} for external reference). If the desired output voltage is equal to the reference voltage (typical for tracking applications), R3 is not installed.

To achieve the lowest possible load regulation in applications where voltage positioning is not desired, R1 is not installed and R3 is calculated as follows:

$$R3 = \left(\frac{V_{FB}}{V_{OUT} - V_{FB}}\right) \times R2$$

Compensation

To ensure stable operation, connect a compensation capacitor (Cr) across the upper feedback resistor as shown in Figure 7. To find the value of this capacitor, follow the compensation design procedure below.

Choose a closed-loop bandwidth (f_C) that is less than 1/3 the switching frequency (f_S). Calculate the output double pole (f_O) as follows:

$$f_O = \frac{1}{2\pi\sqrt{L \times C_{OUT} \times \frac{R_{LOAD} + ESR}{R_{LOAD} + DCR}}}$$

The FB peak-to-peak voltage ripple is:

$$V_{FB\_RIPPLE} = \left(\frac{1 + \frac{R2}{R1}}{1 + \frac{R2}{R3} + \frac{R2}{R1}}\right) \times \left(\frac{V_{OUT}}{\left(1 + \frac{DCR}{R_{LOAD}}\right) \times \frac{f_C}{f_O}}\right)$$

The output ripple voltage due to the ESR of the output capacitor, C_{OUT}, is:

$$V_{OUT\_RIPPLE} = \frac{\frac{V_{OUT}}{V_{IN}}\left(V_{IN} - V_{OUT}\right)}{L \times f_S} \times \left(ESR + \frac{1}{8 \times C_O \times f_S}\right)$$

Target the feedback ripple in the 25mV to 60mV range. For high duty-cycle applications (> 70%), a feedback ripple of 25mV is recommended.

Finally, calculate the value of Cr as follows:

$$Cr = \frac{\frac{V_{OUT}}{V_{IN}}\left(V_{IN} - V_{OUT}\right)}{R1 \times f_S \times \left|\left(V_{FB\_RIPPLE} - V_{OUT\_RIPPLE}\right)\right|}$$

MOSFET Selection

Each output of the MAX8664 is capable of driving two to four external, logic-level, n-channel MOSFETs as the circuit switch elements. The key selection parameters are:

- On-resistance ($R_{DS(ON)}$)—the lower, the better.
- Maximum Drain-to-Source Voltage (V_{DSS})—should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
- Gate charges (Q_g, Q_{gd}, Q_{gs})— the lower, the better.

For a 5V input application, choose MOSFETs with rated $R_{DS(ON)}$ at $V_{GS} \le 4.5V$. With higher input voltages, the internal VL regulator provides 6.5V for gate drive in order to minimize the on-resistance for a wide range of MOSFETs.

For a good compromise between efficiency and cost, choose the high-side MOSFETs that have conduction losses equal to switching losses at nominal input voltage and output current. Low $R_{DS(ON)}$ is preferred for low-side MOSFETs. Make sure that the low-side MOSFET(s) does not spuriously turn on due to dV/dt caused by the high-side MOSFET(s) turning on, as this would result in shoot-through current and degrade the efficiency. MOSFETs with a lower Q_{gd} / Q_{gs} ratio have higher immunity to dV/dt. For high-current applications, it is often preferable to parallel two MOSFETs rather than to use a single large MOSFET.

For proper thermal management, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage. For the-low side MOSFET(s), the worst-case power dissipation occurs at the highest duty cycle ($V_{IN(MAX)}$). The low-side MOSFET(s) operate as zero voltage switches; therefore, major losses are the channel conduction loss (P_{LSCC}) and the body diode conduction loss (P_{LSDC}):

$$P_{LSCC(MAX)} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \times I^2_{LOAD(MAX)} \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{LSDC(MAX)} = 2 \times I_{LOAD(MAX)}\ V_F \times t_{DT} \times f_S$$

where V_F is the body diode forward-voltage drop, t_{DT} is the dead time between high-side and low-side switching transitions (25ns typical), and f_S is the switching frequency.

The high-side MOSFET(s) operate as duty-cycle control switches and have the following major losses: the channel conduction loss (P_{HSCC}), the overlapping switching loss (P_{HSSW}), and the drive loss (P_{HSDR}). The maximum power dissipation could occur either at $V_{IN(MAX)}$ or $V_{IN(MIN)}$:

$$P_{HSCC(MAX)} = \frac{V_{OUT}}{V_{IN(MIN)}} \times I^2_{LOAD(MAX)} \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{HSSW(MAX)} = V_{IN(MAX)} \times I_{LOAD(MAX)} \times \frac{Q_{GD}}{I_{GATE}} \times f_S$$

where I_{GATE} is the average DH driver output-current capability determined by:

$$I_{GATE} \cong \frac{0.5 \times V_{VL}}{R_{DS(ON)(DR)} + R_{GATE}}$$

where $R_{DS(ON)(DR)}$ is the DH_ driver's on-resistance (see the *Electrical Characteristics*) and R_{GATE} is the internal gate resistance of the MOSFET (~ 2Ω):

$$P_{HSDR} = Q_G \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DS(ON)(DR)}}$$

where $V_{GS} \approx V_{VL}$.

The high-side MOSFET(s) do not have body diode conduction loss, unless the converter is sinking current. When sinking current, calculate this loss as $P_{HSDC(MAX)} = I_{LOAD(MAX)} \times V_F \times (2 \times t_{DT} + t_{WD}) \times f_S$, where t_{WD} is about 130ns.

Allow an additional 20% for losses due to MOSFET output capacitances and low-side MOSFET body diode reverse-recovery charge dissipated in the high-side MOSFET(s). Refer to the MOSFET data sheet for thermal resistance specifications to calculate the PCB area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

MOSFET Snubber Circuit

Fast switching transitions cause ringing because of resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, a series RC snubber circuit is added across each low-side switch. Below is the procedure for selecting the value of the series RC circuit.

Connect a scope probe to measure $V_{LX\_}$ to GND and observe the ringing frequency, f_R.

Find the capacitor value (connected from LX_ to GND) that reduces the ringing frequency by half.

The circuit parasitic capacitance (C_{PAR}) at LX_ is then equal to 1/3 the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R_{SNUB}) is equal to $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak-voltage excursion.

The capacitor (C_{SNUB}) should be at least 2 to 4 times the value of the C_{PAR} to be effective. The power loss of the snubber circuit is dissipated in the resistor (P_{RSNUB}) and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_{SW}$$

where V_{IN} is the input voltage and f_{SW} is the switching frequency. Choose an R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Setting the Overcurrent Threshold

Connect a resistor from ILIM_ to the drain of the high-side MOSFET(s) to set the overcurrent protection threshold. ILIM_ sinks 50µA (typ) through this resistor. When the drain-source voltage exceeds the voltage drop across this resistor during the high-side MOSFET(s) on-time, overcurrent protection is triggered. To set the output current level where overcurrent protection is triggered (I_{LIMIT}), calculate the value of the ILIM_ resistor as follows:

$$R_{ILIM\_} = \frac{R_{DS(ON)HS} \times I_{LIMIT}}{50\mu A}$$

where $R_{DS(ON)HS}$ is the maximum on-resistance of the high-side MOSFET(s) at +25°C. At higher temperatures, the ILIM current increases to compensate for the temperature coefficient of the high-side MOSFET(s).

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

Input Capacitor

The input filter capacitors reduce peak currents drawn from the power source and reduce noise and voltage ripple on the input caused by the circuit's switching. The input capacitors must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The ripple current requirement can be estimated by the following equation:

$$I_{RMS} = \frac{1}{V_{IN}} \sqrt{(I_{OUT1})^2 \times V_{OUT1} \times (V_{IN} - V_{OUT1}) + (I_{OUT2})^2 \times V_{OUT2} \times (V_{IN} - V_{OUT2})}$$

Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

Applications Information

PCB Layout Guidelines

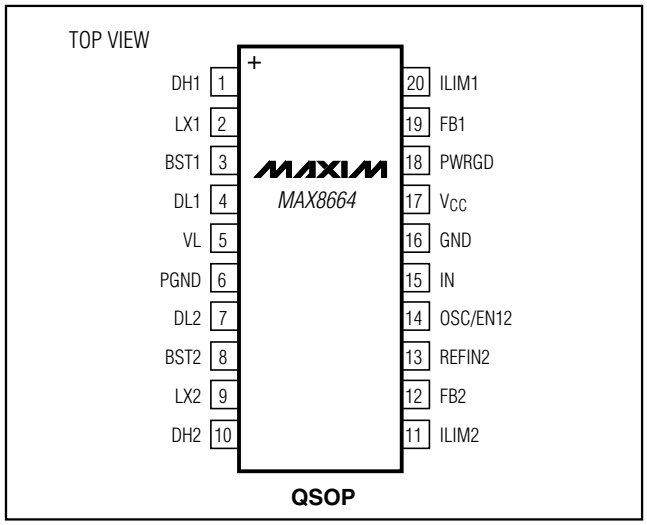
Careful PCB layout is an important factor in achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

1) A multilayer PCB is recommended.
2) Place IC decoupling capacitors as close as possible to the IC pins. Keep separate power ground and signal ground planes. Place the low-side MOSFETs near the PGND pin. Arrange the high-side MOSFETs and low-side MOSFETs in such a way that the high-side MOSFET's drain is close and near the low-side MOSFET's source. This allows the input ceramic decoupling capacitor to be placed directly across and as close as possible to the high-MOSFET's drain and the low-side MOSFET's source. This helps contain the high switching current within this small loop.
3) Pour an analog ground plane in the second layer underneath the IC to minimize noise coupling.
4) Connect input, output, and VL capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
5) Place the MOSFETs as close as possible to the IC to minimize trace inductance of the gate drive loop. If parallel MOSFETs are used, keep the trace lengths to both gates equal and short.
6) Connect the drain leads of the power MOSFET to a large copper area to help cool the device. Refer to the power MOSFET data sheet for recommended copper area.
7) Place the feedback network components as close as possible to the IC pins.
8) The current-limit setting RC should be Kelvin connected to the high-side MOSFETs' drain.

Refer to the MAX8664 evaluation kit for an example layout.

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

Pin Configuration



Chip Information

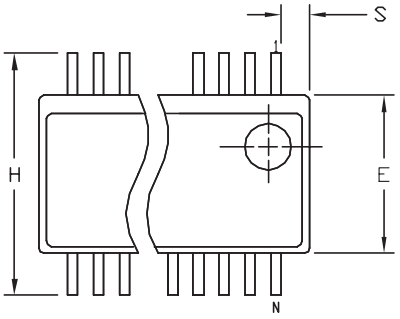
PROCESS: BiCMOS

Low-Cost, Dual-Output, Step-Down Controller with Fast Transient Response

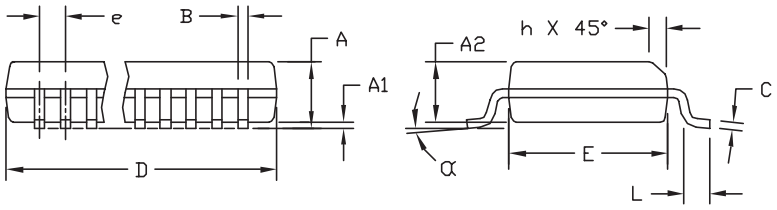
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	F	1/1