19-1174; Rev 0; 12/96

MAXIM

Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

General Description

The MAX768 low-noise, dual-output, regulated charge pump provides a negative output for biasing GaAsFET power amplifiers, and a positive output for powering voltage-controlled oscillators (VCOs) in wireless handsets. The outputs can also be used to power LCDs. Output ripple is less than 2mVp-p. The MAX768 is intended for use in low-voltage systems where a simple charge-pump inverter is inadequate, or where the VCO needs more range to improve its signal-to-noise ratio. The input range is 2.5V to 5.5V, enabling direct power from 1Li+ and 3-cell NiMH/NiCd batteries.

The MAX768 includes a voltage-doubler charge pump, followed by an inverting charge pump. This combination produces unregulated outputs that are ±2x the input. Two internal low-dropout linear regulators provide the low-noise, regulated positive and negative outputs. Output current is guaranteed to be at least 5mA per output. The linear regulators use CMOS devices, so the quiescent current remains independent of output loading (even in dropout), and the dropout voltage approaches zero with no load current.

The MAX768 has two preset switching frequencies (25kHz or 100kHz), or can be synchronized by an external clock from 20kHz to 240kHz. This flexibility permits users to optimize their designs based on noise, capacitor size, and quiescent-supply-current criteria.

The device features Dual Mode™ operation: the output voltage is preset to +5V and -5V, or can be adjusted by adding external resistor dividers. Other features include independent shutdowns and a logic output that signals when the negative voltage has risen to within 10% of its regulation setpoint (to protect the power amplifier GaAsFET). The MAX768 is available in a space-saving, 16-pin QSOP, which is the same size as a standard 8-pin SO.

Applications

GaAsFET Power Amp Bias
Voltage-Controlled Oscillator (VCO) Supply
Tuner Diode Power Supply
Positive and Negative LCD Supply
Cellular Phone
PCS and Cordless Phone
Wireless Handsets
Wireless Handheld Computers
Wireless PCMCIA Cards
Modems

Features

- **Dual Positive/Negative Regulated Outputs: ±5V$_{OUT}$ from 3V$_{IN}$**
- **Output-Ready Indicator to Protect GaAsFET PAs**
- **2.5V to 5.5V Input Voltage Range**
- **Low-Noise Output Ripple: < 2mVp-p**
- **Synchronizable Switching Frequency**
- **Uses Only Small, Low-Cost Capacitors**
- **0.1µA Independent Shutdown Controls**
- **Adjustable Output Voltages**
- **Small 16-Pin QSOP Package**

Ordering Information

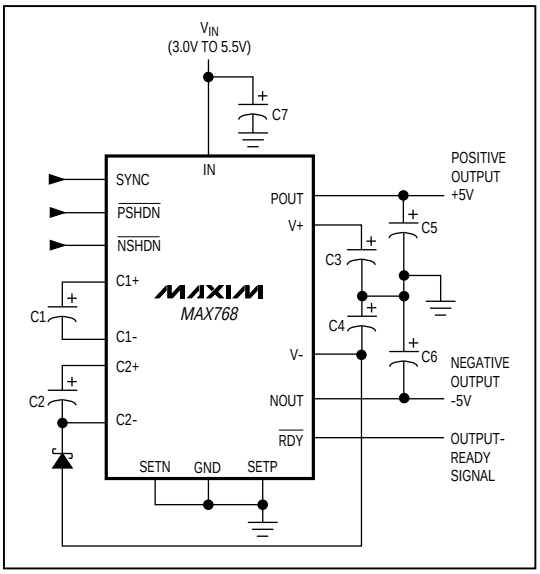
PART	TEMP. RANGE	PIN-PACKAGE
MAX768C/D	0°C to +70°C	Dice*
MAX768EEE	-40°C to +85°C	16 QSOP

**Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configuration appears at end of data sheet.

Dual Mode is a trademark of Maxim Integrated Products.

Typical Operating Circuit



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Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

ABSOLUTE MAXIMUM RATINGS

VIN, C1-, SYNC, $\overline{PSHDN}$, $\overline{NSHDN}$ to GND.....-0.3V to +6V
V+, C1+, C2+, $\overline{RDY}$ to GND.....-0.3V to +12V
SETP to GND ..... -0.3V to +3V
SETN to GND.....-3V to +0.3V
V-, C2- to GND ..... -12V to +0.3V
OUTP, OUTN Short Circuited to GND .....Continuous
NOUT to V- ..... -0.3V to +12V
POUT to V+ ..... -12V to +0.3V

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.70mW/°C above +70°C).....696mW
Operating Temperature Range
MAX768EEE.....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, SYNC = IN, SETN = SETP = GND, $\overline{NSHDN}$ = $\overline{PSHDN}$ = IN, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 2.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			3.0		5.5	V
Minimum Input Start-Up Voltage	I_{LOAD} = 0			2.5		V
Positive Output Voltage	0mA < I_{LOAD} < 5mA, V_{IN} = 3.0V to 5.5V		4.81	5.00	5.14	V
Negative Output Voltage	0mA < I_{LOAD} < 5mA, V_{IN} = 3.0V to 5.5V		-5.10	-5.00	-4.82	V
Positive Output Voltage Adjustable Range	(Note 2)		1.25		11	V
Negative Output Voltage Adjustable Range	(Note 3)		-11		-1.25	V
Maximum POUT, NOUT Output Currents	V_{IN} = 3V, V_{POUT} ≥ 4.81V, V_{NOUT} ≤ -4.82V		5			mA
No-Load Supply Current at 100kHz (both regulators active)	V_{IN} = 3.0V			0.8	1.4	mA
	V_{IN} = 5.5V			1.5		
No-Load Supply Current at 100kHz (negative regulator off)	$\overline{NSHDN}$ = GND			0.3		mA
No-Load Supply Current at 25kHz (both regulators active)	V_{SYNC} = GND			0.45	0.80	mA
Dropout Voltage (2 x V_{IN} - $\lvert V_{OUT} \rvert$)	2 x V_{IN} - $\lvert V_{OUT} \rvert$	I_{POUT} = I_{NOUT} = 0.1mA		20		mV
		I_{POUT} = I_{NOUT} = 5mA		420	900	
Line Regulation	V_{IN} = 3V to 5.5V		-0.12	0.0	0.12	%/V
Load Regulation	I_{POUT} = 0mA to 5mA, I_{NOUT} = 0mA to -5mA			0.06	0.12	%/mA
Output Voltage Noise	C_{POUT} = C_{NOUT} = 10µF, 10kHz < f < 1MHz	POUT		1.2		mVp-p
		NOUT		1.7		
Shutdown/SYNC Logic-Low Input Threshold					0.4	V
Shutdown/SYNC Logic-High Input Threshold			2.0			V
SHUTDOWN						
$\overline{SHDN}$ Input Bias Current	$V_{\overline{SHDN}}$ = 3V			0.1	2	µA
Shutdown Supply Current	$\overline{NSHDN}$ = $\overline{PSHDN}$ = SYNC = GND			0.1	10	µA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, SYNC = IN, SETN = SETP = GND, $\overline{NSHDN}$ = $\overline{PSHDN}$ = IN, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 2.) (Note 1)

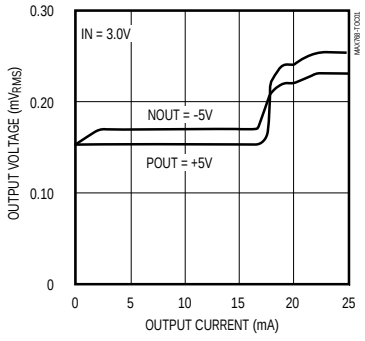
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC						
SYNC Frequency Range (external)			20		240	kHz
SYNC Duty Cycle (external)			40		60	%
Oscillator Frequency (internal)	SYNC = GND (divide by 4)		21.5	25	28.5	kHz
	V_{SYNC} = 3V		85	100	115	
SYNC Input Leakage Current				0.1	2	µA
SET INPUT						
Positive Set-Reference Voltage	I_{POUT} = 0.1mA	T_A = +25°C	1.217	1.25	1.283	V
		T_A = -40°C to + 85°C	1.215	1.25	1.285	
Negative Set-Reference Voltage	I_{NOUT} = 0.1mA	T_A = +25°C	-1.270	-1.25	-1.230	V
		T_A = -40°C to + 85°C	-1.275	-1.25	-1.225	
SETP, SETN Input Leakage Current	V_{SETP} = V_{SETN} = 1.3V			0.01	0.1	µA
$\overline{RDY}$ OUTPUT						
$\overline{RDY}$ Output Threshold	Percent of V_{NOUT}, I_{NOUT} = 5mA		85	94	98	%
Output Low Voltage	I_{SINK} = 2mA				0.25	V
Output Off Current	V_{RDY} = 10V			0.01	2	µA
Maximum Sink Current				10		mA

Note 1: Parameters to -40°C are guaranteed by design, not production tested.
Note 2: Maximum output voltage range is from the positive reference voltage to 2 x V_{IN} - dropout voltage.
Note 3: Maximum output voltage range is from the negative reference voltage to -2 x V_{IN} + dropout voltage.

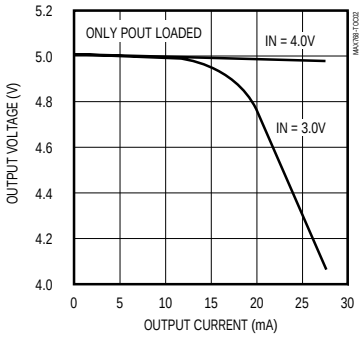
Typical Operating Characteristics

(SYNC = IN, T_A = +25°C, unless otherwise noted.)

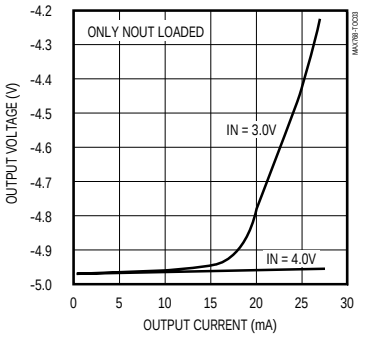
mV_{RMS} OUTPUT VOLTAGE vs. OUTPUT CURRENT



POUT OUTPUT VOLTAGE vs. OUTPUT CURRENT



NOUT OUTPUT VOLTAGE vs. OUTPUT CURRENT



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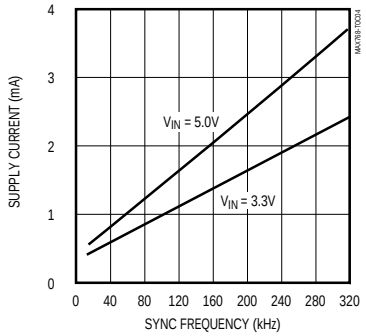
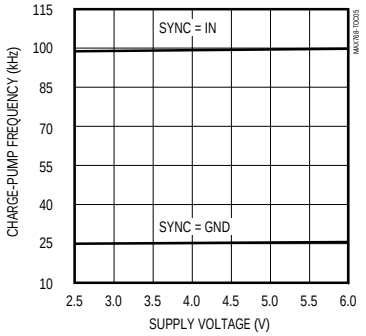
Typical Operating Characteristics (continued)

(SYNC = IN, T_A = +25°C, unless otherwise noted.)

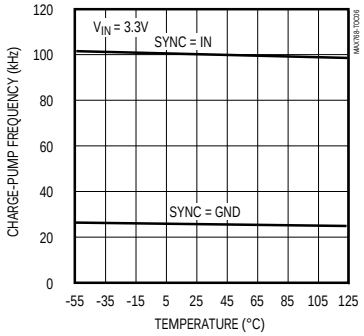
SUPPLY CURRENT vs. SYNC FREQUENCY



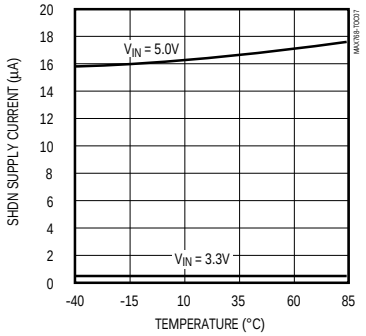
CHARGE-PUMP FREQUENCY vs. SUPPLY VOLTAGE



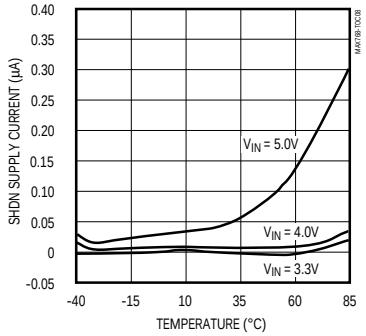
CHARGE-PUMP FREQUENCY vs. TEMPERATURE



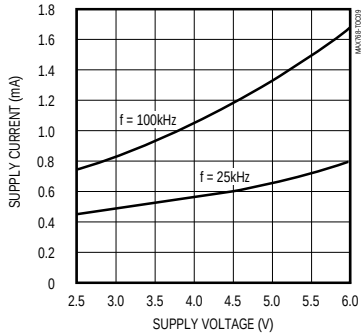
SHDN SUPPLY CURRENT vs. TEMPERATURE



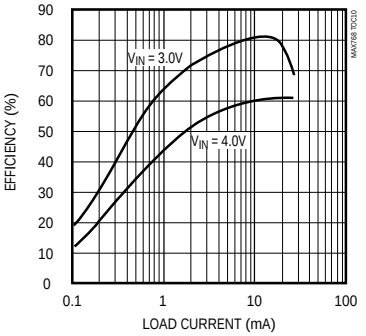
SHDN SUPPLY CURRENT vs. TEMPERATURE



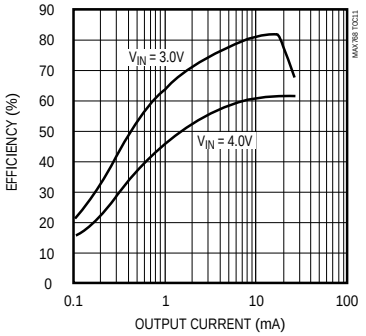
SUPPLY CURRENT vs. SUPPLY VOLTAGE (NO LOAD)



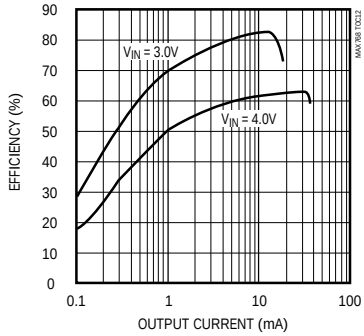
EFFICIENCY vs. LOAD CURRENT (NOUT ONLY LOADED)



EFFICIENCY vs. OUTPUT CURRENT (POUT ONLY LOADED)



EFFICIENCY vs. OUTPUT CURRENT LOAD BETWEEN POUT AND NOUT



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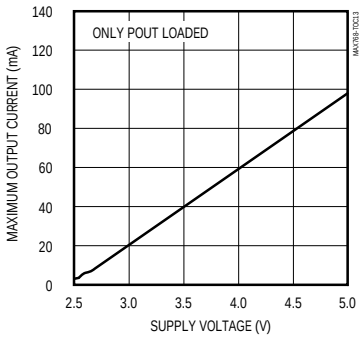
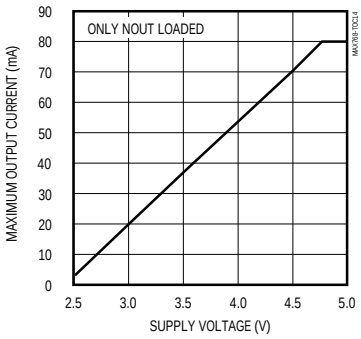
Typical Operating Characteristics (continued)

(SYNC = IN, T_A = +25°C, unless otherwise noted.)

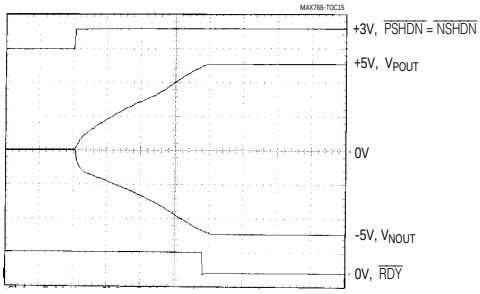
POUT MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



NOUT MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE

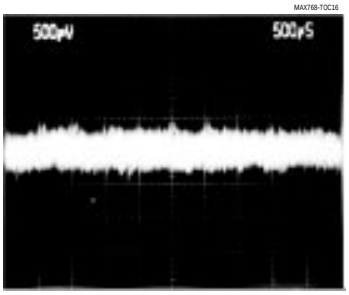


TIME TO EXIT SHUTDOWN



1ms/div

POUT OUTPUT NOISE AND RIPPLE

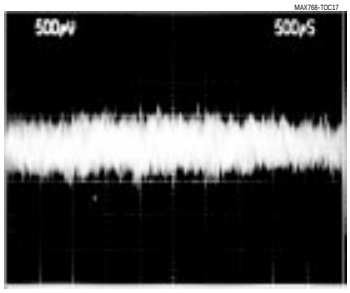


VPOUT, 500µV/div
AC COUPLED

500µs/div

POUT = +5V AT 5mA
IN = 3.0V

NOUT OUTPUT NOISE AND RIPPLE



VNOUT, 500µV/div
AC COUPLED

500µs/div

NOUT = -5V AT 5mA
IN = 3.0V

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Pin Description

PIN	NAME	FUNCTION
1	C1-	Negative Terminal of the Doubler Charge-Pump Capacitor. See Table 2 for capacitor selection.
2	GND	Ground
3	C2-	Negative Terminal of the Inverter Charge-Pump Capacitor
4	V-	Inverter Charge-Pump Output. See Table 2 for capacitor selection.
5	NOUT	Negative Regulator Output. See Table 2 for capacitor selection.
6	SETN	Set Negative Output Voltage Input. Connect SETN to GND for factory-preset -5V. Connect a resistor divider between NOUT, SETN, and GND for custom output voltage setting.
7	$\overline{\text{NSHDN}}$	Negative-Supply Shutdown Input. Pull $\overline{\text{NSHDN}}$ low to turn off the inverting charge pump, the negative regulator, and the bias-ready indicator. If $\overline{\text{PSHDN}}$ is also low, the part completely shuts down.
8	$\overline{\text{PSHDN}}$	Positive-Supply Shutdown Input. Pull $\overline{\text{PSHDN}}$ low to turn off the positive regulator. If $\overline{\text{NSHDN}}$ is also low, the part completely shuts down.
9	SYNC	Clock Synchronizing Input. Connect an external 20kHz ≤ f_{CLK} ≤ 240kHz to SYNC to synchronize the MAX768 to that frequency. Connect SYNC to GND to select the internal 25kHz clock, or to IN for the internal 100kHz clock.
10	$\overline{\text{RDY}}$	Output-Ready Indicator. This open-drain output pulls to GND when the negative output voltage (NOUT) is within 10% of the regulation voltage.
11	SETP	Set Positive Output Voltage Input. Connect SETP to GND for factory-preset +5V output. Connect a resistor divider between POUT, SETP, and GND for custom output voltage setting.
12	POUT	Positive Regulator Output. See Table 2 for capacitor selection.
13	V+	Doubler Charge-Pump Output. See Table 2 for capacitor selection.
14	C1+	Positive Terminal of the Doubler Charge-Pump Capacitor. See Table 2 for capacitor selection.
15	IN	Supply (3V to 5.5V). Bypass IN with 4.7µF to GND.
16	C2+	Positive Terminal of the Inverter Charge-Pump Capacitor. See Table 2 for capacitor selection.

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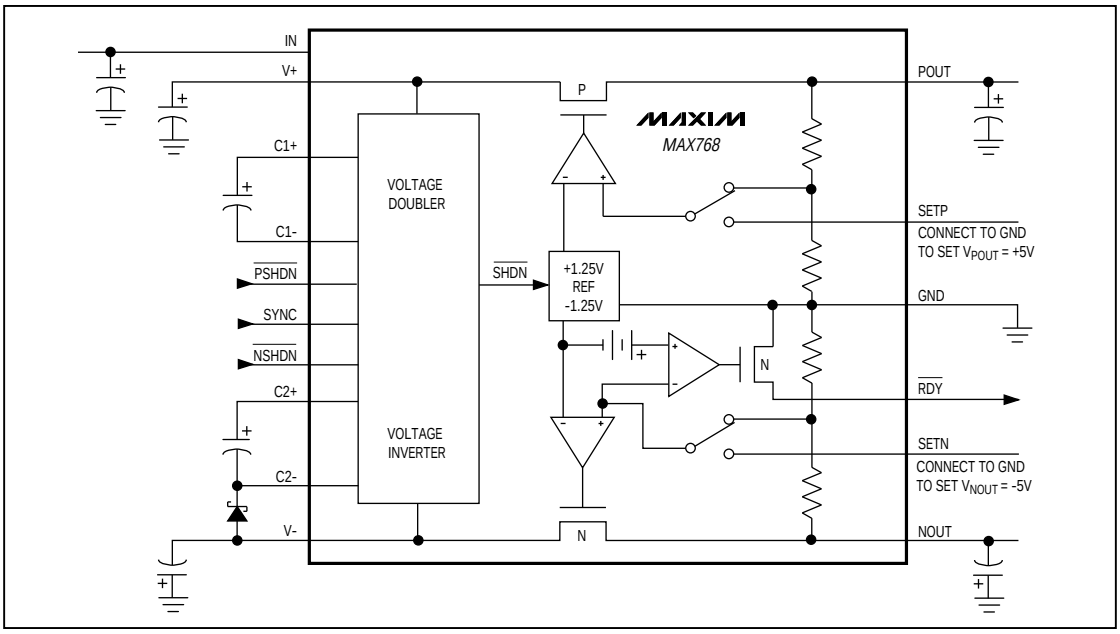

Figure 1. Functional Diagram

Detailed Description

The MAX768 requires only seven external capacitors to implement a regulated voltage doubler/inverter. These can be ceramic or polarized electrolytic capacitors ranging from 2.2µF to 47µF. Figure 1 is a functional diagram of the MAX768. The applied input voltage (V_{IN}) is first doubled to a value of $2V_{IN}$ by a capacitor charge pump and then stored in the V+ reservoir capacitor. Next, the voltage at V+ is inverted to $-2V_{IN}$ and stored at the V- reservoir capacitor. The voltages at V+ and V- are then linear regulated and appear at POUT and NOUT, respectively. The ripple noise induced by the doubling and inverting charge pump is reduced by the linear regulators to 1.2mVp-p for POUT and 1.7mVp-p for NOUT. In addition, the linear regulator's excellent AC rejection attenuates noise from the incoming supply. A minimum of 5mA is available at each output. When NOUT is more negative than 90% of the regulated output voltage, the open-drain $\overline{RDY}$ output pulls to GND.

The charge pump operates in three modes: when $\overline{SYNC}$ = GND, the charge pump operates at 25kHz; when $\overline{SYNC}$ = IN, it operates at 100kHz, or $\overline{SYNC}$ can be overdriven with an external clock in the 20kHz to 240kHz range. The clock must have a 40% to 60% duty cycle.

Applications Information

Setting the Output Voltage

Connect SETP or SETN directly to GND to select a fixed +5V or -5V output voltage, respectively (Figure 2). Select an alternative voltage for either output by connecting SETP or SETN to the midpoint of a resistor voltage divider from POUT or NOUT, respectively, to GND (Figure 3). ($2 \times V_{IN}$) must be 1.0V above the absolute value of the output voltage to ensure proper regulation. Calculate the output voltage from the formulas below. Choose R1 and R3 at between 100kΩ to 400kΩ.

$$R2 = (R1)\left(\frac{V_{POUT}}{V_{PSET\ REF}} - 1\right)$$

$$R4 = (R3)\left(\frac{V_{NOUT}}{V_{NSET\ REF}} - 1\right)$$

where $V_{PSET\ REF}$ = 1.25V (typical) and $V_{NSET\ REF}$ = -1.25V (typical).

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Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

Table 1. Shutdown-Control Logic

$\overline{PSHDN}$	$\overline{NSHDN}$	POUT STATUS	NOUT STATUS	SUPPLY CURRENT (mA)
1	1	Positive output active	Negative output active	0.8
1	0	Positive output active	Negative output inactive	0.7
0	1	Positive output inactive	Negative output active	0.3
0	0	Shutdown (low-power mode)	Shutdown (low-power mode)	0.0001

Table 2. Charge-Pump Capacitor Selection (Figure 2)

SYNC INPUT	FREQUENCY (kHz)	CAPACITORS		
		C1, C2, C3, C4	C5, C6	C7
GND	25	10µF	10µF	4.7µF
IN	100	2.2µF		
External Clock	20 to 240	C = 220µF/f (kHz)		

Shutdown

The MAX768 has two active-low, TTL logic-level shutdown inputs: $\overline{PSHDN}$ and $\overline{NSHDN}$. When both inputs are pulled low, the MAX768 shuts down and the supply current is reduced to 10µA max over temperature. Pulling $\overline{PSHDN}$ low turns off the positive linear regulator; the doubler charge pump remains active. Pulling the $\overline{NSHDN}$ input low while $\overline{PSHDN}$ remains high turns off the inverter charge pump, the negative linear regulator, and the output-ready indicator (Table 1).

Capacitors

The overall dropout voltage is a function of the charge pump's output resistance and the voltage drop across the linear regulator. The charge-pump output resistance is a function of the switching frequency and the capacitor's ESR value. Therefore, minimizing the charge-pump capacitors' ESR minimizes dropout voltage.

$$R_{POUT} = 84 + 8(C1_{ESR}) + (C3_{ESR}) + \frac{2}{f_{OSC}C1}$$

$$R_{NOUT} = 84 + 8(C1_{ESR}) + 4(C2_{ESR}) + (C4_{ESR}) + \frac{2}{f_{OSC}C1} + \frac{1}{f_{OSC}C2}$$

See Table 2 for capacitor selection. All capacitors should be either surface-mount ceramic chip or tantalum. External capacitor values may be adjusted to optimize size, performance, and cost.

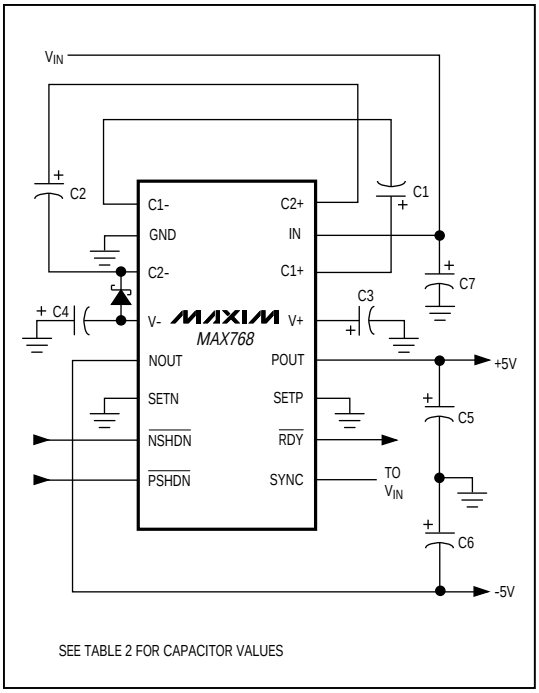

Figure 2. MAX768 Standard Application Circuit

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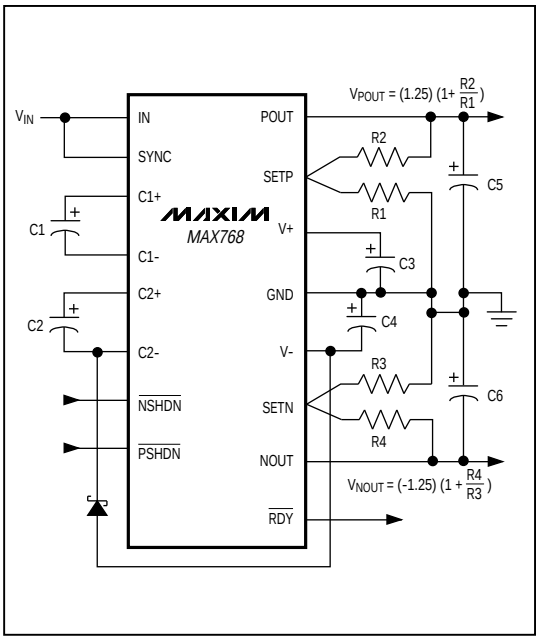

Figure 3. MAX768 Adjustable Configuration

Switching-Frequency Control

For applications sensitive to the MAX768's internal switching frequency, connect an external TTL/CMOS (within IN and GND) clock to SYNC. The clock must be a 20kHz to 240kHz square wave between 40% and 60% duty cycle.

Schottky Diodes

When under heavy loads, where POUT is sourcing into NOUT (i.e., load current flows from POUT to NOUT, rather than from supply to ground), do not allow NOUT to pull above ground. In applications where large currents from POUT to NOUT are likely, use a Schottky diode (1N5817) between GND and NOUT, with the anode connected to GND (Figure 4).

Connect a IN5817-type Schottky diode from C2- to V- to assure proper start-up.

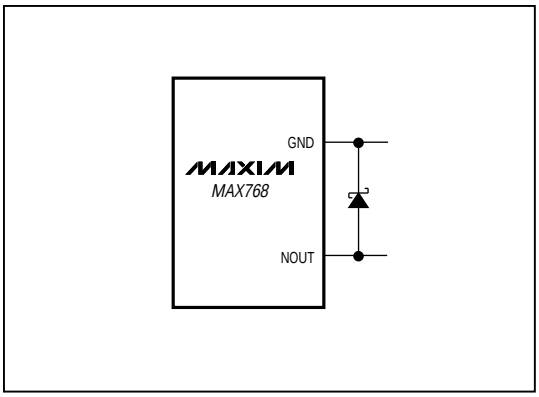

Figure 4. A Schottky diode protects the MAX768 when a large current flows from POUT to NOUT.

Layout and Grounding

Good layout is important, primarily for good noise performance:

1) Mount all components as close together as possible.
2) Keep traces short to minimize parasitic inductance and capacitance. This includes connections to SETP and SETN.
3) Use a ground plane.

Noise and Ripple Measurement

Accurately measuring output noise and ripple can be difficult. Brief differences in ground potential between the circuit and the oscilloscope (which result from the charge pump's switching action) cause ground currents in the probe's wires, inducing sharp voltage spikes. For best results, measure directly across output capacitor C3, C4, C5, or C6. Do not use the oscilloscope probe's ground lead; instead, remove the cover's ground lead and touch the ground ring on the probe directly to the ground terminal of C3, C4, C5, or C6. Or, use a Tektronix chassis-mount test jack (part no. 131-0258) to connect your scope probe directly. This direct connection provides the most accurate noise and ripple measurement.

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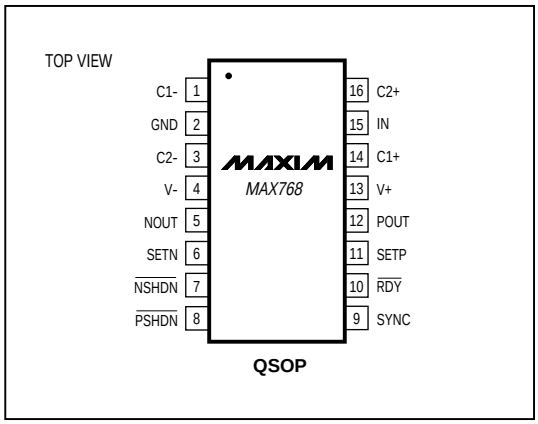
Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies

Pin Configuration



Chip Information

TRANSISTOR COUNT: 657

SUBSTRATE CONNECTED TO GND

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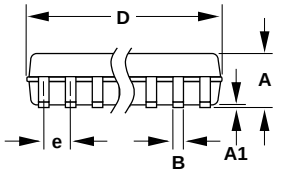
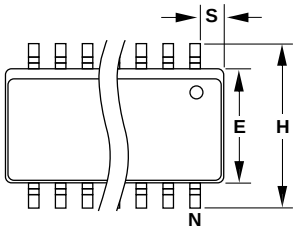
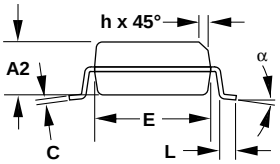
Package Information







DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.127	0.25
A2	0.055	0.061	1.40	1.55
B	0.008	0.012	0.20	0.31
C	0.0075	0.0098	0.19	0.25
D	SEE PIN COUNT VARIATIONS			
E	0.150	0.157	3.81	3.99
e	0.25 BSC		0.635 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
N	SEE PIN COUNT VARIATIONS			
S	SEE PIN COUNT VARIATIONS			
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.189	0.196	4.80	4.98
S	16	0.0020	0.0070	0.05	0.18
D	20	0.337	0.344	8.56	8.74
S	20	0.0500	0.0550	1.27	1.40
D	24	0.337	0.344	8.56	8.74
S	24	0.0250	0.0300	0.64	0.76
D	28	0.386	0.393	9.80	9.98
S	28	0.0250	0.0300	0.64	0.76

21-0055A

QSOP
QUARTER
SMALL-OUTLINE
PACKAGE

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NOTES

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