19-0097; Rev 1; 8/93

Evaluation Kit Available

MAXIM

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

MAX741

General Description

The MAX741 is a highly versatile switch-mode power-supply (SMPS) controller IC that operates from an input supply as low as 2.7V, and typically starts up from 1.8V.

The MAX741 can be pin-programmed into hundreds of different SMPS configurations. The internal blocks (reference, error amplifier, etc.) are interconnected via analog switches so they can be reconfigured into different architectures by applying trilevel data (V+, VREF, GND) to certain logic input pins. This pin-programming feature lends tremendous application flexibility. For example, the output stage can drive N-channel or P-channel MOSFETs (or bipolar transistors) in single-ended, complementary, or push-pull modes. The error amplifier can accommodate positive or negative feedback voltages. The output voltage can be adjusted with external resistors, or it can be set at any one of six preset values by switching in the appropriate laser-trimmed resistor-divider network.

For mainstream applications (step-up, step-down, and inverting), basic MAX741 circuits can be designed directly into the system with little effort using the tested circuit layouts found in the *Application Circuits* section. At the same time, the MAX741 provides the power-supply designer the right inputs and controls to implement nearly any SMPS function.

Applications

Battery-Operated Equipment
Distributed Power Systems
Isolated Off-Line Supplies
On-Card DC-DC Converters

Features

- ♦ **Pin-Programmable Architecture**
- ♦ **Operates on Supply Voltages from 2.7V**
- ♦ **Starts up from 1.8V**
- ♦ **Low Supply Current — 1.6mA (MAX741U) (50µA in Shutdown)**
- ♦ **Bootstrap Input for Low-Voltage Applications**
- ♦ **Current-Mode PWM Control**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **Adjustable Undervoltage Lockout and Soft-Start**
- ♦ **Oscillator Synchronization Input/Output**
- ♦ **Shutdown-Control Input**
- ♦ **Low-Noise, Fixed-Frequency Operation**
- ♦ **Evaluation Kits Available**
- ♦ **PCB Layout Information Available**

Ordering Information

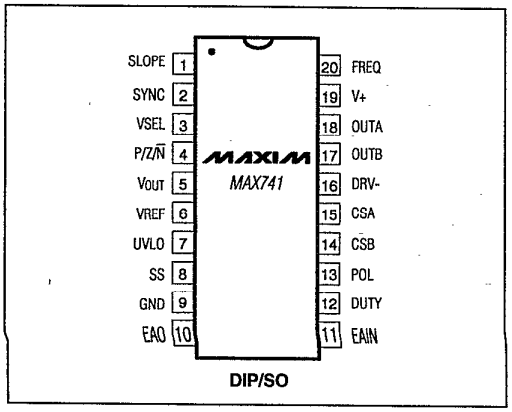
PART	TEMP. RANGE	PIN-PACKAGE
MAX741UCPP	0°C to +70°C	20 Plastic DIP
MAX741UCAP	0°C to +70°C	20 SSOP
MAX741UC/D	0°C to +70°C	Dice*
MAX741UEPP	-40°C to +85°C	20 Plastic DIP
MAX741UEAP	-40°C to +85°C	20 SSOP
MAX741UMJP	-55°C to +125°C	20 CERDIP**

Ordering Information continued on last page.

* *Dice are tested at T_A = +25°C only.*

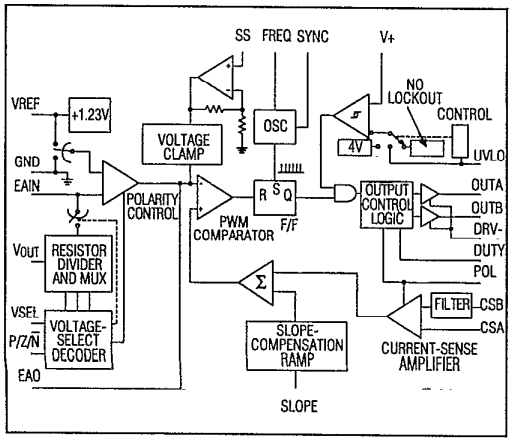
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



DIP/SO

Block Diagram



Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V+ to GND ..... +17V, -0.3V
Oscillator Output Voltage (SYNC) ..... -0.3V to (V+ + 0.3V)
MOSFET Driver Supply Voltage (DRV- to V+) ..... +0.3V, -17V
Feedback Voltage (V_{OUT} to GND) ..... ±50V
Auxiliary Input Voltages (SLOPE, SS, VSEL, P/Z/$\overline{N}$, EAIN, DUTY, POL, CSA, CSB, FREQ to GND) ..... -0.3V to (V+ + 0.3V)
Peak Output Current (I_{OUTA} or I_{OUTB}) 1.0A
Reference Current (I_{VREF}) 2.5mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX741_C__ ..... 0°C to +70°C
MAX741_E__ ..... -40°C to +85°C
MAX741_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply-Voltage Range		2.7		15.5	V
Start-Up Supply Voltage	T_A = +25°C, UVLO = V+		1.8		V
Shutdown-Mode Supply Current	FREQ = 0V, T_A = +25°C		50	150	µA
Reference Voltage		1.17	1.23	1.29	V
Reference-Voltage Line Regulation	V+ = 2.7V to 15.5V, T_A = +25°C		±0.5	±4	mV/V
Reference-Voltage Load Regulation	I_{LOAD} = 0µA to 300µA, T_A = +25°C, MAX741N only		1.4	6	mV
Oscillator Frequency	FREQ = V+, T_A = +25°C	130	160	190	kHz
	FREQ = VREF, T_A = +25°C		150		
External Clock Frequency Synchronization Range (at SYNC)			40-200		kHz
SYNC Input Capacitance			10		pF
SYNC Trip Threshold	"0" level, used as clock input		0.2		V
	"1" level, used as clock input		V+ - 0.2		
3-Level Pin Trip Thresholds (P/Z/$\overline{N}$, FREQ, DUTY)	High Level		V+ - 0.3		V
	Middle Level		VREF±0.3		
	Low Level		0.3		
SYNC Output Low Voltage	I_{OL} = 25µA, used as clock output		0.2		V
SYNC Output High Voltage	I_{OH} = 25µA, used as clock output		4.8		V
SYNC Input Current	V_{IH} = V+, used as clock input		1.0		mA
	V_{IL} = 0V, used as clock input		-1.0		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error-Amplifier Input Bias Current	P/Z/$\overline{N}$ = VREF		0.005	10	µA
Error-Amplifier Open-Loop Gain	EAO = 2V to 3V		2000		V/V
Output Voltage Low	OUTA or OUTB, T_A = +25°C, I_{OL} = 50mA		0.65	0.95	V
	I_{OL} = 50mA, DRV- = -10V		-9.85	-9.50	
Output Voltage High	OUTA or OUTB, T_A = +25°C, I_{OH} = -50mA	4.10	4.35		V
	I_{OH} = -50mA, DRV- = -10V	4.50	4.70		
Output Rise or Fall Time	OUTA or OUTB, T_A = +25°C, C_{LOAD} = 1nF (Note 1)		50	100	ns
UVLO Threshold	Adjustable mode, measured at UVLO (Note 1)	0.39 x VREF	0.425 x VREF	0.46 x VREF	V
UVLO Start-Up Threshold	UVLO = 0V	3.0	4.0	4.4	V

ELECTRICAL CHARACTERISTICS – MAX741U

(Step-Up Circuit of Figure 1a, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, V+ = 3.3V, VSEL = V+ (Note 2)	4.80	5.00	5.20	V
	VSEL = VREF, T_A = +25°C	11.52	12.00	12.48	
	VSEL = 0V, T_A = +25°C	14.40	15.00	15.60	
	Adjustable mode, referred to error-amplifier input	1.18	1.23	1.28	
Supply Current	VSEL = V+ = 3.3V (Note 3)		1.6	3.5	mA

ELECTRICAL CHARACTERISTICS – MAX741N

(Inverting Circuit of Figure 1b, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, VSEL = V+ (Note 2)	-5.20	-5.00	-4.80	V
	VSEL = VREF, T_A = +25°C	-12.48	-12.00	-11.52	
	VSEL = 0V, T_A = +25°C	-15.60	-15.00	-14.40	
	Adjustable mode, R1 = 50kΩ, R2 = 50kΩ	-1.29	-1.23	-1.17	
Supply Current	VSEL = V+ (Note 3)		2.2	4.0	mA

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

ELECTRICAL CHARACTERISTICS – MAX741D

(Step-Down Circuit of Figure 1c, V+ = 12V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

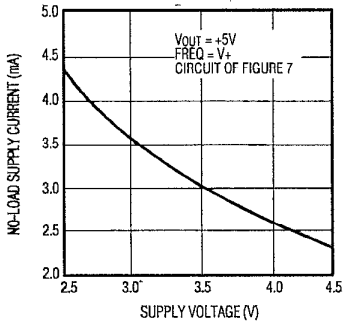
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, VSEL = V+ (Note 2)	4.80	5.00	5.20	V
	Adjustable mode, referred to error-amplifier input	1.18	1.23	1.28	
Supply Current	VSEL = V+ (Note 3)		2.8	4.25	mA

Note 1: Guaranteed, but not 100% tested.
Note 2: Output Voltage Initial Accuracy tests include the effects of the error-amplifier input offset voltage.
Note 3: Total supply current under actual operating conditions, including currents drawn by components.

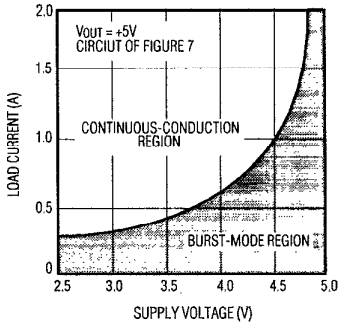
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

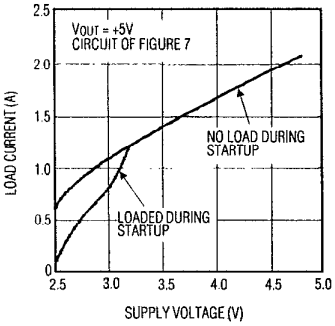
MAX741U STEP-UP NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



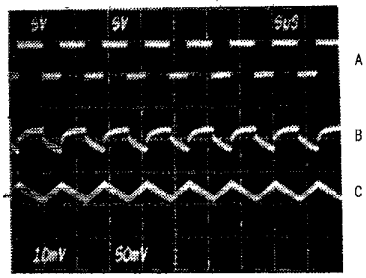
MAX741U STEP-UP CONTINUOUS-CONDUCTION REGION



MAX741U STEP-UP LOAD CURRENT vs. SUPPLY VOLTAGE

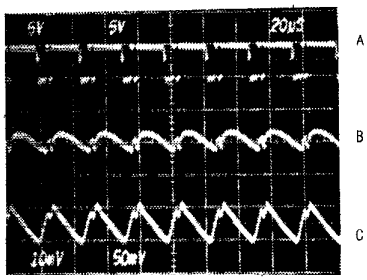


MAX741U SWITCHING WAVEFORMS – CONTINUOUS-CONDUCTION



A = MOSFET DRAIN VOLTAGE (5V/div)
B = OUTPUT VOLTAGE RIPPLE (AC: 50mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

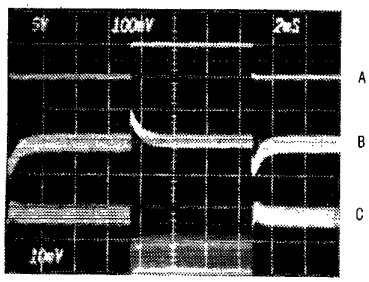
MAX741U SWITCHING WAVEFORMS – BURST-MODE



A = MOSFET DRAIN VOLTAGE (5V/div)
B = OUTPUT VOLTAGE RIPPLE (AC: 50mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

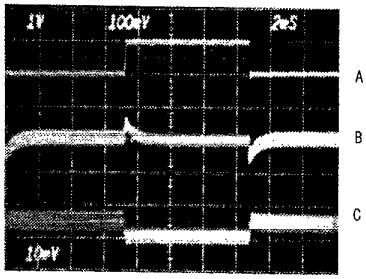
Typical Operating Characteristics (continued)

MAX741U LOAD-TRANSIENT RESPONSE



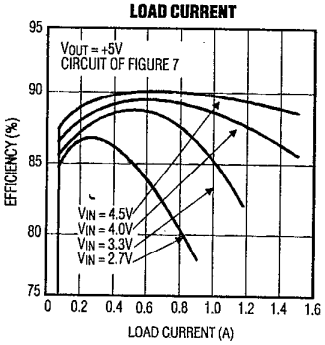
A = 1A LOAD (HIGH) / 200mA LOAD (LOW)
B = OUTPUT VOLTAGE (AC: 100mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

MAX741U LINE TRANSIENT RESPONSE

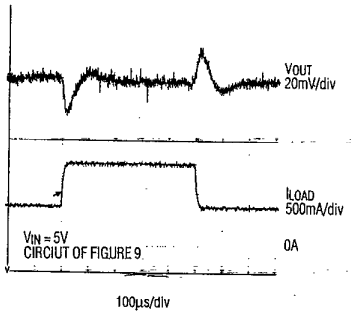


A = V_{IN} = 4V (HIGH) / V_{IN} = 3V (LOW)
B = OUTPUT VOLTAGE (AC: 100mV/div)
C = INDUCTOR CURRENT (1A/div)
CIRCUIT OF FIGURE 7

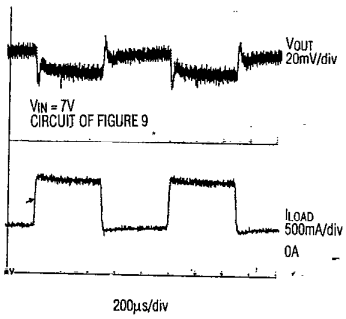
MAX741U STEP-UP EFFICIENCY vs. LOAD CURRENT



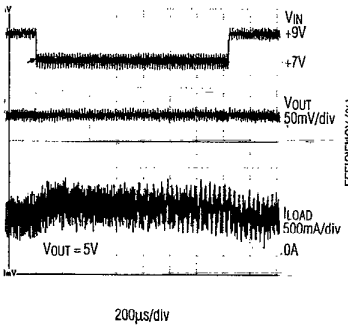
MAX741D STEP-DOWN LOAD-TRANSIENT RESPOSNE (V_{OUT} = 3.3V)



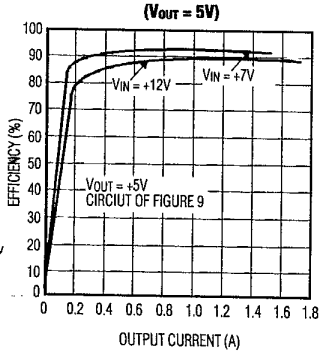
MAX741D STEP-DOWN LOAD-TRANSIENT RESPOSNE (V_{OUT} = 5V)



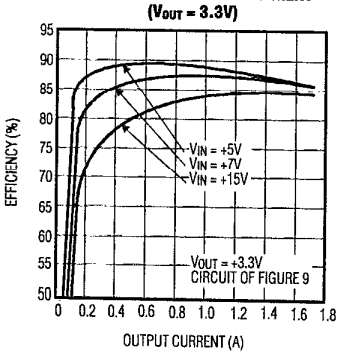
MAX741D STEP-DOWN LINE-TRANSIENT RESPOSNE



MAX741D STEP-DOWN EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5V)



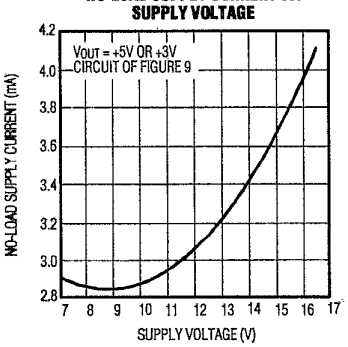
MAX741D STEP-DOWN EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 3.3V)



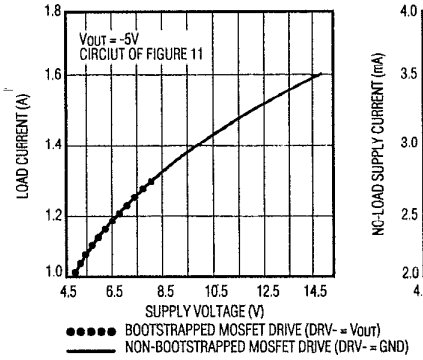
Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

Typical Operating Characteristics (continued)

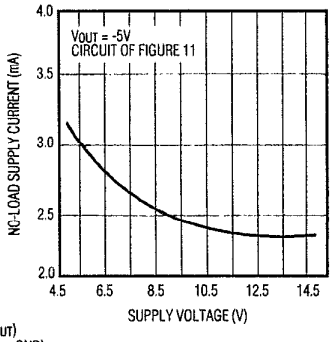
MAX741D STEP-DOWN NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



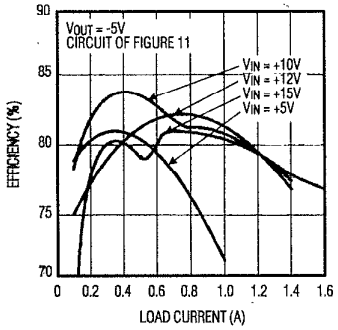
MAX741N INVERTING LOAD CURRENT vs. SUPPLY VOLTAGE



MAX741N INVERTING NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX741N INVERTING EFFICIENCY vs. LOAD CURRENT



Pin Description

PIN	NAME	FUNCTION
1	SLOPE	Sets slope compensation for AC stability. Normally a 50kΩ to 1MΩ resistor connected to ground. Required for continuous-conduction mode operation.
2	SYNC	SYNC output at the oscillator frequency. Also functions as a clock input when driven externally. Capacitive loads reduce oscillator frequency up to 25%. When using an external clock, the clock's high time corresponds to power switch-off time.
3	VSEL	Voltage Select (VSEL) and P/$\overline{Z}$/N are decoded to determine the output voltage. See Table 2 under *Output Voltage Selection*.
4	P/$\overline{Z}$/N	See VSEL (pin 3). V+ = Positive Output (P) VREF = Adjustable Mode ($\overline{Z}$) GND = Negative Output (N)
5	VOUT	Output Voltage connection to internal resistor dividers. Connect to output or leave open in adjustable mode.
6	VREF	Voltage-Reference Output that can source 300µA for external loads. Bypass with 1µF minimum.
7	UVLO	Undervoltage Lock-Out disables IC when V+ is less than the UVLO threshold. See *Undervoltage Lockout* section. V+ = No Lockout 0.47V+ to 0.075V+ = adjustable threshold GND = 4V threshold
8	SS	Soft-Start and current-limit adjust. A DC voltage applied here sets the maximum peak switch-current limit. See *Soft-Start and Current Limiting* section. An RC network reduces surge currents on start-up. Connect a 150kΩ resistor from VREF to SS and 0.1µF from SS to GND for a 15ms soft-start time. Always connect a resistor (50kΩ to 1MΩ) between VREF and SS.
9	GND	Ground
10	EAO	Error-Amplifier Output
11	EAIN	Error-Amplifier Input
12	DUTY	Duty-Cycle Adjust when DUTY = V+: push-pull mode, 50% max duty cycle DUTY = VREF: complementary, 50% max duty cycle DUTY = GND and FREQ = V+: complementary, 85% max duty cycle DUTY = GND and FREQ = VREF: complementary mode, 95% max duty cycle
13	POL	Polarity. Selects current-sense amplifier output polarity and controls OUTA and OUTB polarity when in push-pull mode. V+ = N-Channel (CS inputs sense around GND) GND = P-Channel (CS inputs sense around V+)
14	CSB	Current-Sense Amp "B" Input, connects to signal side of current-sense resistor. Signal passes through a 1st-order LP filter.
15	CSA	Current-sense amp "A" input. Connect to V+ in buck and inverting circuits. Connect to GND in step-up circuits. CSA should be bypassed with 0.1µF located close to CSA and GND when in the buck or inverting power-supply modes.
16	DRV-	Negative Drive Bootstrap Supply Voltage Input accepts a DC bias voltage as the negative supply rail for the drivers at OUTA and OUTB, useful when driving P-channel MOSFETs from low supply voltages. Observe *Absolute Maximum Ratings* carefully.
17	OUTB	Output B MOSFET Driver drives P-Channel or PNP transistors in complementary modes. See Table 1. When V+ > 14V, use 5.6Ω in series between OUTB and gate of power FET.
18	OUTA	Output A MOSFET Driver drives N-channel or NPN transistors in complementary modes. When V+ > 14V, use 5.6Ω in series between OUTA and gate of power FET. See Table 1.
19	V+	Positive Supply Voltage +2.7V to +15.5V. Bypass with at least 0.1µF close to V+ and GND pins of IC.
20	FREQ	Frequency/Shutdown Control sets oscillator frequency or forces a non-operating shutdown mode. V+ = 145kHz with 85% duty cycle 1.4V = 140kHz with 95% duty cycle (see 3-level input pins section) GND = Shutdown Mode

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

Detailed Description

The MAX741 is a monolithic, CMOS, current-mode PWM controller that can be used in a variety of configurations with one or more external power switching transistors. The current-mode PWM control scheme provides tight output-voltage regulation, excellent load- and line-transient response, and low noise. An external current-sensing resistor provides cycle-by-cycle current limiting, and output current limiting in applications where there is no DC path from input to output. The MAX741 is optimized for step-up (MAX741U), step-down (MAX741D), or inverting (MAX741N) configurations.

The basic step-up, step-down, and inverting applications, presented in detail in the *Application Circuits* section, use the standard topologies shown in Figure 1. Table 1 describes the pin programming necessary for various modes, including Figure 1's three basic circuits. The MAX741 can also accomodate specialized applications needing complementary or push/pull power switches. Table 1 describes the pin programming used to obtain complementary and push/pull drive, and Figure 2 shows the resulting drive waveforms at OUTA and OUTB.

Operating Principle

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current via the current-sense resistor and amplifier, and an outer (voltage) loop that monitors the output voltage via the error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, truncating the on-time of the power transistor when the switch current reaches a threshold predetermined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

Table 1. Output-Stage Programming

PROGRAM PINS			PROGRAM MODES			
DUTY	POL	FREQ	OUTA	OUTB	MODE	MAXIMUM DUTY CYCLE
V+	V+	V+	N	N	OUTA, OUTB push/pull	50%
V+	V+	VREF	N	N	OUTA, OUTB push/pull	50%
V+	GND	V+	P	P	OUTA, OUTB push/pull	50%
V+	GND	VREF	P	P	OUTA, OUTB push/pull	50%
V+	V+	GND	GND	GND	Shut down using N-channel push/pull	
V+	GND	GND	V+	V+	Shut down using P-channel push/pull	
VREF	V+	V+	N	P	OUTA, OUTB complementary	50%
VREF	V+	VREF	N	P	OUTA, OUTB complementary	50%
VREF	GND	V+	N	P	OUTA, OUTB complementary	50%
VREF	GND	VREF	N	P	OUTA, OUTB complementary	50%
VREF	X	GND	GND	V+	Shut down (non-push/pull mode)	
GND	V+	V+	N	P	OUTA, OUTB complementary	85%
GND	V+	VREF	N	P	OUTA, OUTB complementary	95%
GND	GND	V+	N	P	OUTA, OUTB complementary	85%
GND	GND	VREF	N	P	OUTA, OUTB complementary	95%
GND	X	GND	GND	V+	Shut down (non-push/pull mode)	

N = Drives N-Channel FETs (On = V+)
P = Drives P-Channel FETs (On = GND)
X = Don't Care

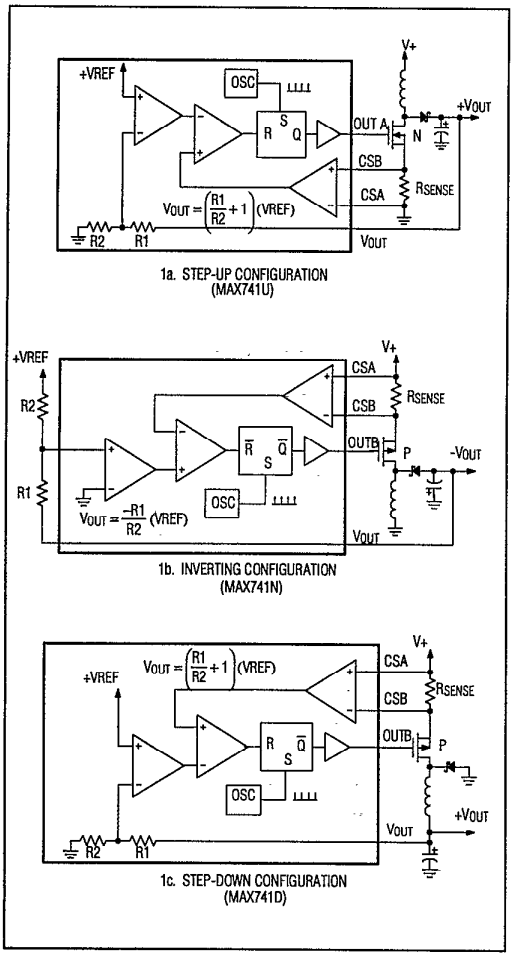


Figure 1. Basic Configurations

Continuous-/Discontinuous-Conduction Modes

In continuous-conduction mode (CCM), the inductor current never decays to zero. In discontinuous-conduction mode (DCM or "burst-mode"), the inductor current slope is steep enough so it decays to zero before the end of the transistor off-time. The MAX741 operates in either CCM or DCM by the selection of higher or lower inductor values, respectively. CCM allows the MAX741 to deliver maximum load currents, and is normally less noisy than DCM. However, DCM does not provide a continuous feedback path through the inductor, and hence is easier to stabilize; it does not require slope compensation, and allows for a smaller output capacitor.

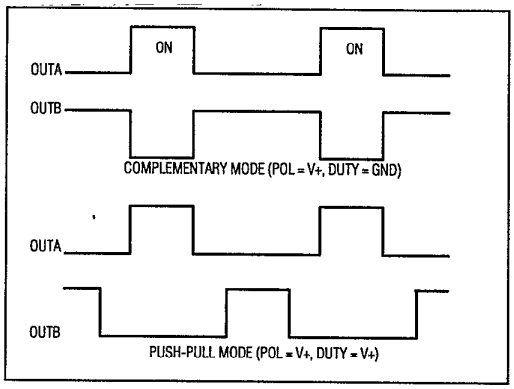


Figure 2. Push-Pull and Complementary Waveforms

Output-Voltage Selection

The output voltage can be adjusted by an external resistor-divider network, or it can be set to a fixed level (+5V, +12V, +15V, -5V, -12V or -15V) by pin programming the MAX741 as shown in Table 2. When using an external resistor divider, the output voltage is determined by the ratio of the resistors in the divider and the internal +1.23V reference. See the *Application Circuits* section for more information on output-voltage adjustment.

Table 2. Output Voltage

VSEL	P/Z/$\overline{N}$	OUTPUT	EAIN IMPEDANCE (Ω)
V+	V+	5V	16.5k
V+	VREF	Adj. Positive	>50M HiZ
V+	GND	-5V	17.5k
VREF	V+	12V	5.5k
VREF	VREF	Prohibited	NA
VREF	GND	-12V	16k
GND	V+	15V	5k
GND	VREF	Adj. Negative	>50M HiZ
GND	GND	-15V	10k

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3-Level Input Pins

Pins P/Z/$\overline{N}$, FREQ, and DUTY have three levels: Low (GND to 0.3V), middle (VREF ±0.3V), and high (V+ - 0.3V to V+). Obtain middle level operation by typing the appropriate 3-level input to VREF (Figure 8), except pin 20 (FREQ), which should be held at 1.4V. This 1.4V can be generated with two forward-biased diodes tied to ground and pulled up with 100kΩ to V+. This resistance value is suitable for V+ voltages in the +5V to +15V range. For operation with V+ as low as 2.7V, use a 60kΩ resistor.

Slope Compensation

Slope compensation is used to eliminate subharmonic oscillation in the power output stage. Compensation is controlled by resistor R_{SLOPE}, connected from SLOPE to ground. Current-mode regulators tend to oscillate in a local loop in the output stage, because the inductor current waveform can bounce between zero and the maximum current-limit threshold. This instability is corrected by a slope compensation scheme that adds a ramp signal to the current-sense amplifier output.

Slope compensation is required when the switch duty cycle exceeds 50%. When this is the case, varying degrees of slope compensation eliminate inner-loop instability. Excessive slope compensation makes the loop behave like a traditional voltage-mode (triangle-wave) PWM, where the AC stability can also suffer due to the extra pole in the loop response. Slope compensation is not required when operating in DCM.

Inner-loop instability manifests itself as "staircasing" of the inductor current, where the current waveform ramps up in steps until it hits the maximum current-limit threshold (set by the voltage at SS) and then declines. This effect is also seen in the output-voltage ripple waveform where the noise has a large subharmonic component, or at the switching nodes where the duty cycle is seen to be successively increasing over a period of several cycles. This instability differs distinctly from instability in the outer voltage regulation feedback loop, which has a more random character and must be debugged separately.

Ideal slope compensation is achieved by adding to the rising inductor current-sense signal a ramp whose value is equal to the slope of the **declining** inductor current. The slope (m) of the declining inductor current is determined from the output voltage and the inductance value:

$m = V_{OUT}/L$ for step-down converters and inverters; or
$m = (V_{OUT} - V_{IN})/L$ for step-up circuits.

The voltage slope (SVS) at the current-sense amplifier's output is equal to

$$SVS = (m)(R_{SENSE}),$$

where R_{SENSE} is the current-sense resistor value.

The slope compensation voltage (CVS) is generated by a current source (controlled by a resistor connected to the SLOPE pin) charging an internal 10pF capacitor, as shown in Figure 3. This compensation voltage is summed with the signal from the current-sense amplifier, and, for ideal compensation, must be equal to the declining inductor current signal (SVS) calculated above. Hence the slope compensation voltage is given by

$$SVS = CVS = VREF/[(20)(10pF)(R_{SLOPE})],$$

where the factor of 20 arises from the current source gain (Figure 3). Rearranged, these equations give the formula for the slope resistor (R_{SLOPE}) to be connected to the SLOPE pin:

$$R_{SLOPE} = VREF/[(20)(10pF)(m)(R_{SENSE})].$$

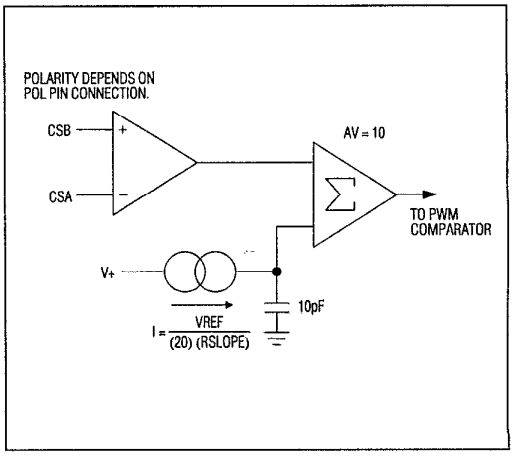

Figure 3. Current Amplifier and Slope Compensation Model

Slope Compensation Example

The following slope compensation calculation is for a +5V to +15V step-up converter using a 30µH inductor and a 0.1Ω sense resistor. The ideal compensation slope is equal to the declining inductor current slope, which is given by

$m = (V_{IN} - V_{OUT})/L$
$= (15V - 5V)/30\mu H = 0.33A/\mu s.$

The voltage slope (SVS) at the current-sense amplifier's output is equal to

$SVS = (m)(R_{SENSE})$
$= 0.33A/\mu s(0.1\Omega) = 0.033V/\mu s.$

The slope resistor (R_{SLOPE}) is thus

$R_{SLOPE} = VREF/[(20)(10pF)(m)(R_{SENSE})]$
$= 1.23V/[(20)(10pF)(0.33A/\mu s)(0.1\Omega)] = 186k\Omega$

AC Compensation

The stability of the outer voltage feedback loop can be evaluated using load-transient response tests. Significant overshoot or ringing after a step from zero to full load indicates potential stability problems. The outer loop can be compensated with an RC network around the error amplifier.

Typically, a pole-zero cancellation scheme is used to eliminate excess phase shift due to the zero caused by the output filter capacitor's equivalent series resistance (ESR). The following example shows the compensation calculations for a 1000µF, 0.05Ω ESR output capacitor (CF). The calculations are the same regardless of the circuit type (step-up, step-down, or inverting).

The zero caused by the output capacitor's ESR occurs at a frequency (f_Z) given by

$f_Z = 1/[(2)(\pi)(ESR)(CF)]$

$= 1/[(6.284)(0.05\Omega)(1000\mu F)] = 3.18kHz$

A cancellation pole is required at 3.18kHz. This compensation pole's frequency (f_P) is given by

$f_P = 1/[(2)(\pi)(R_{EAIN})(C4)]$

where R_{EAIN} is the impedance of the error-amplifier input pin (EAIN), and C4 is the value of the compensation capacitor in Figures 7 and 9. From Table 2, with VSEL and P/$\overline{Z}$/N connected to V+, EAIN has a nominal impedance of 16.5kΩ, so

$CC = 1/[(2)(\pi)(R_{EAIN})(f_P)]$

$= 1/[(2)(3.142)(16.5k\Omega)(3.18kHz)] = 3nF$

Additional outer-loop compensation may be required in step-up circuits. Capacitor C5 in Figure 7 provides the extra compensation needed in this application.

The actual compensation capacitor values required depends on the printed circuit layout and the capacitor type used. These values may, therefore, vary significantly from those calculated. Prototyping is essential.

Current-Sense Amplifier

The current-sense amplifier (Figure 4) employs a switched- capacitor design to achieve a common-mode voltage range that exceeds both supply rails by 0.3V. The current-sense amplifier has a gain of 10 with a 0.6V ±200mV output offset. For clarity, Figure 4's block diagram of the soft-start and current-limit sections omits the slope compensation circuit and summing amplifier shown in Figure 3.

Soft-Start (SS) and Current Limiting

The switch transistor's maximum peak current limit is determined by the voltage on SS. An external RC network on SS results in a gradual increase in peak current on power-up, minimizing the possibility of overloading the source.

The SS voltage is amplified by a factor of 3.5, and this voltage clamps the maximum swing of the error amplifier (a transconductance amplifier) as it is presented to the PWM comparator. For example: with SS connected to VREF (1.23V) and R_{SENSE} = 0.1Ω, the highest peak current is:

$$I_{PK} = \frac{3.5\ (V_S) - 0.6V}{(10)\ (R_{SENSE})} = \frac{3.5\ (1.23V) - 0.6V}{(10)\ (0.1\Omega)} = 3.7A,$$

where V_S is the SS pin voltage.

Under normal load, a good value for the peak voltage differential across the current-sense amplifier inputs is 200mV or so, achieved by adjusting the sense-resistor value. Setting the SS current limit at 1.5 to 2 times that (3V to 4V at the error-amplifier output) adds margin to handle worst-case loads.

Ensure that the error amplifier's maximum swing allows enough peak current to meet the average load current. Peak transistor current in a typical switch-mode power supply is several times greater than the DC load current. The exact value depends on configuration, input/output voltage ratio, frequency, and inductor value.

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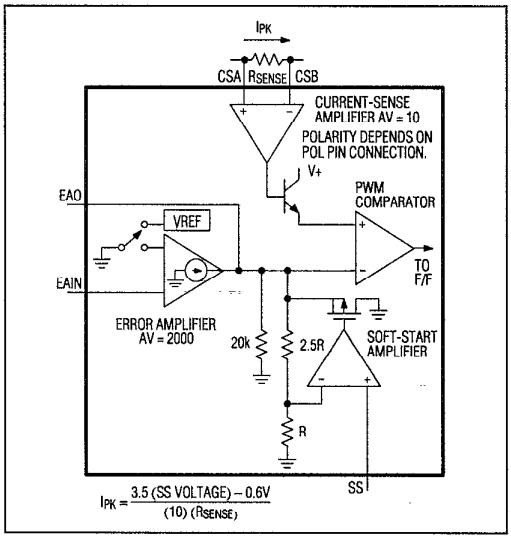

Figure 4. Soft-Start and Current Limit

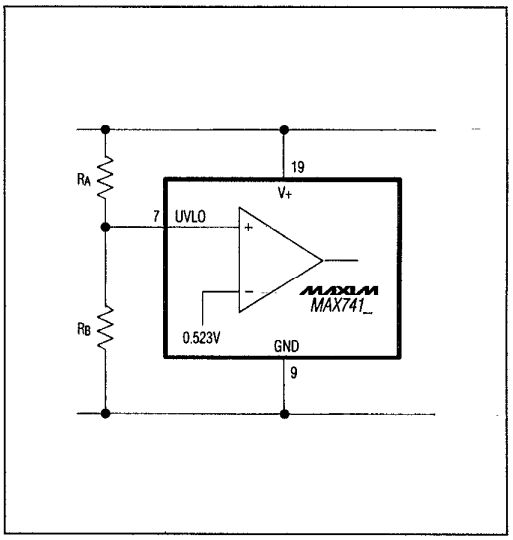

Figure 5. Undervoltage Lockout Comparator (Adjustable Mode)

Undervoltage Lockout

Switching with low gate-drive to the power MOSFET results in low efficiency and can cause excessive heating of the switching transistor. Undervoltage lockout inhibits switching activity while the supply voltage is low. When lockout is triggered, the output power FETs are disabled and the SS pin is internally pulled to GND.

There are three undervoltage lockout modes: disabled, fixed at +4V, and adjustable. Connect UVLO to V+ to disable the undervoltage lockout. Connect UVLO to GND to trigger lockout at 4V or less. Undervoltage is adjustable when the voltage applied to the UVLO pin is between (0.075)(V+) and (0.47)(V+). In adjustable mode, the UVLO pin lockout threshold is nominally 0.523V. Connect a resistor-divider network from V+ to UVLO to GND as shown in Figure 5. The nominal undervoltage lockout voltage is

$$V+ = \frac{(0.523)\,(R_A + R_B)}{R_B}$$

Values for R_A and R_B can range from 10kΩ to 100k, since UVLO is a high-impedance input with leakage currents under 1µA. For example, connect an 82kΩ resistor from V+ to UVLO (R_A), and a 10kΩ resistor from UVLO to GND (R_B) to achieve a nominal 4.81V lockout-voltage threshold.

These calculations define the undervoltage-lockout threshold when V+ is rising from a low value. Hysteresis built into the MAX741 provides a UVLO threshold voltage typically 6% lower when V+ is falling from above the undervoltage-lockout threshold.

SYNC Input/Output Clock

The SYNC output typically drives up to five CMOS gates. Capacitive loading of this pin lowers the internal oscillator frequency. When driven by an external gate, SYNC becomes an input. The clock source must have 1mA source and sink capability. Standard +5V CMOS logic can easily drive this pin, as long as the logic supply voltage does not exceed V+. If V+ drops below +5V, buffer the SYNC input signal with a CMOS logic gate with its supply rails connected to GND and V+.

Externally Synchronizing the Switching Frequency

To synchronize the switching frequency to an external clock, apply the clock to the SYNC pin. This signal's duty cycle controls the maximum duty cycle of OUTA or OUTB (the high portion of the clock controls the minimum off-time). A 20% duty cycle clock signal applied at SYNC, for example, forces a minimum of 20% off-time for the MOSFET driven by OUTA or OUTB. Therefore, for most applications, it is appropriate to clock SYNC with a duty cycle of approximately 10% (a series of short pulses at the desired switching frequency) allowing OUTA and OUTB to achieve duty cycles of up to 90%.

Application Circuits

Low-Voltage Step-Up Converter

Figure 7 shows a 3V to 5V step-up (or boost) converter capable of delivering 1A. Bootstrapped operation provides efficiencies between 80% and 90%, depending on the load current and the input voltage. At light loads, the MAX741U enters discontinuous-conduction "burst-mode" operation, in which inductor currents may staircase before discharging into the output capacitor. The resulting output voltage ripple may be higher than CCM noise (up to 100mV), and subharmonics of the fundamental switching frequency will be present. With heavier loads, the MAX741U enters CCM, giving lower noise performance, see *Typical Operating Characteristics*.

This circuit's output can be turned on and off with an open-drain logic signal applied to the ON/$\overline{OFF}$ control. In the off state, the output remains connected to the input via inductor L1 and diode D1. The ON/$\overline{OFF}$ control should be taken below 0.5V to turn the circuit off, or left open to turn it on. Do not apply a voltage to the ON/$\overline{OFF}$ control that exceeds the circuit's output voltage.

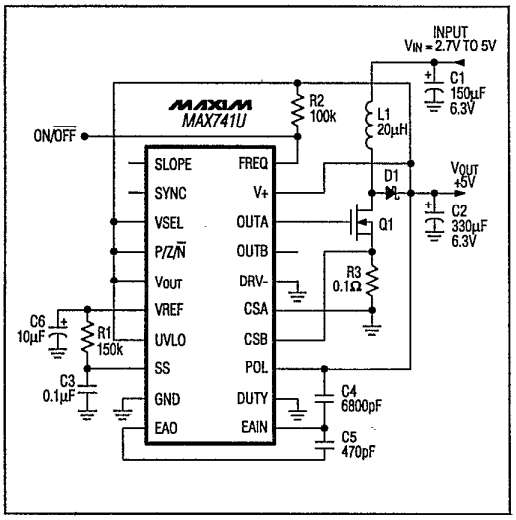

Figure 6. MAX741U EV Kit Schematic. This step-up converter supplies +5V at 1A from a +3V input.

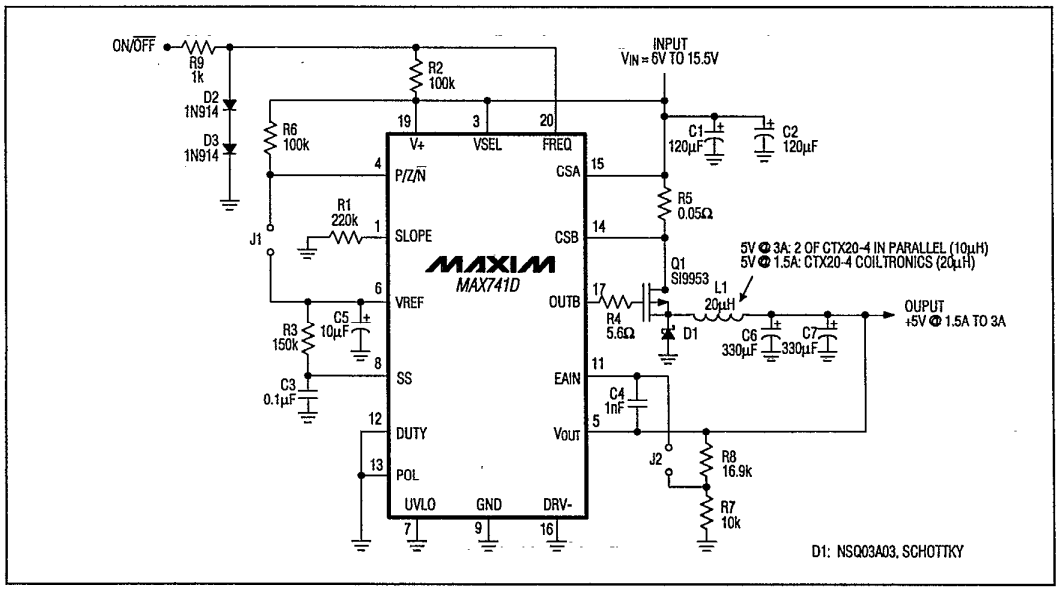

Figure 7. MAX741D EV Kit Schematic. +6V to +15.5V Input Step-Down Converter Supplies +5V at 1.5A or 3A.

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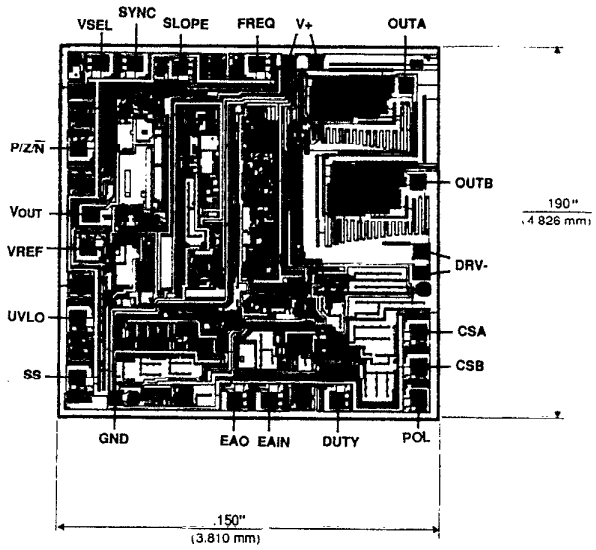
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX741DCPP	0°C to +70°C	20 Plastic DIP
MAX741DCAP	0°C to +70°C	20 SSOP
MAX741DC/D	0°C to +70°C	Dice*
MAX741DEPP	-40°C to +85°C	20 Plastic DIP
MAX741DEAP	-40°C to +85°C	20 SSOP
MAX741DMJP	-55°C to +125°C	20 CERDIP**
MAX741NCPP	0°C to +70°C	20 Plastic DIP
MAX741NCAP	0°C to +70°C	20 SSOP
MAX741NC/D	0°C to +70°C	Dice*
MAX741NEPP	-40°C to +85°C	20 Plastic DIP
MAX741NEAP	-40°C to +85°C	20 SSOP
MAX741NMJP	-55°C to +125°C	20 CERDIP**
MAX741D EVKIT-SO	0°C to +70°C	Surface-Mount
MAX741U EVKIT-SO	0°C to +70°C	Surface-Mount

** Dice are tested at T_A = +25°C only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



TRANSISTOR COUNT: 614
SUBSTRATE CONNECTED TO V+.