19-2312; Rev 1; 6/02

MAXIM

2-Wire Interfaced, 2.7V to 5.5V, 4-Digit 5 × 7 Matrix LED Display Driver

General Description

The MAX6953 is a compact cathode-row display driver that interfaces microprocessors to 5 × 7 dot-matrix LED displays through an I²C™-compatible serial interface. The MAX6953 drives up to four digits (140 LEDs).

Included on-chip are an ASCII 104-character font, multiplex scan circuitry, column and row drivers, and static RAM that stores each digit, as well as font data for 24 user-definable characters. The segment current for the LEDs is set by an internal digit-by-digit digital brightness control.

The device includes a low-power shutdown mode, segment blinking (synchronized across multiple drivers, if desired), and a test mode that forces all LEDs on. The LED drivers are slew-rate limited to reduce EMI.

For an SPI™-compatible version, refer to the MAX6952 data sheet. An EV kit is available for the MAX6952.

Applications

Message Boards

Medical Equipment

Industrial Displays

Audio/Video Equipment

Gaming Machines

Features

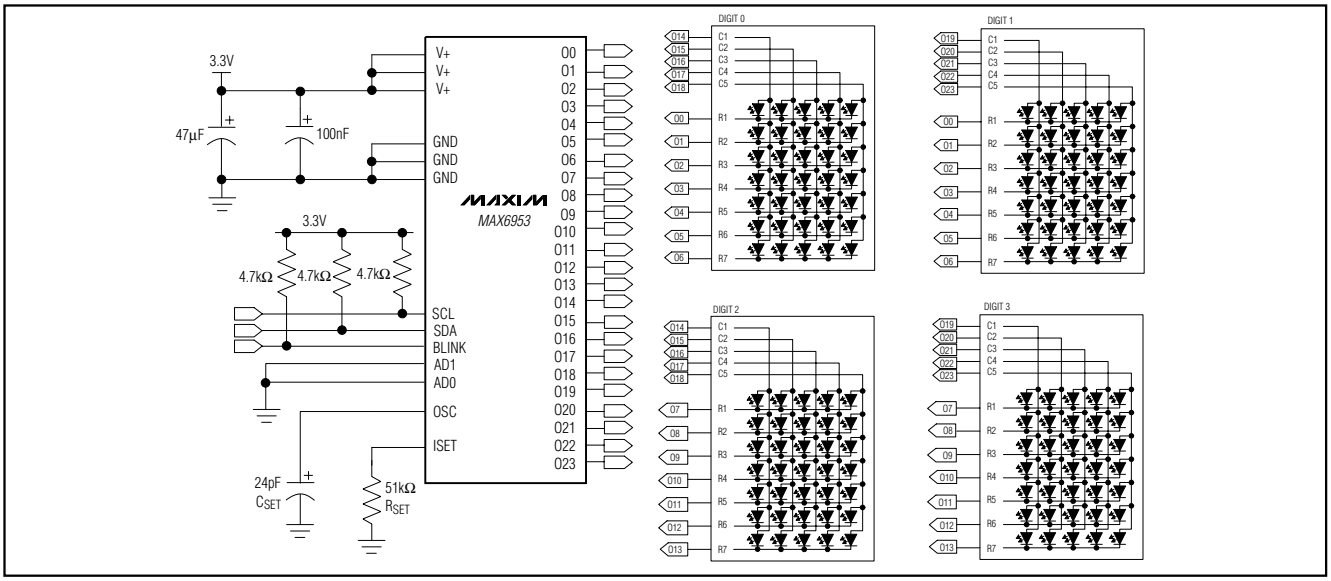
- ♦ **400kbps 2-Wire Interface Compatible with I²C**
- ♦ **2.7V to 5.5V Operation**
- ♦ **Drives 4 Monocolor or 2 Bicolor Cathode-Row 5 × 7 Matrix Displays**
- ♦ **Built-In ASCII 104-Character Font**
- ♦ **24 User-Definable Characters Available**
- ♦ **Automatic Blinking Control for Each Segment**
- ♦ **70µA Low-Power Shutdown (Data Retained)**
- ♦ **16-Step Digital Brightness Control**
- ♦ **Display Blanked on Power-Up**
- ♦ **Slew-Rate-Limited Segment Drivers for Lower EMI**
- ♦ **36-Pin SSOP and 40-Pin DIP Packages**
- ♦ **Extended Temperature Range as Standard**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6953EAX	-40°C to +85°C	36 SSOP
MAX6953EPL	-40°C to +85°C	40 PDIP

Pin Configurations appear at end of data sheet.

Typical Application Circuit



I²C is a trademark of Philips Corp.

SPI is a trademark of Motorola, Inc.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

2-Wire Interfaced, 2.7V to 5.5V, 4-Digit 5 × 7 Matrix LED Display Driver

ABSOLUTE MAXIMUM RATINGS

Voltage (with Respect to GND)
V+ .....-0.3V to +6V
All Other Pins.....-0.3V to (V+ + 0.3V)
O0–O13 Sink Current..... 500mA
O14–O23 Source Current 50mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin SSOP (derate 11.8mW/°C above +70°C) 941.2mW
40-Pin PDIP (derate 16.7mW/°C above +70°C).....1333mW

Operating Temperature Range
MAX6953E .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Typical operating circuit, V+ = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Shutdown mode, all digital inputs at V+ or GND	T_A = T_{MIN} to T_{MAX}			130	µA
			T_A = +25°C		70	100	
Operating Supply Current	I+	All segments on, intensity set to full, internal oscillator, no display load connected, BLINK open circuit			12	15	mA
Master Clock Frequency (OSC Internal Oscillator)	f_{OSC}	OSC = RC oscillator, R_{SET} = 51kΩ, C_{SET} = 24pF			4		MHz
Master Clock Frequency (OSC External Clock)	f_{OSC}	OSC overdriven externally		1		8	MHz
Dead Clock Protection Frequency	f_{OSC}				90		kHz
OSC Internal/External Detection Threshold	V_{OSC}				1.7		V
OSC High Time	t_{CH}			50			ns
OSC Low Time	t_{CL}			50			ns
Slow Segment Blink Period (OSC Internal Oscillator)	$f_{SLOWBLINK}$	OSC = RC oscillator, R_{SET} = 51kΩ, C_{SET} = 24pF			1		s
Fast Segment Blink Period (OSC Internal Oscillator)	$f_{FASTBLINK}$	OSC = RC oscillator, R_{SET} = 51kΩ, C_{SET} = 24pF			0.5		s
Fast or Slow Segment Blink Duty Cycle (Note 2)				49.5		50.5	%
Column Drive Source Current	I_{COLUMN}	V_{LED} = 2.4V, V+ = 3.0V		-30.5		-58.5	mA

DC ELECTRICAL CHARACTERISTICS (continued)

(Typical operating circuit, V+ = 3.0V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Current Slew Rate	$\Delta I_{SEG}/\Delta t$	T_A = +25°C		12.5		mA/µs
Segment Drive Current Matching (Within IC)	ΔI_{SEG}	T_A = +25°C		4		%
LOGIC INPUTS						
Input High Voltage SDA, SCL, AD0, AD1	V_{IH}		0.7 x V+			V
Input Low Voltage SDA, SCL, AD0, AD1	V_{IL}				0.3 × V+	V
Input Hysteresis SDA, SCL, AD0, AD1	V_{HYST}			0.05 × V+		V
Input Leakage Current	I_{IL}, I_{IH}		-2		2	µA
Input Capacitance	C_I			10		pF
DIGITAL OUTPUT						
SDA Output Low Voltage	V_{OLSDA}	I_{SINK} = 4mA			0.4	V
BLINK Output Low Voltage	V_{OLBK}	I_{SINK} = 1.6mA			0.4	V

MAX6953 TIMING CHARACTERISTICS

(V+ = 2.7V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 3)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.6			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 2, 4)		20 + 0.1C_B	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 2, 4)		20 + 0.1C_B	300	ns

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MAX6953 TIMING CHARACTERISTICS (continued)

(V+ = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

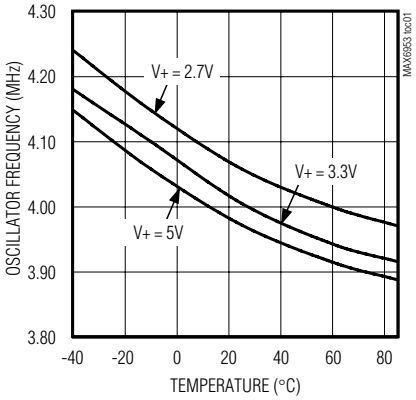
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time of SDA Transmitting	t_F	(Notes 2, 5)		20 + 0.1C_B	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 6)	0	50		ns
Capacitive Load for Each Bus Line	C_B	(Note 2)		400		pF

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 4: C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 5: $I_{SINK} \le 6mA$. C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 6: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

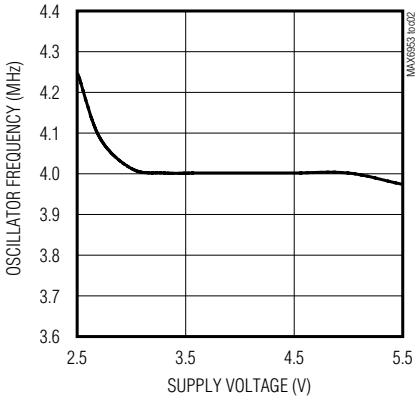
Typical Operating Characteristics

(Typical application circuit, V+ = 3.3V, LED forward voltage = 2.4V, scan limit set to 4 digits, T_A = +25°C, unless otherwise noted.)

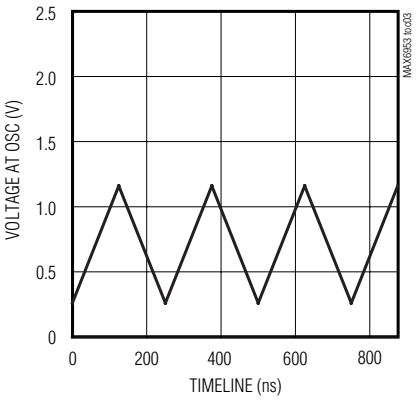
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



INTERNAL OSCILLATOR WAVEFORM AT OSC (PIN 19 OR 21)

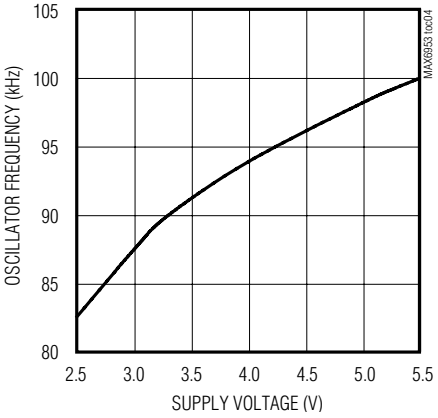


2-Wire Interfaced, 2.7V to 5.5V, 4-Digit 5 × 7 Matrix LED Display Driver

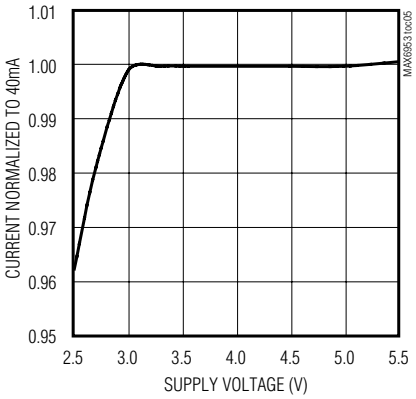
Typical Operating Characteristics (continued)

(Typical application circuit, V+ = 3.3V, LED forward voltage = 2.4V, scan limit set to 4 digits, T_A = +25°C, unless otherwise noted.)

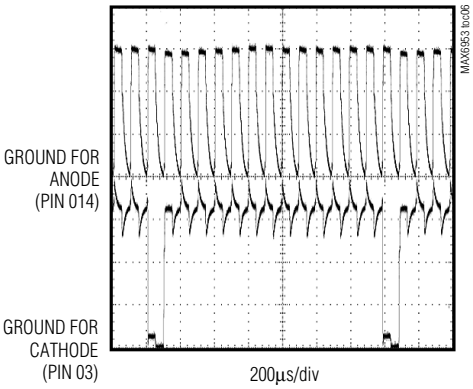
DEAD CLOCK OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE



WAVEFORMS AT O2 (PIN 3) AND O14 (PIN 28) V+ = 3.3V, 8/16 INTENSITY



Pin Description

PIN		NAME	FUNCTION
SSOP	PDIP		
1, 2, 3, 6–14, 23, 24	1, 2, 3, 7–15, 26, 27	O0 to O13	LED Cathode Drivers. O0 to O13 outputs sink current from the display's cathode rows.
4, 5, 17	4, 5, 6, 19	GND	Ground
15	17	ISET	Segment Current Setting. Connect ISET to GND through series resistor R_{SET} to set the peak current.
16	18	AD1	Address Input 1. Sets device slave address. Connect to either GND, V+, SCL, SDA to give four logic combinations. See Table 3.
—	16, 25	N.C.	Not Connected
18	20	BLINK	Blink Output. Output is open drain.
19	21	OSC	Multiplex Clock Input. To use internal oscillator, connect capacitor C_{SET} from OSC to GND. To use external clock, drive OSC with a 1MHz to 8MHz CMOS clock.
20	22	AD0	Address Input 0. Sets device slave address. Connect to either GND, V+, SCL, SDA to give four logic combinations. See Table 3.
21	23	SDA	I^2C-Compatible Serial Data I/O
22	24	SCL	I^2C-Compatible Serial Clock Input
25–31, 34, 35, 36	28–34, 38, 39, 40	O14 to O23	LED Anode Drivers. O14 to O23 outputs source current to the display's anode columns.
32, 33	35, 36, 37	V+	Positive Supply Voltage. Bypass V+ to GND with a 47µF bulk capacitor and a 0.1µF ceramic capacitor.

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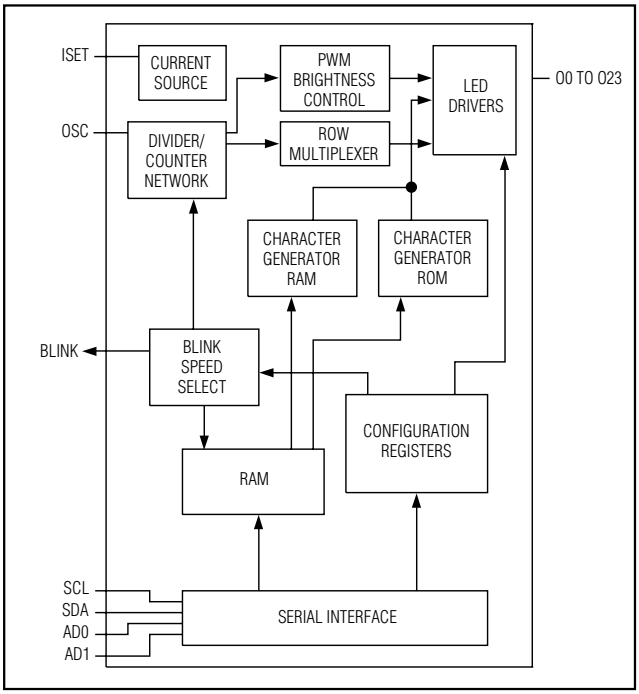

Figure 1. MAX6953 Functional Diagram

Detailed Description

The MAX6953 is a serially interfaced display driver that can drive four digits of 5 × 7 cathode-row dot-matrix displays. The MAX6953 can drive either four monocolor digits (Table 1) or two bicolor digits (Table 2). The MAX6953 includes a 128-character font map comprising 104 predefined characters and 24 user-definable characters. The predefined characters follow the Arial font, with the addition of the following common symbols: £, <, ¥, °, µ, ±, ↑, and ↓. The 24 user-definable characters are uploaded by the user into on-chip RAM through the serial interface and are lost when the device is powered down. Figure 1 is the MAX6953 functional diagram.

Serial Interface

Serial Addressing

The MAX6953 operates as a slave that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX6953, and generates the SCL clock that synchronizes the data transfer (Figure 2).

The MAX6953 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on the SDA. The MAX6953 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX6953 7-bit slave address plus R/$\overline{W}$ bit (Figure 6), a register address byte, 1 or more data bytes, and finally a STOP condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning the SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Table 1. Connection Scheme for Four Monocolor Digits

DIGIT	O0–O6	O7–O13	O14–O18	O19—O23
1	Digit 0 rows (cathodes) R1 to R7 Digit 1 rows (cathodes) R1 to R7	—	Digit 0 columns (anodes) C1 to C5	Digit 1 columns (anodes) C6 to C10
2	—	Digit 2 rows (cathodes) R1 to R7 Digit 3 rows (cathodes) R1 to R7	Digit 2 columns (anodes) C1 to C5	Digit 3 columns (anodes) C6 to C10

Table 2. Connection Scheme for Two Bicolor Digits

DIGIT	O0–O6	O7–O13	O14–023	
1	Digit 0 rows (cathodes) R1 to R14	—	Digit 0 columns (anodes) C1 to C10	
			- the 5 green anodes -	- the 5 red anodes -
2	—	Digit 1 rows (cathodes) R1 to R14	Digit 1 columns (anodes) C1 to C10	
			- the 5 green columns -	- the 5 red anodes -

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX6953, the MAX6953 generates the acknowledge bit because the MAX6953 is the recipient. When the MAX6953 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX6953 has a 7-bit-long slave address (Figure 6). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, high for a read command.

The first 3 bits (MSBs) of the MAX6953 slave address are always 101. Slave address bits A3, A2, A1, and A0 are selected by the address input pins AD1 and AD0. These two input pins may be connected to GND, V+, SDA, or SCL. The MAX6953 has 16 possible slave addresses (Table 3) and therefore a maximum of 16 MAX6953 devices may share the same interface.

Message Format for Writing

A write to the MAX6953 comprises the transmission of the MAX6953's slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte, which determines which register of the MAX6953 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, then the MAX6953 takes no further action (Figure 7) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX6953 selected by the command byte (Figure 8).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX6953 internal registers because the command byte address generally autoincrements (Table 4) (Figure 9).

Message Format for Reading

The MAX6953 is read using the MAX6953's internally stored command byte as address pointer, the same way the stored command byte is used as address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 4). Thus, a read is initiated by first configuring the MAX6953's command byte by performing a write (Figure 7). The master can now read n consecutive bytes from the MAX6953, with the first data byte being read from the register addressed by the initialized command byte (Figure 9). When performing

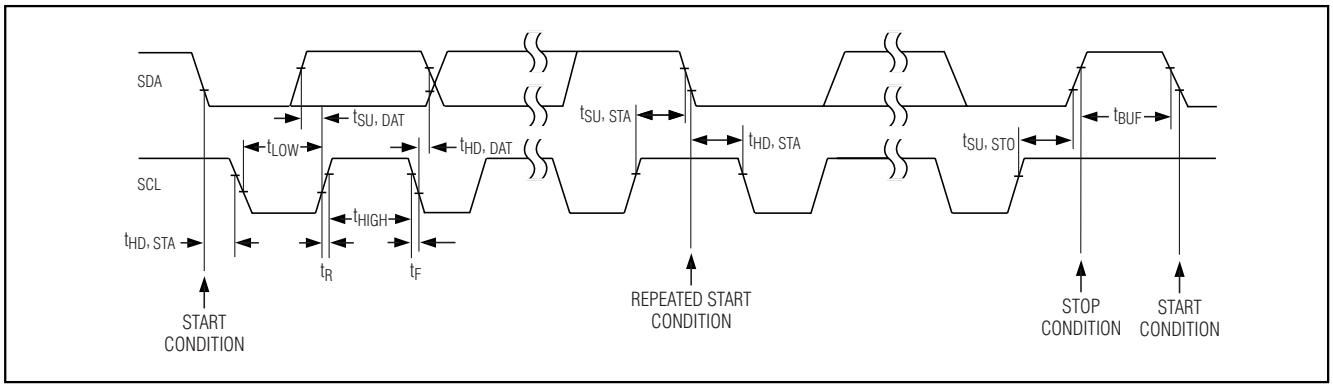

Figure 2. 2-Wire Serial Interface Timing Details

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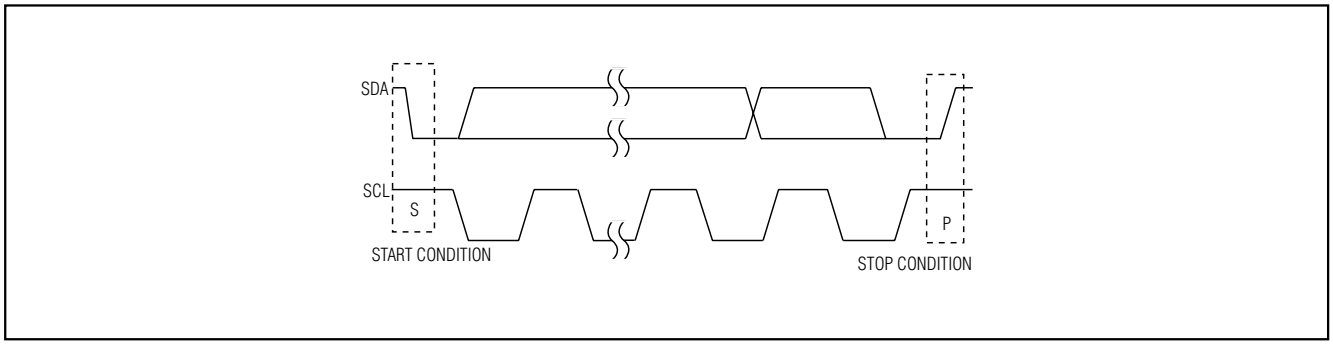

Figure 3. Start and Stop Conditions

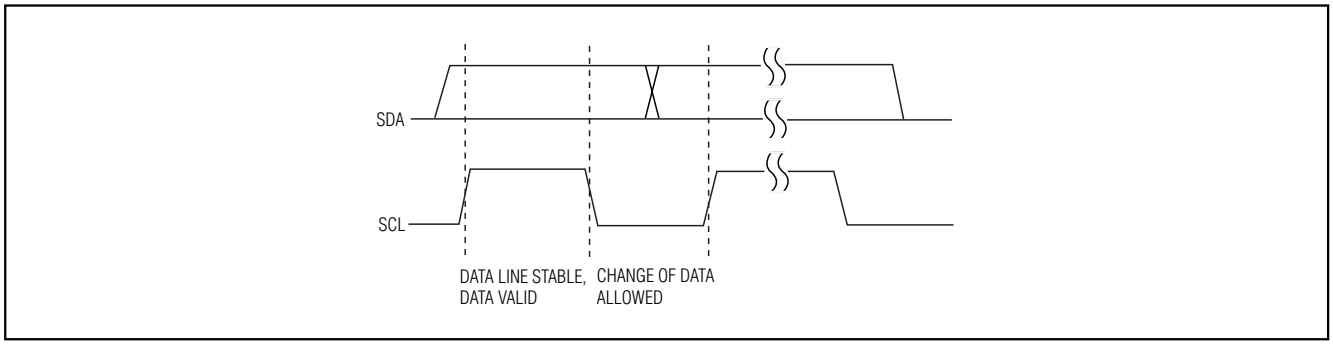

Figure 4. Bit Transfer

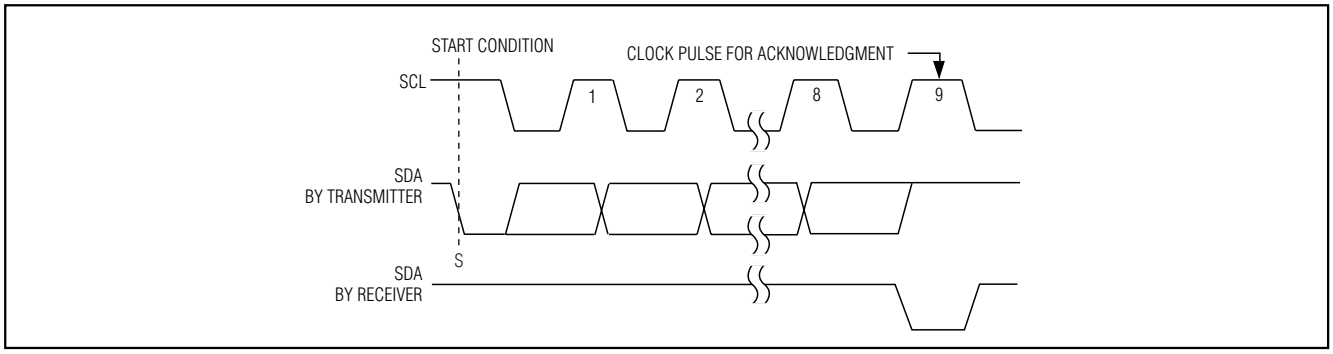

Figure 5. Acknowledge

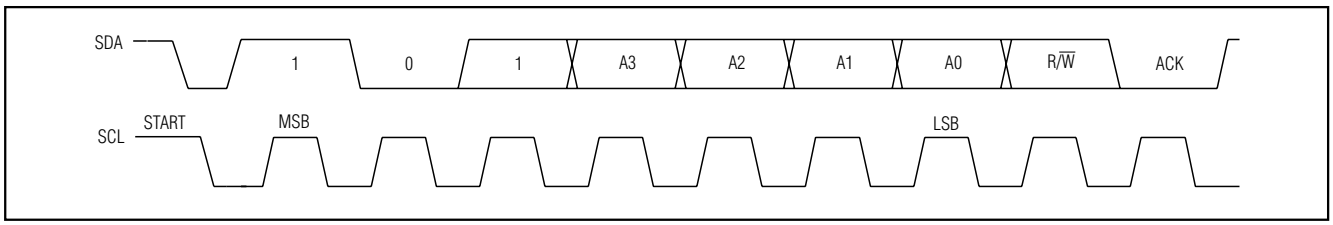

Figure 6. Slave Address

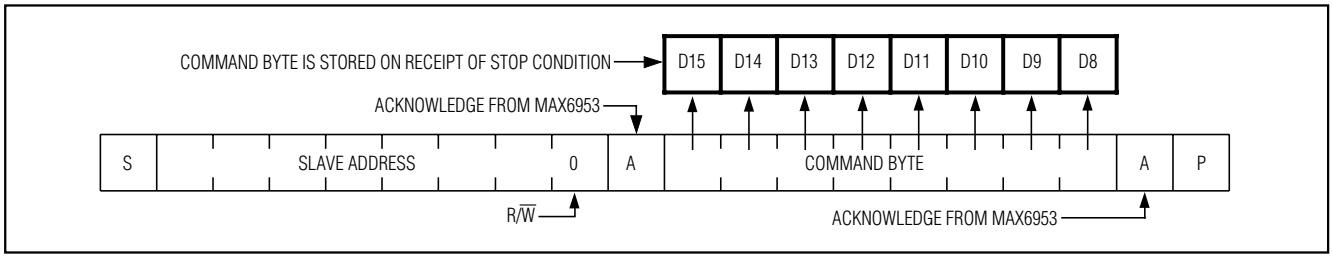

Figure 7. Command Byte Received

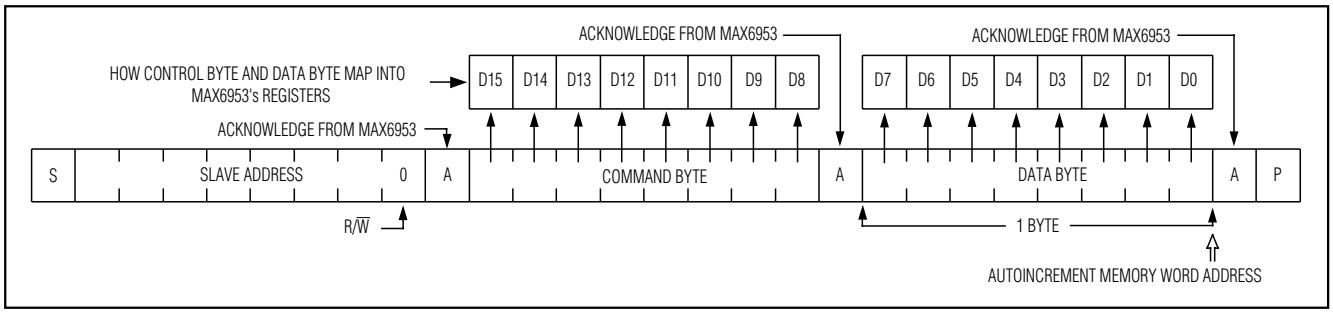

Figure 8. Command and Single Data Byte Received

read-after-write verification, reset the command byte's address because the stored byte address generally is autoincremented after the write (Table 4).

Operation with Multiple Masters

If the MAX6953 is operated on a 2-wire interface with multiple masters, a master reading the MAX6953 should use a repeated start between the write, which sets the MAX6953's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX6953's address pointer but before master 1 has read the data. If master 2 subsequently changes the MAX6953's address pointer, then master 1's delayed read may be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the MAX6953 to be configured with the shortest number of transmissions by minimizing the number of times the command byte needs to be sent. The command address or the font pointer address stored in the MAX6953 generally increments after each data byte is written or read (Table 4).

Digit Registers

The MAX6953 uses eight digit registers to store the characters that the user wishes to display on the four 5 × 7 LED digits. These digit registers are implemented with two planes of 4 bytes, called P0 and P1. Each LED digit is represented by 2 bytes of memory, 1 byte in plane P0 and the other in plane P1. The digit registers are mapped so that a digit's data can be updated in plane P0, or plane P1, or both planes at the same time (Table 5).

If the blink function is disabled through the Blink Enable Bit E (Table 10) in the configuration register, then the digit register data in plane P0 is used to multiplex the display. The digit register data in P1 is not used. If the blink function is enabled, then the digit register data in both plane P0 and plane P1 are alternately used to multiplex the display. Blinking is achieved by multiplexing the LED display using data planes P0 and P1 on alternate phases of the blink clock (Table 11).

The data in the digit registers does not control the digit segments directly. Instead, the register data is used to address a character generator, which stores the data of a 128-character font (Table 15). The lower 7 bits of the digit data (D6 to D0) select the character from the font. The most-significant bit of the register data (D7) selects whether the font data is used directly (D7 = 0) or whether the font data is inverted (D7 = 1). The inversion feature can be used to enhance the appearance of bicolor displays by displaying, for example, a red character on a green background.

Display Blink Mode

The display blinking facility, when enabled, makes the driver flip automatically between displaying the digit register data in planes P0 and P1. If the digit register data for any digit is different in the two planes, then that

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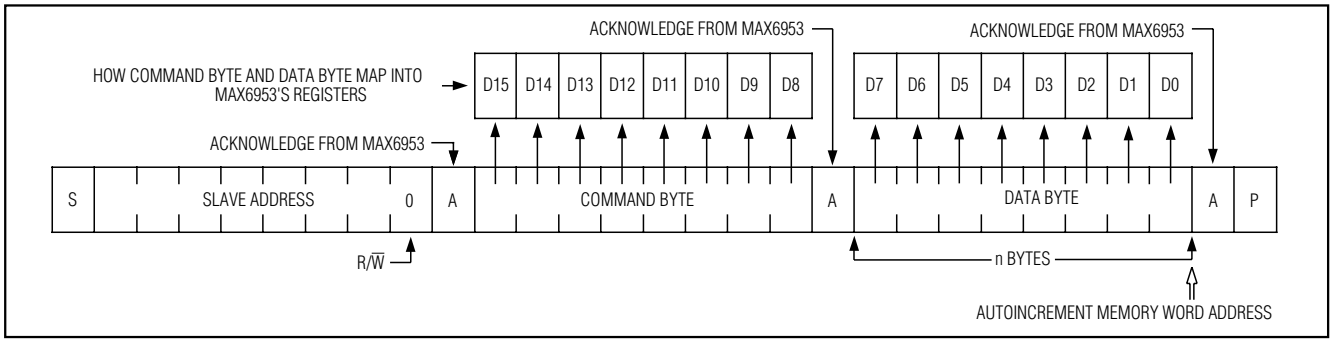

Figure 9. n Data Bytes Received

digit appears to flip between two characters. To make a character appear to blink on or off, write the character to one plane, and use the blank character (0x20) for the other plane. Once blinking has been configured, it continues automatically without further intervention.

Blink Speed

The blink speed is determined by frequency of the multiplex clock, OSC, and by setting the Blink Rate Selection Bit B (Table 9) in the configuration register. The Blink Rate Selection Bit B sets either fast or slow blink speed for the whole display.

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, intensities are set to minimum, and shutdown is enabled (Table 6).

Configuration Register

The configuration register is used to enter and exit shutdown, select the blink rate, globally enable and disable the blink function, globally clear the digit data, and reset the blink timing (Table 7).

Shutdown Mode (S Data Bit D0) Format

The S bit in the configuration register selects shutdown or normal operation. The display driver can be programmed while in shutdown mode, and shutdown mode is overridden when in the display test mode. For normal operation, the S bit should be set to 1 (Table 8).

Blink Rate Selection (B Data Bit D2) Format

The B bit in the configuration register selects the blink rate. This is the speed that the segments alternate between plane P0 and plane P1 refresh data. The blink rate is determined by the frequency of the multiplex clock OSC, in addition to the setting of the B bit (Table 9).

Table 3. MAX6953 Address Map

PIN		DEVICE ADDRESS						
AD1	AD0	A6	A5	A4	A3	A2	A1	A0
GND	GND	1	0	1	0	0	0	0
GND	V+	1	0	1	0	0	0	1
GND	SDA	1	0	1	0	0	1	0
GND	SCL	1	0	1	0	0	1	1
V+	GND	1	0	1	0	1	0	0
V+	V+	1	0	1	0	1	0	1
V+	SDA	1	0	1	0	1	1	0
V+	SCL	1	0	1	0	1	1	1
SDA	GND	1	0	1	1	0	0	0
SDA	V+	1	0	1	1	0	0	1
SDA	SDA	1	0	1	1	0	1	0
SDA	SCL	1	0	1	1	0	1	1
SCL	GND	1	0	1	1	1	0	0
SCL	V+	1	0	1	1	1	0	1
SCL	SDA	1	0	1	1	1	1	0
SCL	SCL	1	0	1	1	1	1	1

Table 4. Command Address Autoincrement Rules

COMMAND BYTE ADDRESS RANGE	AUTOINCREMENT BEHAVIOR
x0000000 to x0000100	Command byte address autoincrements after byte read or written.
x0000101	Command byte address remains at x0000101 after byte read or written, but the font address pointer autoincrements.
x0000110	Factory reserved; do not write to this register.
x000111 to x1111110	Command byte address autoincrements after byte read or written.
x1111111	Command byte address remains at x1111111 after byte read or written.

Table 5. Register Address Map

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	—
No-Op	X	0	0	0	0	0	0	0	0x00
Intensity10	X	0	0	0	0	0	0	1	0x01
Intensity32	X	0	0	0	0	0	1	0	0x02
Scan Limit	X	0	0	0	0	0	1	1	0x03
Configuration	X	0	0	0	0	1	0	0	0x04
User-Defined Fonts	X	0	0	0	0	1	0	1	0x05
Factory Reserved. Do not write to this.	X	0	0	0	0	1	1	0	0x06
Display Test	X	0	0	0	0	1	1	1	0x07
Digit 0 Plane P0	X	0	1	0	0	0	0	0	0x20
Digit 1 Plane P0	X	0	1	0	0	0	0	1	0x21
Digit 2 Plane P0	X	0	1	0	0	0	1	0	0x22
Digit 3 Plane P0	X	0	1	0	0	0	1	1	0x23
Digit 0 Plane P1	X	1	0	0	0	0	0	0	0x40
Digit 1 Plane P1	X	1	0	0	0	0	0	1	0x41
Digit 2 Plane P1	X	1	0	0	0	0	1	0	0x42
Digit 3 Plane P1	X	1	0	0	0	0	1	1	0x43
Write Digit 0 Planes P0 and P1 with Same Data (Reads as 0x00)	X	1	1	0	0	0	0	0	0x60
Write Digit 1 Planes P0 and P1 with Same Data (Reads as 0x00)	X	1	1	0	0	0	0	1	0x61
Write Digit 2 Planes P0 and P1 with Same Data (Reads as 0x00)	X	1	1	0	0	0	1	0	0x62
Write Digit 3 Planes P0 and P1 with Same Data (Reads as 0x00)	X	1	1	0	0	0	1	1	0x63

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Table 6. Initial Power-Up Register Status

REGISTER	POWER-UP CONDITION	ADDRESS CODE (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Intensity10	1/16 (min on)	0x01	0	0	0	0	0	0	0	0
Intensity32	1/16 (min on)	0x02	0	0	0	0	0	0	0	0
Scan Limit	Display 4 digits: 0 1 2 3	0x03	X	X	X	X	X	X	X	1
Configuration	Shutdown enabled, blink speed is slow, blink disabled	0x04	0	X	0	0	0	0	X	0
User-Defined Font Address Pointer	Address 0x80; pointing to the first user-defined font location	0x05	1	0	0	0	0	0	0	0
Display Test	Normal operation	0x07	X	X	X	X	X	X	X	0
Digit 0 Plane P0	Blank digit (0x20)	0x20	0	0	1	0	0	0	0	0
Digit 1 Plane P0	Blank digit (0x20)	0x21	0	0	1	0	0	0	0	0
Digit 2 Plane P0	Blank digit (0x20)	0x22	0	0	1	0	0	0	0	0
Digit 3 Plane P0	Blank digit (0x20)	0x23	0	0	1	0	0	0	0	0
Digit 0 Plane P1	Blank digit (0x20)	0x40	0	0	1	0	0	0	0	0
Digit 1 Plane P1	Blank digit (0x20)	0x41	0	0	1	0	0	0	0	0
Digit 2 Plane P1	Blank digit (0x20)	0x42	0	0	1	0	0	0	0	0
Digit 3 Plane P1	Blank digit (0x20)	0x43	0	0	1	0	0	0	0	0

Table 7. Configuration Register Format

	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Configuration Register	P	X	R	T	E	B	X	S

Table 8. Shutdown Control (S Data Bit D0) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode	P	X	R	T	E	B	X	0
Normal Operation	P	X	R	T	E	B	X	1

Table 9. Blink Rate Selection (B Data Bit D2) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Slow blinking (segments are refreshed using plane P0 for 1s, plane P1 for 1s, for OSC = 4MHz).	P	X	R	T	E	0	X	S
Fast blinking (segments are refreshed using plane P0 for 0.5s, plane P1 for 0.5s, for OSC = 4MHz).	P	X	R	T	E	1	X	S

Table 10. Global Blink Enable/Disable (E Data Bit D3) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Blink function is disabled.	P	X	R	T	0	B	X	S
Blink function is enabled.	P	X	R	T	1	B	X	S

Table 11. Digit Register Mapping with Blink Globally Enabled

SEGMENT'S BIT SETTING IN PLANE P1	SEGMENT'S BIT SETTING IN PLANE P0	SEGMENT BEHAVIOR
0	0	Segment off
0	1	Segment on only during the 1st half of each blink period
1	0	Segment on only during the 2nd half of each blink period
1	1	Segment on

Global Blink Enable/Disable (E Data Bit D3) Format

The E bit globally enables or disables the blink feature of the device (Table 10). When blink is globally enabled, then the digit data in both planes P0 and P1 are used to control the display (Table 11).

When blink is globally disabled, then only the digit data in plane P0 is used to control the display. The digit data in plane P1 is ignored.

Global Blink Timing Synchronization (T Data Bit D4) Format

By setting the T bit in multiple MAX6953s at the same time (or in quick succession), the blink timing can be synchronized across all the devices (Table 12). Note that the display multiplexing sequence is also reset, which might give rise to a one-time display flicker when the register is written.

Table 12. Global Blink Timing Synchronization (T Data Bit D4) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Blink timing counters are unaffected.	P	X	R	0	E	B	X	S
Blink timing counters are reset during the I^2C acknowledge.	P	X	R	1	E	B	X	S

Table 13. Global Clear Digit Data (R Data Bit D5) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Digit data for both planes P0 and P1 are unaffected.	P	X	0	T	E	B	X	S
Digit data for both planes P0 and P1 are cleared during I^2C acknowledge.	P	X	1	T	E	B	X	S

Table 14. Blink Phase Readback (P Data Bit D7) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
P1 blink phase	0	X	R	T	E	B	X	S
P0 blink phase	1	X	R	T	E	B	X	S

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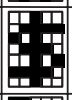
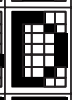
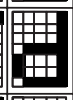
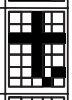
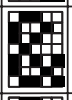
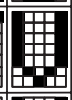
Table 15. Character Map

MSB / LSB	x000	x001	x010	x011	x100	x101	x110	x111
0000	RAM00	RAM16						
0001	RAM01	RAM17						
0010	RAM02	RAM18						
0011	RAM03	RAM19						
0100	RAM04	RAM20						
0101	RAM05	RAM21						
0110	RAM06	RAM22						
0111	RAM07	RAM23						
1000	RAM08							
1001	RAM09							
1010	RAM10							
1011	RAM11							
1100	RAM12							
1101	RAM13							
1110	RAM14							
1111	RAM15							

Global Clear Digit Data (R Data Bit D5) Format

When global digit data clear is set, the digit data for both planes P0 and P1 for all digits are cleared during the acknowledge (Table 13).

Blink Phase Readback (P Data Bit D7) Format

When the configuration register is read, the P bit reflects the state of the blink output pin at that time (Table 14).

Character Generator Font Mapping

The font is a 5 × 7 matrix comprising 104 characters in ROM, and 24 user-definable characters. The selection from the total of 128 characters is represented by the lower 7 bits of the 8-bit digit registers. The most-significant bit, shown as x in the ROM map, is zero to light LEDs as shown by the black segments in Table 15, and 1 to display the inverse.

The character map follows the Arial font for 96 characters in the range 0x0101000 through x1111111. The first 32 characters map the 24 user-definable positions (RAM00 to RAM23), plus eight extra common characters in ROM.

User-Defined Fonts

The 24 user-definable characters are represented by 120 entries of 7-bit data, five entries per character, and are stored in MAX6953's internal RAM.

The 120 user-definable font data entries are written and read through a single register, address 0x05. An autoincrementing font address pointer in the MAX6953 indirectly accesses the font data. The font address pointer can be written, setting one of 120 addresses between 0x00 and 0xF7, but cannot be read back. The font data is written to and read from MAX6953 indirectly, using this font address pointer. Unused font locations can be used as general-purpose scratch RAM, bearing in mind that the font registers are only 7 bits wide, not 8.

Table 16 shows how the single user-defined font register 0x05 is used to set the font address pointer, write font data, and read font data. A read action always returns font data from the font address pointer position. A write action sets the 7-bit font address pointer if the MSB is set, or writes 7-bit font data to the font address pointer position if the MSB is clear.

The font address pointer autoincrements after a valid access to the user-definable font data. Autoincrementing allows the 120 font data entries to be written and read back very quickly because the font pointer address need only be set once. When the last data location 0xF7 is written, the font address pointer autoincrements to address 0x80. If the font address pointer is

Table 16. Memory Mapping of User-Defined Font Register 0x05

ADDRESS CODE (HEX)	REGISTER DATA	I²C READ OR WRITE	FUNCTION
0x05	0x00–0x7F	Read	Read 7-bit user-definable font data entry from current font address. MSB of the register data is clear. Font address pointer is incremented after the read.
0x05	0x00–0x7F	Write	Write 7-bit user-definable font data entry to current font address. Font address pointer is incremented after the write.
0x05	0x80–0xFF	Write	Write font address pointer with the register data.

Table 17. Font Pointer Address Behavior

FONT POINTER ADDRESS	ACTION
0x80 to 0xF6	Valid range to set the font address pointer. Pointer autoincrements after a font data read or write, while pointer address remains in this range.
0xF7	Font address resets to 0x80 after a font data read or write to this pointer address.
0xF8 to 0xFF	Invalid range to set the font address pointer. Pointer is set to 0x80 if address.

set to an out-of-range address by writing data in the 0xF8 to 0xFF range, then address 0x80 is set instead (Table 17).

Table 18 shows the user-definable font pointer base addresses.

Table 19 shows an example of data (characters 0, 1, and 2) being stored in the first three user-defined font locations, illustrating the orientation of the data bits.

Table 20 shows the six sequential write commands required to set a MAX6953's font character RAM02 with the data to display character 2 given in the font RAM illustration above.

Multiplex Clock and Blink Timing

The OSC pin can be fitted with capacitor C_{SET} to GND (to use the internal RC multiplex oscillator), or driven by an external clock. The multiplex clock frequency determines the multiplex scan rate and the blink timing. The display scan rate (the frequency that the complete four-digit display is updated) is calculated by dividing the frequency at OSC by 5600. With OSC at 4MHz, each digit row is enabled for 100µs, and the display scan rate is 714.29Hz.

The on-chip oscillator may be accurate enough for applications using a single device. If an exact blink rate is required, use an external clock ranging between 1MHz and 8MHz to drive OSC. The OSC inputs of multiple MAX6953s can be tied together to a common external clock to make the devices blink at the same rate. The relative blink phasing of multiple MAX6953s can be synchronized by setting the T bit in the configuration register for all the devices in quick succession (Table 12).

Blink Output

The blink output pin indicates the blink phase, and is high during the P0 period and low during the P1 period. Blink phase status can also be read back as the P bit in the configuration register (Table 14). Typical uses for this output are:

- To provide an interrupt to the processor so that segment data can be changed synchronous to the blinking. For example, a clock application may have colon segments blinking every second between hours and minute digits, and the minute display is best changed in step with the colon segments. Also, if the rising edge of blink is detected, there is half a blink period to change the P1 digit data. Similarly, if the falling edge of blink is detected, the user has half a blink period to change the P0 digit data.
- If OSC is driven with an accurate frequency, blink can be used as a seconds counter or similar.

Scan-Limit Register

The scan-limit register sets how many monocolor digits are displayed, either two or four. A bicolor digit is connected as two monocolor digits (Table 21).

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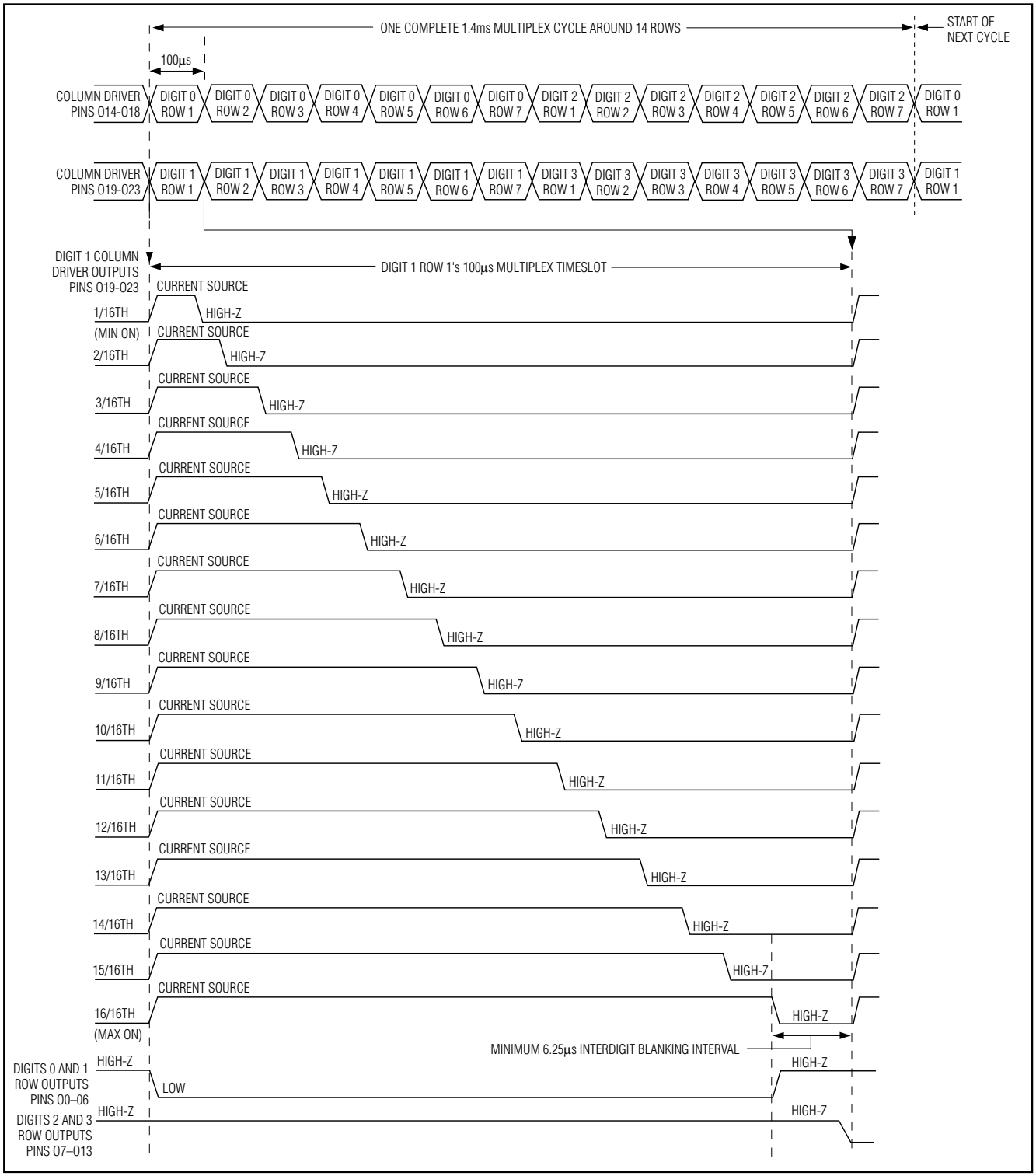

Figure 10. Multiplex Timing Diagram (OSC = 4MHz)

Table 18. User-Definable Font Pointer Base Address Table

FONT CHARACTER	ADDRESS CODE (HEX)	REGISTER DATA (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
RAM00	0x05	0x80	1	0	0	0	0	0	0	0
RAM01	0x05	0x85	1	0	0	0	0	1	0	1
RAM02	0x05	0x8A	1	0	0	0	1	0	1	0
RAM03	0x05	0x8F	1	0	0	0	1	1	1	1
RAM04	0x05	0x94	1	0	0	1	0	1	0	0
RAM05	0x05	0x99	1	0	0	1	1	0	0	1
RAM06	0x05	0x9E	1	0	0	1	1	1	1	0
RAM07	0x05	0xA3	1	0	1	0	0	0	1	1
RAM08	0x05	0xA8	1	0	1	0	1	0	0	0
RAM09	0x05	0xAD	1	0	1	0	1	1	0	1
RAM10	0x05	0xB2	1	0	1	1	0	0	1	0
RAM11	0x05	0xB7	1	0	1	1	0	1	1	1
RAM12	0x05	0xBC	1	0	1	1	1	1	0	0
RAM13	0x05	0xC1	1	1	0	0	0	0	0	1
RAM14	0x05	0xC6	1	1	0	0	0	1	1	0
RAM15	0x05	0xCB	1	1	0	0	1	0	1	1
RAM16	0x05	0xD0	1	1	0	1	0	0	0	0
RAM17	0x05	0xD5	1	1	0	1	0	1	0	1
RAM18	0x05	0xDA	1	1	0	1	1	0	1	0
RAM19	0x05	0xDF	1	1	0	1	1	1	1	1
RAM20	0x05	0xE4	1	1	1	0	0	1	0	0
RAM21	0x05	0xE9	1	1	1	0	1	0	0	1
RAM22	0x05	0xEE	1	1	1	0	1	1	1	0
RAM23	0x05	0xF3	1	1	1	1	0	0	1	1

The multiplexing scheme drives digits 0 and 1 at the same time, then digits 2 and 3 at the same time. To increase the effective brightness of the displays, drive only two digits instead of four. By doing this, the average segment current doubles, but also doubles the number of MAX6953s required to drive a given number of digits.

Because digit 1 is driven at the same time as digit 0 (and digit 3 is driven at the same time as digit 2), only 1 bit is used to set the scan limit. The bit is clear if one or two digits are to be driven, and set if three or four digits are to be driven (Table 21).

Intensity Registers

Display brightness is controlled digitally by four pulse-width modulators, one for each display digit. Each digit is controlled by a nibble of one of the two intensity registers, Intensity10 and Intensity32. The modulator scales the average segment current in 16 steps from a maximum of 15/16 down to 1/16 of the peak current. The minimum interdigit blanking time is therefore 1/16 of a cycle. The maximum duty cycle is 15/16 (Tables 23 and 24).

No-Op Register

A write to the No-Op register is ignored.

Selecting External Components R_{SET} and C_{SET} to Set Oscillator Frequency and Segment Current

The RC oscillator uses an external resistor R_{SET} and an external capacitor C_{SET} to set the oscillator frequency, f_{OSC}. The allowed range of f_{OSC} is 1MHz to 8MHz. R_{SET} also sets the peak segment current. The recommended values of R_{SET} and C_{SET} set the oscillator to

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Table 19. User-Definable Character Storage Example

FONT CHARACTER	FONT ADDRESS POINTER	ADDRESS CODE (HEX)	FONT POINTER ADDRESS (HEX)	REGISTER DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
RAM00	0x00	0x05	0x80	0	0	1	1	1	1	1	0
RAM00	0x01	0x05	0x81	0	1	0	1	0	0	0	1
RAM00	0x02	0x05	0x82	0	1	0	0	1	0	0	1
RAM00	0x03	0x05	0x83	0	1	0	0	0	1	0	1
RAM00	0x04	0x05	0x84	0	0	1	1	1	1	1	0
RAM01	0x05	0x05	0x85	0	0	0	0	0	0	0	0
RAM01	0x06	0x05	0x86	0	1	0	0	0	0	1	0
RAM01	0x07	0x05	0x87	0	1	1	1	1	1	1	1
RAM01	0x08	0x05	0x88	0	1	0	0	0	0	0	0
RAM01	0x09	0x05	0x89	0	0	0	0	0	0	0	0
RAM02	0x0A	0x05	0x8A	0	1	0	0	0	0	1	0
RAM02	0x0B	0x05	0x8B	0	1	1	0	0	0	0	1
RAM02	0x0C	0x05	0x8C	0	1	0	1	0	0	0	1
RAM02	0x0D	0x05	0x8D	0	1	0	0	1	0	0	1
RAM02	0x0E	0x05	0x8E	0	1	0	0	0	1	1	0

Table 20. Setting a Font Character to RAM Example

ADDRESS CODE (HEX)	REGISTER DATA (HEX)	ACTION BEING PERFORMED
0x05	0x8A	Set font address pointer to the base address of font character RAM02.
0x05	0x42	1st 7 bits of data: 1000010 goes to font address 0x8A; pointer then autoincrements to address 0x8B.
0x05	0x61	2nd 7 bits of data: 1100001 goes to font address 0x8B; pointer then autoincrements to address 0x8C.
0x05	0x51	3rd 7 bits of data: 1010001 goes to font address 0x8C; pointer then autoincrements to address 0x8D.
0x05	0x49	4th 7 bits of data: 1001001 goes to font address 0x8D; pointer then autoincrements to address 0x8E.
0x05	0x46	5th 7 bits of data: 1000110 goes to font address 0x8E; pointer then autoincrements to address 0x8F.

Table 21. Scan-Limit Register Format

SCAN LIMIT	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
		D7	D6	D5	D4	D3	D2	D1	D0	
Display Digits 0 and 1 Only	0x03	X	X	X	X	X	X	X	0	0xX0
Display Digits 0, 1, 2, and 3	0x03	X	X	X	X	X	X	X	1	0xX1

4MHz, which makes the blink frequencies 0.5Hz selectable between 1Hz. The recommended value of R_{SET} also sets the peak current to 40mA, which makes the segment current adjustable from 2.5mA to 37.5mA in 2.5mA steps:

$$I_{SEG} = K_I / R_{SET}\ mA$$
$$f_{OSC} = K_F / (R_{SET} \times C_{SET} + C_{STRAY})\ MHz$$

where:

K_I = 2040

K_F = 5304

R_{SET} = external resistor in kΩ

C_{SET} = external capacitor in pF

C_{STRAY} = stray capacitance from OSC pin to GND in pF, typically 2pF

The recommended value of R_{SET} is 51kΩ and the recommended value of C_{SET} is 24pF.

The recommended value of R_{SET} is the minimum allowed value since it sets the display driver to the maximum allowed segment current. R_{SET} can be set to a higher value to set the segment current to a lower peak value where desired. The user must also ensure that the peak current specifications of the LEDs connected to the driver are not exceeded.

The effective value of C_{SET} includes not only the actual external capacitor used, but also the stray capacitance from OSC to GND. This capacitance is usually in the 1pF to 5pF range, depending on the layout used.

Display-Test Register

The display-test register switches the drivers between one of two modes: normal and display test. Display-test mode turns all LEDs on by overriding, but not altering, all control and digit registers (including the shutdown register). In display-test mode, eight digits are scanned and the duty cycle is 7/16 (half power). Table 22 lists the display-test register format.

Applications Information

Choosing Supply Voltage to Minimize Power Dissipation

The MAX6953 drives a peak current of 40mA into LEDs with a 2.4V forward-voltage drop when operated from a supply voltage of at least 3.0V. The minimum voltage drop across the internal LED drivers is therefore (3.0V - 2.4V) = 0.6V. If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly. However, if the LEDs used have a higher forward voltage drop than 2.4V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.6V headroom.

The voltage drop across the drivers with a nominal 5V supply (5.0V - 2.4V) = 2.6V is nearly 3 times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.4V) = 0.9V. In most systems, consumption is an important design criterion, and the MAX6953 should be operated from the system's 3.3V nominal supply. In other designs, the lowest supply voltage may be 5V. The issue now is to ensure that the dissipation limit for the MAX6953 is not exceeded. This can be achieved by inserting a series resistor in the supply to the MAX6953, ensuring that the supply decoupling capacitors are still on the MAX6953 side of the resistor. For example, consider the requirement that the minimum supply voltage to a MAX6953 must be 3.0V, and the input supply range is 5V ±5%. Maximum supply current is:

$$15mA + (40mA \times 10) = 415mA$$

Minimum input supply voltage is 4.75V. Maximum series resistor value is:

$$(4.75V - 3.0V) / 0.415A = 4.22\Omega$$

We choose 3.3Ω ±5%. Worst-case resistor dissipation is at maximum toleranced resistance, i.e., $(0.415A)^2 \times (3.3\Omega \times 1.05) = 0.577W$. We choose a 1W resistor rating. The maximum MAX6953 supply voltage is at maximum input supply voltage and minimum toleranced resistance, i.e., $5.25V - (0.415A \times 3.3\Omega \times 0.95) = 3.95V$.

Table 22. Display-Test Register Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Normal operation	0x07	X	X	X	X	X	X	X	0
Display test	0x07	X	X	X	X	X	X	X	1

2-Wire Interfaced, 2.7V to 5.5V, 4-Digit 5 × 7 Matrix LED Display Driver

Table 23. Intensity Register Format for Digit 0 (Address 0x01) and Digit 2 (Address 0x02)

DUTY CYCLE	TYPICAL SEGMENT CURRENT (mA)	ADDRESS CODE (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
1/16 (min on)	2.5	0x01, 0x02	See Table 24.				0	0	0	0	0xX0
2/16	5	0x01, 0x02					0	0	0	1	0xX1
3/16	7.5	0x01, 0x02					0	0	1	0	0xX2
4/16	10	0x01, 0x02					0	0	1	1	0xX3
5/16	12.5	0x01, 0x02					0	1	0	0	0xX4
6/16	15	0x01, 0x02					0	1	0	1	0xX5
7/16	17.5	0x01, 0x02					0	1	1	0	0xX6
8/16	20	0x01, 0x02					0	1	1	1	0xX7
9/16	22.5	0x01, 0x02					1	0	0	0	0xX8
10/16	25	0x01, 0x02					1	0	0	1	0xX9
11/16	27.5	0x01, 0x02					1	0	1	0	0xXA
12/16	30	0x01, 0x02					1	0	1	1	0xXB
13/16	32.5	0x01, 0x02					1	1	0	0	0xXC
14/16	35	0x01, 0x02					1	1	0	1	0xXD
15/16	37.5	0x01, 0x02					1	1	1	0	0xXE
15/16 (max on)	37.5	0x01, 0x02					1	1	1	1	0xXF

Table 24. Intensity Register Format for Digit 1 (Address 0x01) and Digit 3 (Address 0x02)

DUTY CYCLE	TYPICAL SEGMENT CURRENT (mA)	ADDRESS CODE (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
1/16 (min on)	2.5	0x01, 0x02	0	0	0	0	See Table 23.				0x0X
2/16	5	0x01, 0x02	0	0	0	1					0x1X
3/16	7.5	0x01, 0x02	0	0	1	0					0x2X
4/16	10	0x01, 0x02	0	0	1	1					0x3X
5/16	12.5	0x01, 0x02	0	1	0	0					0x4X
6/16	15	0x01, 0x02	0	1	0	1					0x5X
7/16	17.5	0x01, 0x02	0	1	1	0					0x6X
8/16	20	0x01, 0x02	0	1	1	1					0x7X
9/16	22.5	0x01, 0x02	1	0	0	0					0x8X
10/16	25	0x01, 0x02	1	0	0	1					0x9X
11/16	27.5	0x01, 0x02	1	0	1	0					0xAX
12/16	30	0x01, 0x02	1	0	1	1					0xBX
13/16	32.5	0x01, 0x02	1	1	0	0					0xCX
14/16	35	0x01, 0x02	1	1	0	1					0xDX
15/16	37.5	0x01, 0x02	1	1	1	0					0xEX
15/16 (max on)	37.5	0x01, 0x02	1	1	1	1					0xFX

Low-Voltage Operation

The MAX6953 works over the 2.7V to 5.5V supply range. The minimum useful supply voltage is determined by the forward-voltage drop of the LEDs at the peak current I_{SEG}, plus the 0.6V headroom required by the driver output stages. The MAX6953 correctly regulates I_{SEG} with a supply voltage above this minimum voltage. If the supply drops below this minimum voltage, the driver output stages may brown out, and be unable to regulate the current correctly. As the supply voltage drops further, the LED segment drive current becomes effectively limited by the output driver's on-resistance, and the LED drive current drops. The characteristics of each individual LED in a 5 × 7 matrix digit are well matched, so the result is that the display intensity dims uniformly as supply voltage drops out of regulation and beyond. The MAX6953 operates down to 2V supply voltage (although most displays are very dim at this voltage), providing that the MAX6953 is powered up initially to at least 2.7V to trigger the device's internal reset, and also that the I²C interface is constrained to 100kbps.

Computing Power Dissipation

The upper limit for power dissipation (PD) for the MAX6953 is determined from the following equation:

$$P_D = (V+ \times 15mA) + (V+ - V_{LED})(DUTY \times I_{SEG} \times N)$$

where:

V+ = supply voltage

Duty = duty cycle set by intensity register

N = number of segments driven (worst case is 10)

V_{LED} = LED forward voltage

I_{SEG} = segment current set by R_{SET}

P_D = power dissipation, in mW if currents are in mA

Dissipation example:

I_{SEG} = 40mA, N = 10, Duty = 15 / 16, V_{LED} = 2.4V at 40mA, V+ = 3.6V

$$P_D = 3.6V\ (15mA) + (3.6V - 2.4V)\ (15 / 16 \times 40mA \times 10) = 0.504W$$

Thus, for a 36-pin SSOP package (T_{JA} = 1 / 0.0118 = +85°C/W from operating ratings), the maximum allowed ambient temperature T_A is given by:

$$T_{J(MAX)} = T_A + (P_D \times T_{JA}) = +150°C = T_A + (0.504 \times +85°C/W)$$

So T_A = +107°C. Thus, the part can be operated safely at a maximum package temperature of +85°C.

Power Supplies

The MAX6953 operates from a single 2.7V to 5.5V power supply. Bypass the power supply to GND with a 0.1µF capacitor as close to the device as possible. Add a 47µF capacitor if the MAX6953 is not close to the board's input bulk decoupling capacitor.

Board Layout

When designing a board, use the following guidelines:

1) The R_{SET} connection to the ISET pin is a high-impedance node, and sensitive to layout. Place R_{SET} right next to the ISET pin and route R_{SET} directly to these pins with very short tracks.
2) Ensure that the track from the ground end of R_{SET} routes directly to GND pin 19 (PDIP package) or GND pin 17 (SSOP package), and that this track is not used as part of any other ground connection.

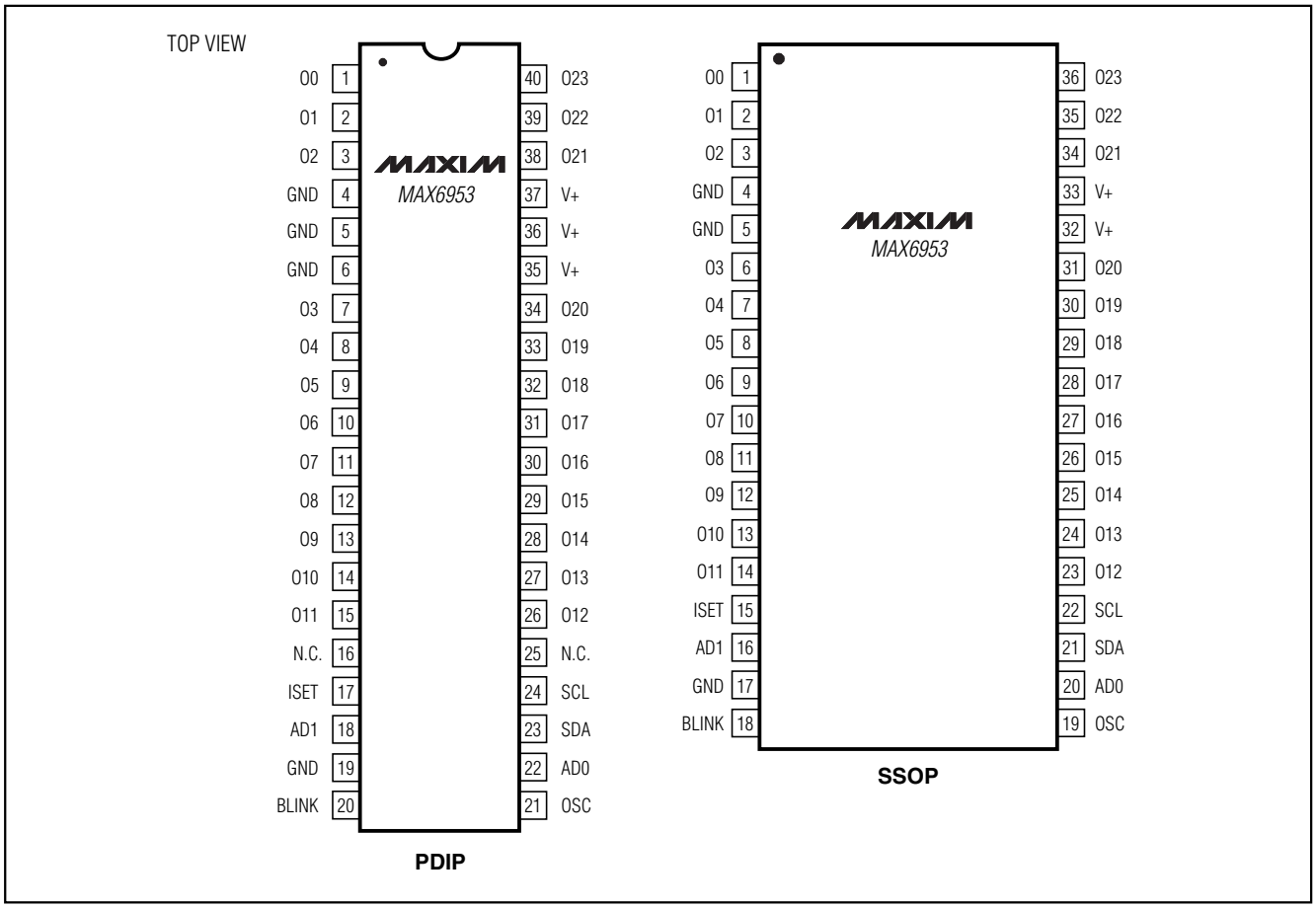
Chip Information

TRANSISTOR COUNT: 44,078

PROCESS: CMOS

2-Wire Interfaced, 2.7V to 5.5V, 4-Digit 5 × 7 Matrix LED Display Driver

Pin Configurations

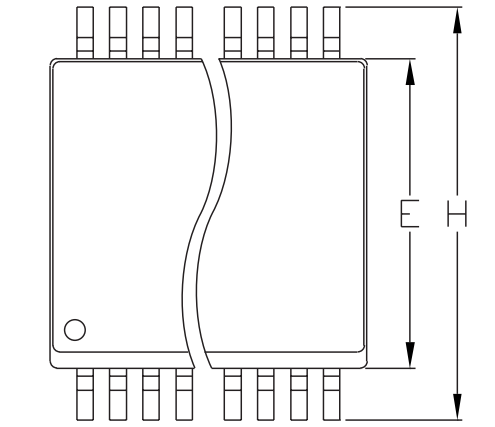


2-Wire Interfaced, 2.7V to 5.5V, 4-Digit 5 × 7 Matrix LED Display Driver

Package Information

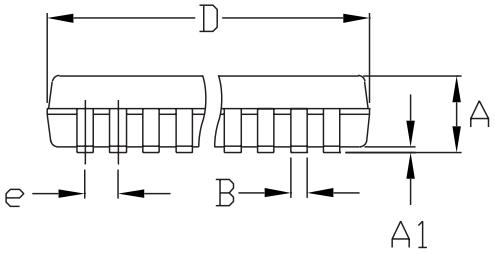
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

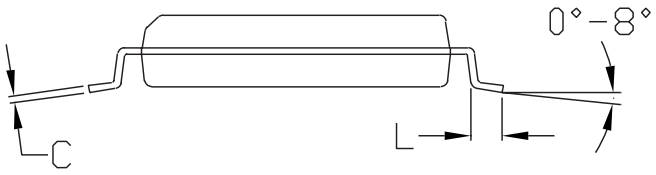
SSOP.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
e	0.0315		0.80	
E	0.292	0.298	7.42	7.57
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.604	0.610	15.34	15.49	36
D	0.702	0.708	17.83	17.98	44





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 36/44L, .300X8mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0040	B	1/1