

## **ADC601**

# 12-Bit 900ns ANALOG-TO-DIGITAL CONVERTER

## **FEATURES**

FAST CONVERSION: 900nsCAN BE SHORT-CYCLED

■ INPUT RANGES: ±5V, ±10V, 0 to -10V
 ● HIGH SIGNAL/NOISE RATIO: 68dB

LOW IMD: 75dB

PARALLEL AND SERIAL OUTPUT

32-PIN CERAMIC DIP PACKAGE

## **DESCRIPTION**

The ADC601 is a high-speed Duolithic<sup>TM</sup> (two chips) successive approximation analog-to-digital converter. This unique two-chip design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADC601 has been tested with several sample/hold amplifiers and distortion results are documented in this data sheet.

The ADC601 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Conversion time is set at the factory to 900ns. Serial and parallel output performance is guaranteed

## **APPLICATIONS**

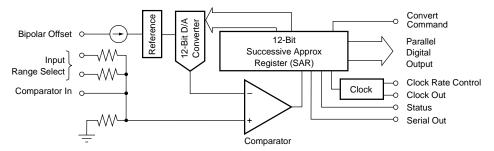
- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

with no missing codes over the full input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of  $\pm 5$ V,  $\pm 10$ V and 0V to -10V. The ADC601's input is specifically designed to be easily driven with minimal disturbance to the driving amplifier.

Output codes are available in complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are  $\pm 15V$  and  $\pm 5V$ .



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# **SPECIFICATIONS**

## **ELECTRICAL**

 $T_{\text{CASE}} = +25^{\circ}\text{C}, \, 900\text{ns conversion time}, \, \pm V_{\text{CC}} = \pm 15\text{V}, \, +V_{\text{DD}} = +5\text{V}, \, \text{and 6-minute warm-up in a normal convection environment unless otherwise noted}.$ 

	ADC601JG		•	ADC601KG			I	
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								•
INPUTS								
Voltage Ranges: Bipolar	Full Scale(FSR)(1)(2)		±5, ±10			*		V
Unipolar	Full Scale(FSR) <sup>(1)(2)</sup>		0 to -10 1.4			*		V
Impedance: -10V to 0V, ±5V ±10V			2.4			*		kΩ kΩ
TRANSFER CHARACTERISTICS	<u> </u>	l						
ACCURACY								
Gain Error <sup>(3)</sup>	990ns Conversion Time		±0.08	±0.55		*	±0.2	%
Input Offset Error <sup>(3)</sup> : Unipolar	990ns Conversion Time		±0.12	±1.2		*	±0.5	% of FSR
Bipolar	990ns Conversion Time		±0.08	±0.8		*	±0.25	% of FSR
Integral Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
Differential Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
No Missing Codes Power Supply Rejection of Offset and Gain	$\Delta + V_{CC} = \pm 5\%$		±0.0036	Guara	inteed	*		%FSR/%V <sub>cc</sub>
Tower supply regionion of shoot and sain	$\Delta - V_{cc} = \pm 5\%$		±0.0005			*		%FSR/%V
	$\Delta + V_{DD} = \pm 5\%$		±0.001				*	%FSR/%VDD
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family			TTL-	Compatib	le CMOS	1		
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
Convert Command Currents	Logic High	+2		+V <sub>DD</sub>	*		*	V 
Convert Command Currents	Logic Low Logic High			-150 -150				μA μA
Convert Command			High	Level Wh	i en Conve	erting		<b>,</b>
CONVERSION TIME								
Factory Set	Without User Adjustment		0.9	1		*	*	μs
Power Supply Rejection of Conversion Time	$D + V_{DD} = \pm 5\%$		±1			*		ns/%V <sub>DD</sub>
OUTPUT								
Logic Family			TTL-	Compatib	le CMOS	1		
Bits 1 through 12, Serial, Status, Clock Out	Logic Low, I <sub>oL</sub> = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I <sub>oH</sub> = −1mA	+2.7	+4.9		*	*	*	V
Internal Clock Frequency Status			13	Level Wh	on Data V	* /alid		MHz
DYNAMIC CHARACTERISTICS (4) (5) (6) Teste		and ADC		Typical P	erformand		)	T
Differential Linearity Error	f <sub>c</sub> = 10kHz: 68.3% of All Codes 99.7% of All Codes		0.5 0.8			0.4 0.6		LSB LSB
	100% of All Codes		1.0			0.7		LSB
Total Harmonic Distortion			-70			*		dBc
Total Harmonic Distortion	$f_c = 10kHz$ , $f_s = 500kHz$ $f_c = 10kHz$ , $f_s = 1MHz$		-74			*		dBc
	$f_{c} = 250 \text{kHz}, f_{s} = 500 \text{kHz}$		-70			*		dBc
	$f_c = 500$ kHz, $f_s = 1$ MHz		-68			*		dBc
Two-Tone Intermodulation Distortion(7)	$f_c = 11$ kHz and 15kHz, $f_s = 500$ kHz		-79			*		dBc
	$f_c = 50$ kHz and 55kHz, $f_s = 500$ kHz		-78			*		dBc
	$f_c = 90kHz$ and 110kHz, $f_s = 500kHz$		-77			*		dBc
Signal-to-Noise and Distortion	$f_{c} = 250 \text{kHz}, f_{s} = 500 \text{kHz}$		66			*		dB
(SINAD) Ratio	$f_c = 500 \text{kHz}, f_s = 1 \text{MHz}$		65			_ ^		dB
Signal-to-Noise Ratio (SNR)	$f_{c} = 250 \text{kHz}, f_{s} = 500 \text{kHz}$ $f_{c} = 500 \text{kHz}, f_{s} = 1 \text{MHz}$		68 67			*		dB dB
PERFORMANCE OVER TEMPERATURE	°C							
Gain	T <sub>MIN</sub> to T <sub>MAX</sub>		±10	±30		*	*	ppm of FSR/°(
Input Offset: Unipolar	T <sub>MIN</sub> to T <sub>MAX</sub>		±2	±7		*	*	ppm of FSR/°(
Bipolar	T <sub>MIN</sub> to T <sub>MAY</sub>		±3	±10		*	*	ppm of FSR/°0
Internal Linearity Error	0.9μs Conversion Time T <sub>MIN</sub> to T <sub>MAX</sub>		±0.02			±0.015		% of FSR
Differential Linearity Error	0.9µs Conversion Time T <sub>MIN</sub> to T <sub>MAX</sub>		±0.02			±0.015		% of FSR
No Missing Codes Conversion Drift	0.9μs Conversion Time $T_{MIN}$ to $T_{MAX}$		2	Guara	nteed I	*		ns/°C
Common Diff.		1	-				1	113/ 0



## SPECIFICATIONS (CONT)

#### **ELECTRICAL**

 $T_{\text{CASE}} = +25^{\circ}\text{C}$ , 900ns conversion time,  $\pm V_{\text{CC}} = \pm 15\text{V}$ ,  $\pm V_{\text{DD}} = +5\text{V}$ , and 6-minute warm-up in a normal convection environment unless otherwise noted.

		Α	ADC601JG		ADC601KG			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS								
Supply Voltages: +V <sub>cc</sub>		+14.25	+15	+15.75	*	*	*	V
-V <sub>cc</sub>		-14.25	-15	-15.75	*	*	*	V
+V <sub>DD</sub>		+4.75	+5	+5.25	*	*	*	V
Supply Currents: +I <sub>cc</sub>			5.4	7.0		*	*	mA
-I <sub>cc</sub>			-65	-84.5		*	*	mA
+l <sub>pp</sub>			53	68.9		*	*	mA
Power Consumption	Nominal $\pm V_{CC}$ and $+V_{DD}$		1.3	1.7		*	*	W
Thermal Resistance, $\theta_{ m JC}$	66 22		25			*	*	°C/W
TEMPERATURE RANGE(8)								
Specification		0		+70	*		*	°C
Operating		-25		+85	*		*	°C

<sup>\*</sup> Same specifications as for ADC601JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) Dynamic tests are performed using SHC804 with ADC601 unless otherwise specified. Performance may vary depending upon choice of sample/hold. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = 0dB;  $f_c$  = input frequency;  $f_s$  = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal ( $\approx$ 0dB), the intermodulation products will be 6dB lower. For example, unit connected for  $\pm$ 10V has 20V FSR. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board; with the test device in a (zero insertion force) socket. Thermal resistance will be lower if the ADC601 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

#### **ABSOLUTE MAXIMUM RATINGS**

±V <sub>cc</sub> +V <sub>DD</sub>	±18V
+V <sub>DD</sub>	+7V
Digital Inputs	
Analog Inputs	
Comparator Input	
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	65°C to +150°C
Stresses above these ratings may permanently	damage the device.

#### ORDERING INFORMATION

Basic Model Number — Performance Grade Code — J, K: 0°C to +70°C Case Temperature	ADC601	G
Package Code G: Ceramic DIP		

#### PACKAGE INFORMATION(1)

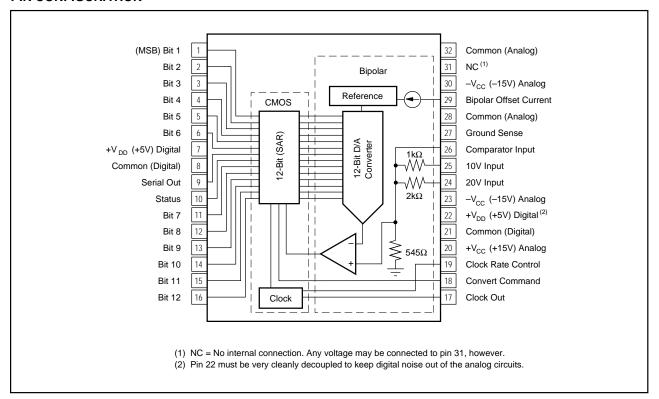
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC601JG	32-Pin Hermetic DIP	172–2
ADC601KG	32-Pin Hermetic DIP	172–2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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#### **PIN CONFIGURATION**



#### **PIN DEFINITIONS**

PIN NUMBER	DESIGNATION	DESCRIPTION		
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data capable of sinking 3.2mA.		
9	Serial Out	12-bit serial data output synchronized with the negative edge of each appropriate clock cycle.		
10	Status	Conversion status strobe is high during data conversion; low when parallel data is valid. Negative edge may be used to latch parallel data, however, appropriate latch set-up time must be provided. Refer to t <sub>BBL</sub> in the ADC601 timing diagram.		
17	Clock Out	Negative edge indicates when serial data is valid. After convert command goes high, fist cycle clocks bit 1 (MSB). The clock continues to run when convert command is high and resets low with convert command.		
18	Convert Command	High transition starts conversion; and should remain high during conversion. Low will reset clock and SAR logic.		
19	Clock Rate Control	May be used to increase clock speed, by increasing the positive portion of the clock. High is normal operation.		
24	20V Input	20V input range allows $\pm 10$ Vp-p analog input signal. Short to ground when not used.		
25	10V Input	10V input range allows 0 to $-10$ Vp-p or $\pm 5$ Vp-p input range.		
26	Comparator In	Only used in bipolar mode when it is connected to bipolar offset pin through short lead with low resistance.		
27	Ground Sense	Ground Sense pin. (See text for use).		
29	Bipolar Offset Current	Bipolar offset current short to comparator In through very short lead with very low resistance for bipolar operation. Short to ground for unipolar operation.		