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# ⟋National Semiconductor

# ADC1005
# 10-Bit µP Compatible A/D Converter

## General Description

The ADC1005 is a CMOS 10-bit successive approximation A/D converter. The 20-pin ADC1005 outputs 10-bit data in a two-byte format for interface with 8-bit microprocessors.

The ADC1005 has differential inputs to permit rejection of common-mode signals, allow the analog input range to be offset, and also to permit the conversion of signals not referred to ground. In addition, the reference voltage can be adjusted, allowing smaller voltage spans to be measured with 10-bit resolution.
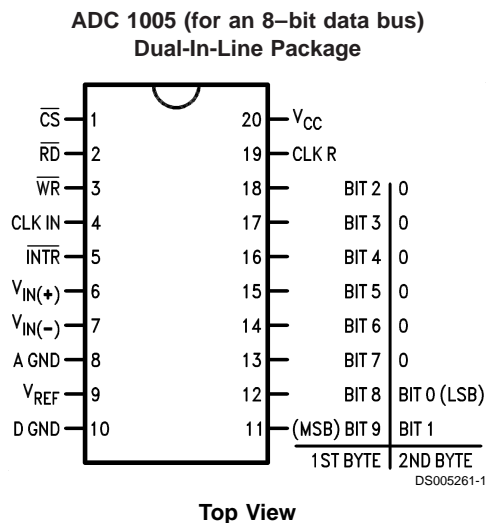
## Features

- Easy interface to all microprocessors
- Differential analog voltage inputs
- Operates ratiometrically or with 5 $V_{DC}$ voltage reference or analog span adjusted voltage reference
- 0V to 5V analog input voltage range with single 5V supply
- On-chip clock generator
- TLL/MOS input/output compatible
- 0.3" standard width 20-pin DIP

## Key Specifications

- Resolution                          10 bits
- Linearity Error            ±½ LSB and ±1 LSB
- Conversion Time                      50 µs

## Connection Diagram

**ADC 1005 (for an 8–bit data bus)**
**Dual-In-Line Package**



| | |
|---|---|
| $\overline{CS}$ — 1 | 20 — $V_{CC}$ |
| $\overline{RD}$ — 2 | 19 — CLK R |
| $\overline{WR}$ — 3 | 18 — BIT 2 \| 0 |
| CLK IN — 4 | 17 — BIT 3 \| 0 |
| $\overline{INTR}$ — 5 | 16 — BIT 4 \| 0 |
| $V_{IN(+)}$ — 6 | 15 — BIT 5 \| 0 |
| $V_{IN(-)}$ — 7 | 14 — BIT 6 \| 0 |
| A GND — 8 | 13 — BIT 7 \| 0 |
| $V_{REF}$ — 9 | 12 — BIT 8 \| BIT 0 (LSB) |
| D GND — 10 | 11 — (MSB) BIT 9 \| BIT 1 |
| | 1ST BYTE \| 2ND BYTE |

DS005261-1

**Top View**

## Ordering Information

| Part Number | Package Outline | Temperature Range | Linearity Error |
|---|---|---|---|
| ADC1005BCJ-1 | J20A | 0˚C to +70˚C | ±½ LSB |
| ADC1005BCJ | J20A | −40˚C to +85˚C | |
| ADC1005CCJ-1 | J20A | 0˚C to +70˚C | ±1 LSB |
| ADC1005CCJ | J20A | −40˚C to +85˚C | |

## Absolute Maximum Ratings (Notes 1, 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 6.5V |
| Logic Control Inputs | −0.3V to +15V |
| Voltage at Other Inputs and Outputs | −0.3V to $V_{CC}$ +0.3V |
| Input Current Per Pin | ±5 mA |
| Input Current Per Package | ±20 mA |
| Storage Temperature Range | −65°C to +150°C |
| Package Dissipation at $T_A$=25°C | 875 mW |
| Lead Temperature | |
| (Soldering, 10 seconds) | |

| | |
|---|---|
| Dual-In-Line Package (Ceramic) | 300°C |
| Surface Mount Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |
| ESD Susceptibility (Note 8) | 800V |

## Operating Ratings (Notes 1, 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.5V to 6.0V |
| Temperature Range | $T_{MN} \leq T_A \leq T_{MAX}$ |
| ADC1005BCJ, ADC1005CCJ | −40°C≤$T_A$≤+85°C |
| ADC1005BCJ-1, ADC1005CCJ-1 | |

## Electrical Characteristics

The following specifications apply for $V_{CC}$ = 5V, $V_{REF}$ = 5V, $f_{CLK}$ = 1.8 MHz unless otherwise specified. **Boldface limits apply from $T_{MIN}$ to $T_{MAX}$**; All other limits $T_A = T_j$ = 25°C.

| Parameter | Conditions | ADC1005BCJ ADC1005CCJ | | | ADC1005BCJ-1, ADC1005CCJ-1 | | | Limit Units |
|---|---|---|---|---|---|---|---|---|
| | | Typ (Note 5) | Tested Limit (Note 6) | Design Limit (Note 7) | Typ (Note 5) | Tested Limit (Note 6) | Design Limit (Note 7) | |
| **Converter Characteristics** | | | | | | | | |
| Linearity Error (Note 3) | | | | | | | | |
| ADC1005BCJ | | | **±0.5** | | | | | LSB |
| ADC1005BCJ-1 | | | | | | ±0.5 | **±0.5** | LSB |
| ADC1005CCJ | | | **±1** | | | | | LSB |
| ADC1005CCJ-1, CCV | | | | | | ±1 | **±1** | LSB |
| Zero Error | | | | | | | | |
| ADC1005BCJ | | | **±0.5** | | | | | LSB |
| ADC1005BCJ-1 | | | | | | ±0.5 | **±0.5** | LSB |
| ADC1005CCJ | | | **±1** | | | | | LSB |
| ADC1005CCJ-1, CCV | | | | | | ±1 | **±1** | LSB |
| Fullscale Error | | | | | | | | |
| ADC1005BCJ | | | **±0.5** | | | | | LSB |
| ADC1005BCJ-1 | | | | | | ±0.5 | **±0.5** | LSB |
| ADC1005CCJ | | | **±1** | | | | | LSB |
| ADC1005CCJ-1, CCV | | | | | | ±1 | **±1** | LSB |
| Reference Input Resistance  MIN | | 4.8 | **2.2** | | 4.8 | 2.4 | **2.2** | kΩ |
|   MAX | | 4.8 | **8.3** | | 4.8 | 7.6 | **8.3** | kΩ |
| Common-Mode Input (Note 4)  MIN | $V_{IN}$(+) or $V_{IN}$(−) | | **$V_{CC}$+0.05** | | | $V_{CC}$+0.05 | **$V_{CC}$+0.05** | V |
|   MAX | | | **GND−0.05** | | | GND−0.05 | **GND−0.05** | V |
| DC Common-Mode Error | Over Common-Mode Input Range | ±⅛ | **±¼** | | ±⅛ | ±¼ | **±¼** | LSB |
| Power Supply Sensitivity | $V_{CC}$=5 $V_{DC}$±5% $V_{REF}$ = 4.75V | ±⅛ | **±¼** | | ±⅛ | ±¼ | **±¼** | LSB |

## Electrical Characteristics (Continued)

The following specifications apply for $V_{CC}$ = 5V, $V_{REF}$ = 5V, $f_{CLK}$ = 1.8 MHz unless otherwise specified. **Boldface limits apply from $T_{MIN}$ to $T_{MAX}$**; All other limits $T_A = T_j = 25°C$.

| Parameter | Conditions | ADC1005BCJ ADC1005CCJ | | | ADC1005BCJ-1, ADC1005CCJ-1 | | | Limit Units |
|---|---|---|---|---|---|---|---|---|
| | | Typ (Note 5) | Tested Limit (Note 6) | Design Limit (Note 7) | Typ (Note 5) | Tested Limit (Note 6) | Design Limit (Note 7) | |
| **DC Characteristics** | | | | | | | | |
| $V_{IN(1)}$ Logical "1" Input Voltage MIN | $V_{CC}$=5.25V (except $CLK_{IN}$) | | **2.0** | | | 2.0 | **2.0** | V |
| $V_{IN(0)}$, Logical "0" Input Voltage MAX | $V_{CC}$=4.75V (Except $CLK_{IN}$) | | **0.8** | | | 0.8 | **0.8** | V |
| $I_{IN}$, Logical "1" Input Current MAX | $V_{IN}$=5.0V | 0.005 | **1** | | 0.005 | 1 | **1** | µA |
| $I_{IN}$, Logical "0" Input Current MAX | $V_{IN}$=0V | −0.005 | **−1** | | −0.005 | −1 | **−1** | µA |
| $V_{T+(MIN)}$, Minimum $CLK_{IN}$ Positive going Threshold Voltage | | 3.1 | **2.7** | | 3.1 | 2.7 | **2.7** | V |
| $V_{T(MAX)}$, Maximum $CLK_{IN}$ Positive going Threshold Voltage | | 3.1 | **3.5** | | 3.1 | 3.5 | **3.5** | V |
| $V_{T−(MIN)}$, Minimum $CLK_{IN}$ Negative going Threshold Voltage | | 1.8 | **1.5** | | 1.8 | 1.5 | **1.5** | V |
| $V_{T−(MAX)}$, Maximum $CLK_{IN}$ Negative going Threshold Voltage | | 1.8 | **2.1** | | 1.8 | 2.1 | **2.1** | V |
| $V_{H(MIN)}$, Minimum $CLK_{IN}$ Hysteresis ($V_{T+}$-$V_{T−}$) | | 1.3 | **0.6** | | 1.3 | 0.6 | **0.6** | V |
| $V_{H(MAX)}$, Maximum $CLK_{IN}$ Hysteresis ($V_{T+}$-$V_{T−}$) | | 1.3 | **2.0** | | 1.3 | 2.0 | **2.0** | V |
| $V_{OUT(1)}$, Logical "1" Output Voltage MIN | $V_{CC}$=4.75V $I_{OUT}$=−360 µA $I_{OUT}$=−10 µA | | **2.4** **4.5** | | | 2.8 4.6 | **2.4** **4.5** | V V |
| $V_{OUT(0)}$, Logical "0" Output Voltage MAX | $V_{CC}$=4.75V $I_{OUT}$=1.6 mA | | **0.4** | | | 0.34 | **0.4** | V |
| $I_{OUT}$, TRI-STATE Output Current MAX | $V_{OUT}$ = 0V $V_{OUT}$ = 5V | −0.01 0.01 | **−3** **3** | | −0.01 0.01 | −0.3 0.3 | **−3** **3** | µA µA |
| $I_{SOURCE}$, Output Source Current MIN | $V_{OUT}$=0V | −14 | **−6.5** | | −14 | −7.5 | **−6.5** | mA |
| $I_{SINK}$, Output Sink Current MIN | $V_{OUT}$=5V | 16 | **8.0** | | 16 | 9.0 | **8.0** | mA |
| $I_{CC}$, Supply Current MAX | $f_{CLK}$=1.8 MHz $\overline{CS}$ ="1" | 1.5 | **3** | | 1.5 | 2.5 | **3** | mA |

# AC Electrical Characteristics

The following specifications apply for $V_{CC}$ = 5V, $V_{REF}$ = 5V, $V_{REF}$ = 5V, $t_r$ = $t_f$ = 20 ns unless otherwise specified. **Boldface limits apply from $T_{MIN}$ to $T_{MAX}$;** All other limits $T_A = T_j = 25°C$.

| Parameter | | Conditions | Typ (Note 5) | Tested Limit (Note 6) | Design Limit (Note 7) | Limit Units |
|---|---|---|---|---|---|---|
| $f_{CLK}$, Clock Frequency | MIN | | | 0.2 | 0.2 | MHz |
| | MAX | | | 2.6 | 2.6 | MHz |
| Clock Duty Cycle | MIN | | | 40 | 40 | % |
| | MAX | | | 60 | 60 | % |
| $t_C$, Conversion Time | MIN | | | 80 | 80 | $1/f_{CLK}$ |
| | MAX | | | 90 | 90 | $1/f_{CLK}$ |
| | MIN | $f_{CLK}$=1.8 MHz | | 45 | 45 | µs |
| | MAX | $f_{CLK}$=1.8 MHz | | 50 | 50 | µs |
| $t_{W(\overline{WR})L}$, Minimum $\overline{WR}$ Pulse Width | | $\overline{CS}$ =0 | 100 | 150 | 150 | ns |
| $t_{ACC}$, Access Time (Delay from falling edge of $\overline{RD}$ to Output Data Valid) | | $\overline{CS}$ =0 $C_L$=100 pF, $R_L$ = 2k | 170 | 300 | 300 | ns |
| $t_{1H}$, $t_{0H}$, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State) | | $R_L$=10k, $C_L$=10 pF | 125 | | 200 | ns |
| | | $R_L$=2k, $C_L$=100 pF | 145 | 230 | 230 | ns |
| $t_{WI}$, $t_{RI}$, Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$ | | | 300 | 450 | 450 | ns |
| $t_{IRS}$, $\overline{INTR}$ to 1st Read Set-up Time | | | 400 | 550 | 550 | ns |
| $C_{IN}$, Capacitance of Logic Inputs | | | 5 | | 7.5 | pF |
| $C_{OUT}$, Capacitance of Logic Outputs | | | 5 | | 7.5 | pF |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to ground.

**Note 3:** Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through the end points of the transfer characteristic.

**Note 4:** For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 00 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than $V_{CC}$ supply. Be careful, during testing at low $V_{CC}$ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog $V_{IN}$ does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 $V_{DC}$ to 5 $V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.950 $V_{DC}$ over temperature variations, initial tolerance and loading.
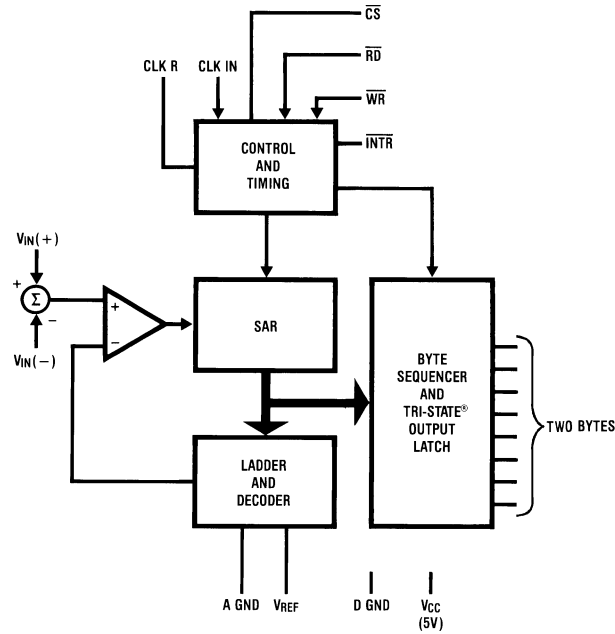
**Note 5:** Typicals are at 25°C and represent most likely parametric norm.

**Note 6:** Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 7:** Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

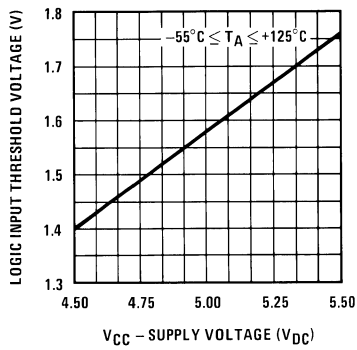**Note 8:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.
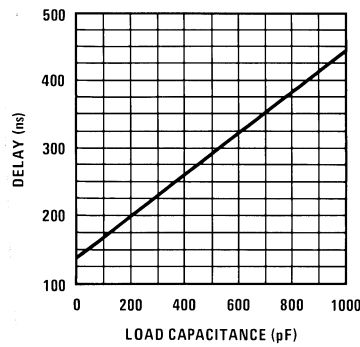
# Functional Diagram



DS005261-3

# Typical Performance Characteristics
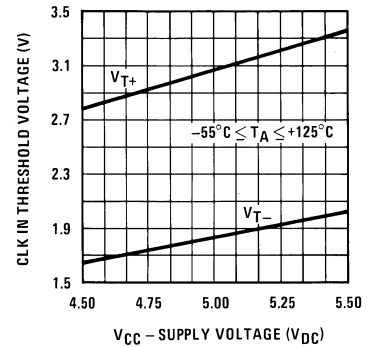
**Logic Input Threshold Voltage vs Supply Voltage**



DS005261-21

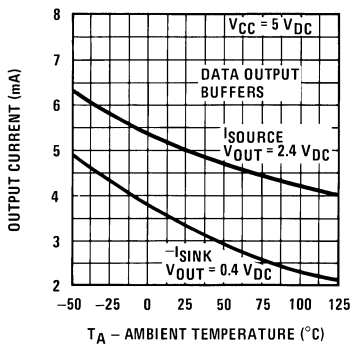**Delay from Falling Edge of RD to Output data Valid vs Load Capacitance**
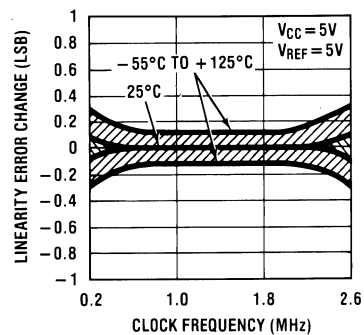


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**CLK IN Schmitt Trip Levels vs Supply Voltage**
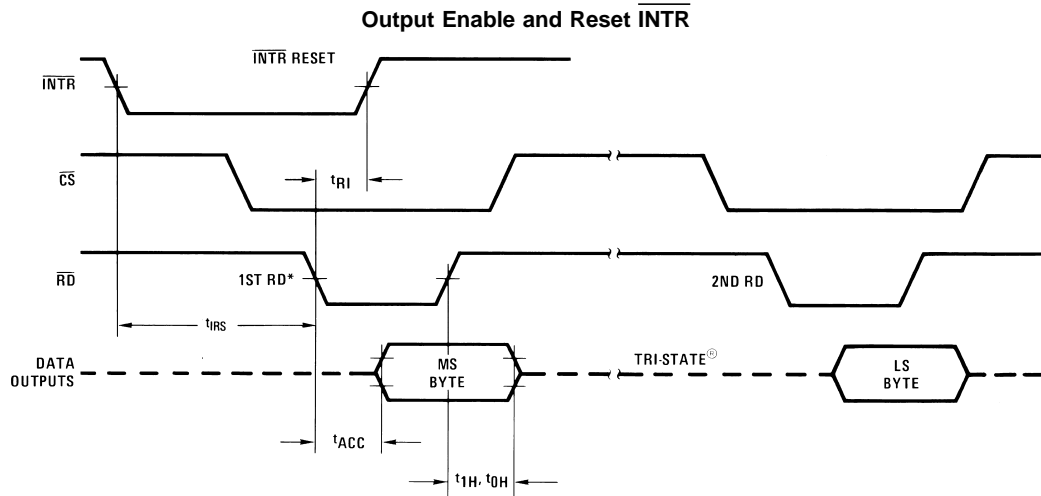


DS005261-23

**Output Current vs Temperature**



DS005261-24

**Typical Linearity Error vs Clock Frequency**



DS005261-25

# Timing Diagrams

**Start Conversion**



DS005261-5

**Output Enable and Reset $\overline{INTR}$**
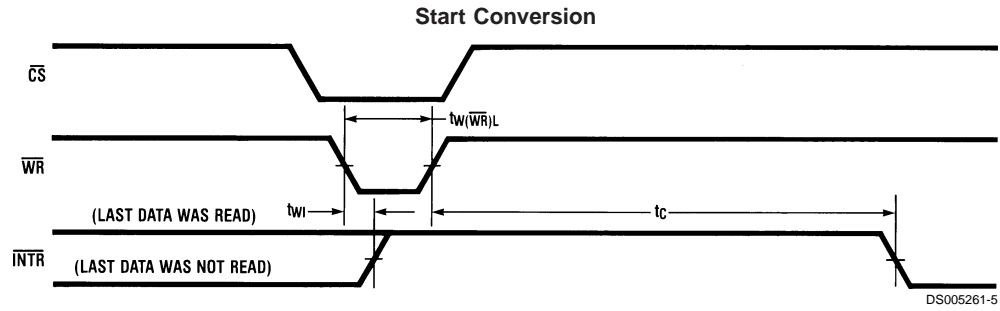


DS005261-6

**Note:** All timing is measured from the 50% voltage points.

**Byte Sequencing for ADC1005**

| Byte Order | 8-Bit Data Bus Connection | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **DB7** | **DB6** | **DB5** | **DB4** | **DB3** | **DB2** | **DB1** | **DB0** |
| 1st | MSB Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 |
| 2nd | Bit 1 | LSB Bit 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# Block Diagram
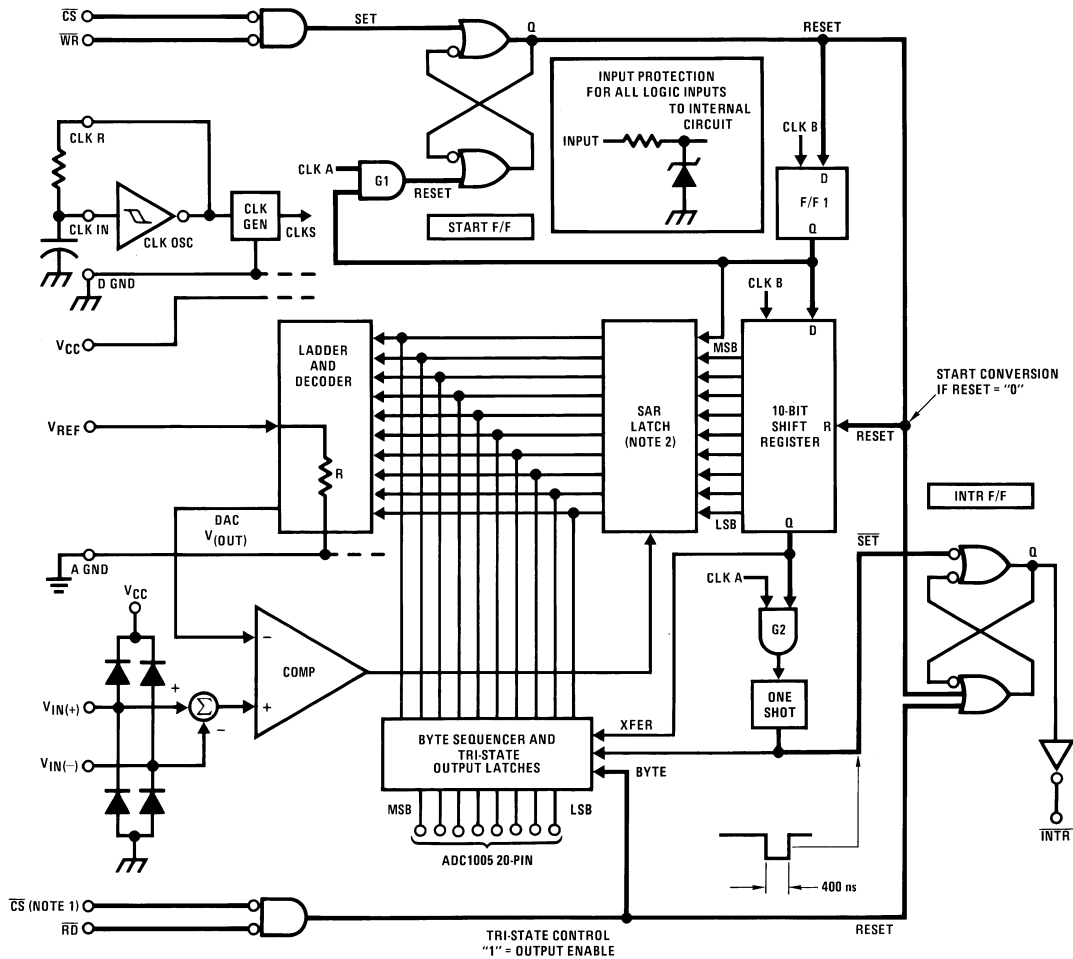


**Note 9:** $\overline{CS}$ shown twice for clarity.

**Note 10:** SAR=Successive Approximation Register.

**FIGURE 1.**

# Functional Description

## 1.0 GENERAL OPERATION

A block diagram of the A/D converter is shown in *Figure 1*. All of the inputs and outputs are shown and the major logic control paths are drawn in heavier weight lines.

## 1.1 Converter Operation

The ADC1005 uses an advanced potentiometric resistive ladder network. The analog inputs, as well as the taps of this ladder network are switched into a weighted capacitor array. The output of this capacitor array is the input to a sampled data comparator. This comparator allows the successive approximation logic to match the analog input voltage $[V_{IN}(+) - V_{IN}(-)]$ to taps on the R network. The most significant bit is tested first and after 10 comparisons (80 clock cycles) a digital 10-bit binary code (all "1"s = full-scale) is transferred to an output latch.

## 1.2 Starting a Conversion

The conversion is initialized by taking $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 10-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is

at the input end of the 10-bit shift register. Internal clock signals then transfer this "1" to the Q ouput of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 10-bit shift register then can have the "1" clocked in, allowing the conversion process to continue. If the set signal were still present, this reset pulse would have no effect and the 10-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals. The converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

To summarize, on the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start after at least one of these inputs makes a low-to-high transition.*

## 1.3 Output Control

After the "1" is clocked through the 10-bit shift register (which completes the SAR search) it causes the new digital word to transfer to the TRI-STATE output latches. When the XFER

# Functional Description (Continued)

signal makes a high-to-low transition the one shot fires, setting the INTR F/F. An inverting buffer then supplies the $\overline{\text{INTR}}$ output signal.

Note that this $\overline{\text{SET}}$ control of the INTR F/F remains low for approximately 400 ns. If the data output is continuously enabled ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ both held low) the $\overline{\text{INTR}}$ output will still signal the end of the conversion (by a high-to-low transition). This is because the $\overline{\text{SET}}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level. This $\overline{\text{INTR}}$ output will therefore stay low for the duration of the $\overline{\text{SET}}$ signal.

When data is to be read, the combination of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled.

### 1.4 Free-Running and Self-Clocking Modes

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{\text{CS}}$ input is grounded and the $\overline{\text{WR}}$ input is tied to the $\overline{\text{INTR}}$ output. This $\overline{\text{WR}}$ and $\overline{\text{INTR}}$ node should be momentarily forced to logic low following a power-up cycle to ensure start up.

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN makes use of a Schmitt trigger as shown in *Figure 2*.
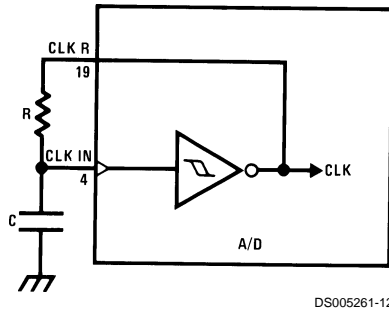


DS005261-12

$$f_{CLK} \cong \frac{1}{1.1\, RC}$$

**FIGURE 2. Self-Clocking the A/D**

### 2.0 REFERENCE VOLTAGE

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 1024 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 4.8 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 3*) the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the $V_{REF}$ pin can be tied to $V_{CC}$. This technique relaxes the stability requirements of the system references as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 4*), where the analog input varies between very specific voltage limits, the reference pin

can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the $V_{CC}$ supply voltage. The minimum value, however, can be small to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout, and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/1024$).
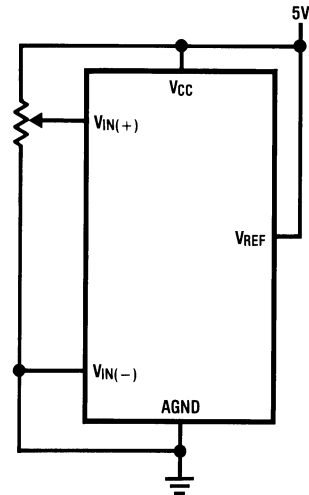


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**FIGURE 3. Ratiometric**
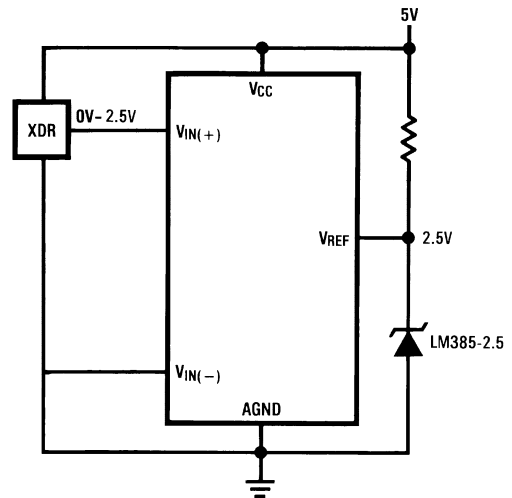


DS005261-18

**FIGURE 4. Absolute with a Reduced Span**

### 3.0 THE ANALOG INPUTS

### 3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential inputs of these converters reduce the effects of common-mode input noise, which is defined as noise common to both selected "+" and "−" inputs (60 Hz is most typical). The time interval between sampling the "+" input and the "−" input is half of an internal clock period. The

# Functional Description (Continued)

change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal, this error is:

$$V_{ERROR(MAX)} = V_{PEAK} (2\pi\, f_{CM}) \times \frac{4}{f_{CLK}}$$

where $f_{CM}$ is the frequency of the common-mode signal, $V_{PEAK}$ is its peak voltage value and $f_{CLK}$ is the clock frequency at the CLK IN pin.

For a 60 Hz common-mode signal to generate a ¼ LSB error (1.2 mV) with the converter running at 1.8 MHz, its peak value would have to be 1.46V. A common-mode signal this large is much greater than that generally found in data aquisition systems.

### 3.2 Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock rising edges during the conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period.

### 3.3 Input Bypass Capacitors

Bypass capacitors at the inputs will average the current spikes noted in 3.2 and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full scale. For continuous conversions with a 1.8 MHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}$ pin* for high resistance sources (>1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a linear function of the differential input voltage.

### 3.4 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* if the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications (≤0.1 kΩ) a 4700 pF bypass capacitor at the inputs will prevent pickup due to series lead induction of a long wire. A 100Ω series resistor can be used to isolate this capacitor – both the R and the C are placed outside the feedback loop – from the output of an op amp, if used.

### 3.5 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 1 kΩ. Larger values of source resistance can cause undesired system noise

pickup. Input bypass capacitors, placed from the analog inputs to ground, can reduce system noise pickup but can create analog scale errors. See section 3.2, 3.3, and 3.4 if input filtering is to be used.

## 4.0 OFFSET AND REFERENCE ADJUSTMENT

### 4.1 Zero Offset

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V(−) input and applying a small magnitude positive voltage to the V(+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 00 0000 0000 to 00 0000 0001 and the ideal ½ LSB value (½ LSB = 2.45 mV for $V_{REF}$ = 5.0 $V_{DC}$).

The zero of the A/D normally does not require adjustment. However, for cases where $V_{IN(MIN)}$ is not ground and in reduced span applications ($V_{REF}$ < 5V), an offset adjustment may be desired. The converter can be made to output an all zero digital code for an arbitrary input by biasing the A/D's $V_{IN}(−)$ input at that voltage. This utilizes the differential input operation of the A/D.

### 4.2 Full Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}$ input for a digital output code that is just changing from 11 1111 1110 to 11 1111 1111.

### 4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/ 1024) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the $000_{HEX}$ $001_{HEX}$ code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(−)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input given by:

$$V_{IN}(+)\ FS\ adj = V_{MAX} - 1.5 \left[ \frac{(V_{MAX} - V_{MIN})}{1024} \right]$$

where $V_{MAX}$ = the high end of the analog input range and $V_{MIN}$ = the low end (the offset zero) of the analog range. (Both are ground referenced).

The $V_{REF}$ (or $V_{CC}$) voltage is then adjusted to provide a code change from $3FF_{HEX}$ to $3FE_{HEX}$. This completes the adjustment procedure.

For an example see the Zero-Shift and Span-Adjust circuit below.

## 5.0 POWER SUPPLIES

Noise spikes on the $V_{CC}$ supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter $V_{CC}$ pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the

## Functional Description (Continued)

system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and the other analog circuitry) will greatly reduce digital noise on the $V_{CC}$ supply.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to the digital ground. Any $V_{REF}$ bypass capacitors, analog input filters capacitors, or input signal shielding should be returned to the analog ground point.
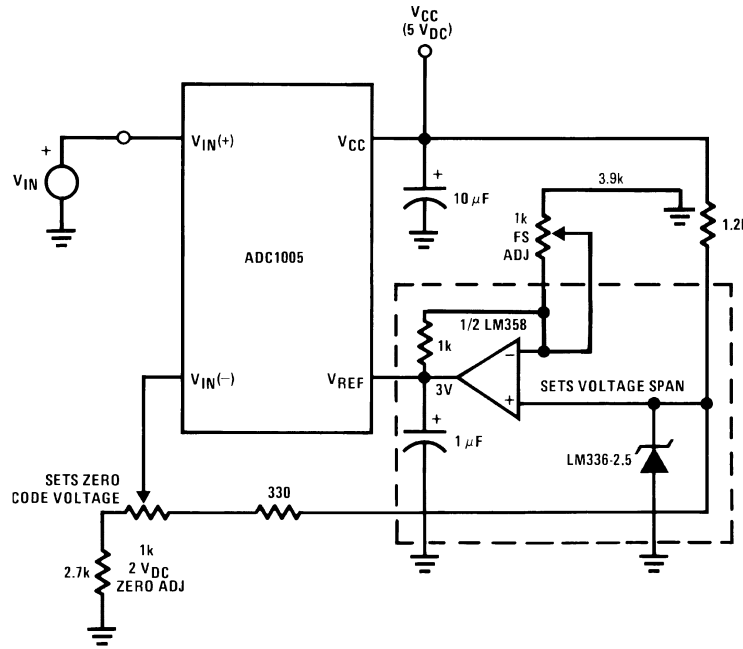


DS005261-16

**FIGURE 5. Zero-Shift and Span-Adjust (2V ≤ $V_{IN}$ ≤ 5V)**

## Typical Applications
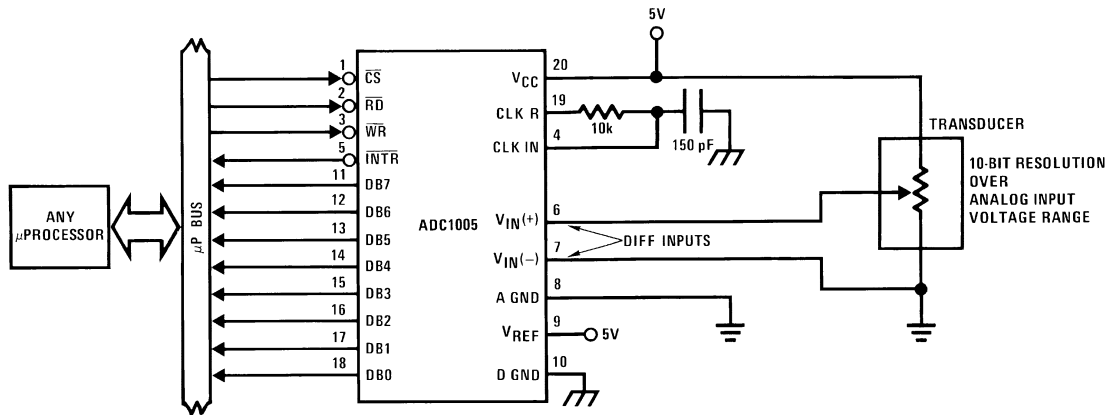


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# Typical Applications (Continued)
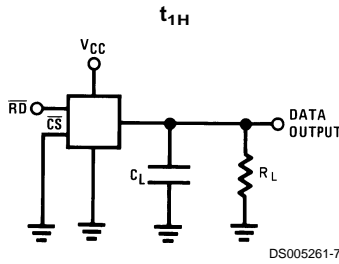
### Operating with Ratiometric Transducers



DS005261-14

$V_{IN}(-) = 0.15 \, V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq$ 85% of $V_{CC}$
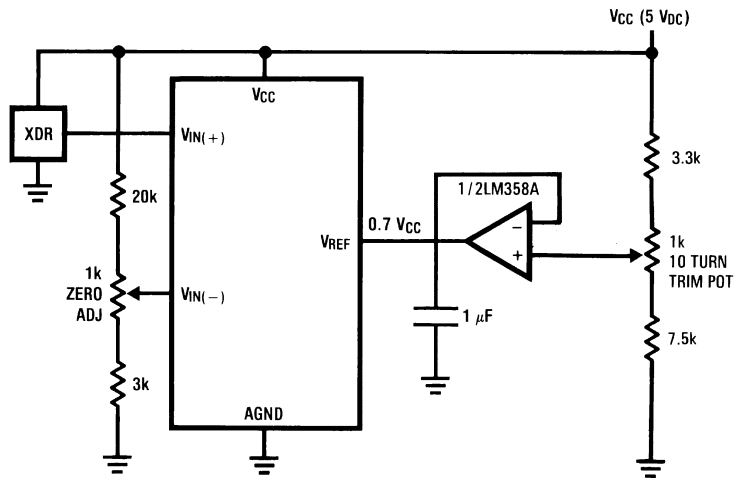
### Handling ±5V Analog Inputs



DS005261-15

# TRI-STATE Test Circuits and Waveforms

$t_{1H}$



DS005261-7

$t_r$=20 ns

$t_{IH}$, $C_L$=10 pF



DS005261-9

$t_{0H}$



DS005261-8

$t_r$=20 ns

$t_{IH}$, $C_L$=10 pF



DS005261-10

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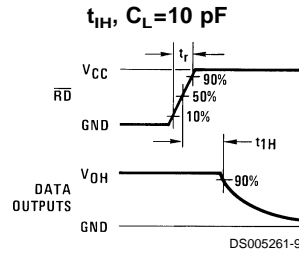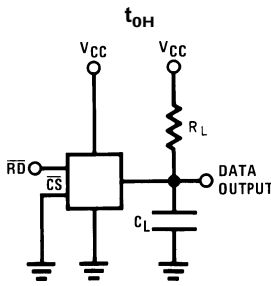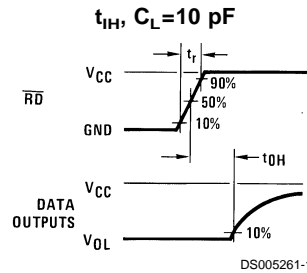
# Physical Dimensions inches (millimeters) unless otherwise noted

0.025
(0.635)
RAD

0.985
(25.019)
MAX

| 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |

0.220 — 0.310
(5.588 — 7.874)

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

0.005 — 0.020
(0.127 — 0.508)
RAD TYP

0.037 ± 0.005
(0.940 ± 0.127)

0.180
(4.572)
MAX

0.290 — 0.320
(7.366 — 8.128)

0.005
(0.127)
MIN

0.055 ± 0.005
(1.397 ± 0.127)

GLASS SEALANT

0.020 — 0.060
(0.508 — 1.524)

0.200
(5.080)
MAX

95° ± 5°

0.008 — 0.012
(0.203 — 0.305)

86° 94°

0.150
(3.810)
MIN

0.125 — 0.200
(3.175 — 5.080)

0.310 — 0.410
(7.874 — 10.41)

0.060
(1.524)
MAX
BOTH ENDS

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

J20A (REV M)

**Hermetic Dual-In-Line Package (J)**
**Order Number ADC1005BCJ, ADC1005BCJ-1,**
**ADC1005CCJ or ADC1005CCJ-1**
**NS Package Number J20A**

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