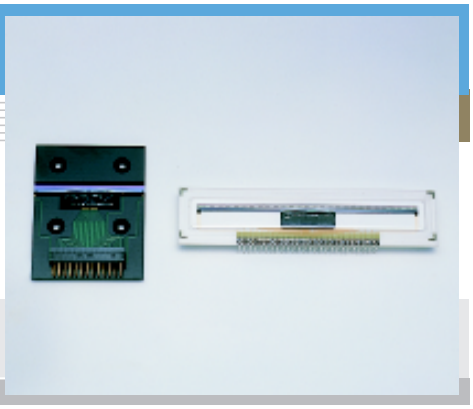
Photodiode array with amplifier
S6493/S6494 series



Photodiode arrays combined with a signal processing circuit chip

S6493 and S6494 series are Si photodiode arrays efficiently combined with a signal processing circuit. The signal processing circuit is formed on a single chip by the CMOS process, and includes a shift register, clamp circuit, hold circuit and charge amplifier array, thus allowing a simplified external circuit configuration.
The photocurrent from the photodiode array is fed to the charge amplifier connected to each element and is converted into a voltage.
The signal voltage is then sent to the clamp circuit and hold circuit, and is finally read out from the shift register in turn as a sequential video signal. The signal readout is performed by means of the charge storage method, so the output is proportional to the amount of light exposure (the product of incident light level and integration time). The vide output is a boxcar waveform which is low noise and easy to handle.
In addition, the readout gain can be selected from two levels by changing the voltage to the external input terminal. (The "high" gain is 10 times that of the "low" gain.) S6493 and S6494 series ensure easy operation since they can operate from a 5 V supply, and yet offer a maximum data rate of 250 kHz.

Features

- Four types are available
  S6493-64: 0.8 mm pitch × 64 ch
  S6493-128: 0.4 mm pitch × 128 ch
  S6494-64: 1.6 mm pitch × 64 ch
  S6494-128: 0.8 mm pitch × 128 ch
- Simultaneous integration by using a charge amplifier array
- Sequential readout with a shift register
- Integrated clamp circuit allows low noise and wide dynamic range
- Two gain levels can be selected
- Operates from single 5 V supply input
- S6493 series:
  Long active area can be configured by use of multiple arrays
  phosphor screen type is also available for X-ray detection
- Custom designed element size and pitch available
- Dedicated driver circuits are available

Applications

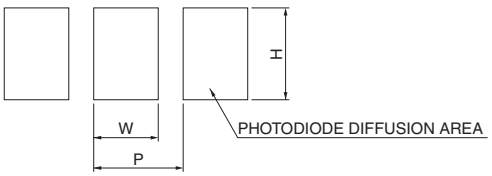
- Image or pattern recognition system

■ Mechanical specifications

Parameter	Symbol *1	S6493-64	S6493-128	S6494-64	S6494-128	Unit
Element pitch	P	0.8	0.4	1.6	0.8	mm
Element diffusion width	W	0.6	0.25	1.3	0.6	
Element height	H	0.8	0.4	1.6	0.8	
Number of elements	-	64	128	64	128	-
Active area length	-	51.2		102.4		mm

*1: Refer to following figure

■ Detail of elements



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■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage	Vdd	-0.3 to +7.0	V
Gain selection terminal voltage	Vgain		
Clock pulse voltage	Vϕ1, Vϕ2		
Start pulse voltage	Vϕst		
Reset pulse voltage	Vϕreset		
Hold pulse voltage	Vϕhold		
Sample pulse voltage	Vϕsample		
Clamp pulse voltage	Vϕclamp		
Operating temperature *2	Topr	-5 to +60	°C
Storage temperature	Tstg	-10 to +70	

*2: No condensation

■ Recommended terminal voltage

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.8	5	5.2	V
Gain selection terminal voltage	Low gain	Vgain (L)	Vdd-0.2	Vdd	Vdd+0.2	
	High gain	Vgain (H)	0	-	0.4	
Clock pulse voltage	High level	Vϕ1, Vϕ2	Vdd-0.2	Vdd	Vdd+0.2	
	Low level		0	-	0.4	
Start pulse voltage	High level	Vϕst	Vdd-0.2	Vdd	Vdd+0.2	
	Low level		0	-	0.4	
Reset pulse voltage	High level	Vϕreset	Vdd-0.2	Vdd	Vdd+0.2	
	Low level		0	-	0.4	
Hold pulse voltage	High level	Vϕhold	Vdd-0.2	Vdd	Vdd+0.2	
	Low level		0	-	0.4	
Sample pulse voltage	High level	Vϕsample	Vdd-0.2	Vdd	Vdd+0.2	
	Low level		0	-	0.4	
Clamp pulse voltage	High level	Vϕclamp	Vdd-0.2	Vdd	Vdd+0.2	
	Low level		0	-	0.4	

■ Electrical characteristics (Ta=25 °C, Vdd=5 V, Vϕ1=Vϕ2=Vϕreset=Vϕhold=Vϕclamp=Vϕsample=5 V)

Parameter	Symbol	S6493-64, S6494-64			S6493-128, S6494-128			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse frequency (video data rate)	fϕ1, fϕ2	15	-	250	15	-	250	kHz
Integration time	Ts	0.3	-	10	0.6	-	10	ms
Clock pulse line capacitance	Cϕ1, Cϕ2	-	15	-	-	30	-	pF
Video line capacitance	Cv	-	20	-	-	40	-	
Output impedance	Zo	-	3	-	-	3	-	kΩ
Current consumption	Idd	-	20	-	-	40	-	mA

■ Electrical and optical characteristics

Parameter		Symbol	S6493-64			S6493-128			S6494-64			S6494-128			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Spectral response range		λ	200 to 1000			200 to 1000			320 to 1000			320 to 1000			nm
Peak sensitivity wavelength		λp	-	720	-	-	720	-	-	720	-	-	720	-	nm
Dark output voltage *3	High gain	Vd	-	0.4	4	-	0.2	2	-	0.8	8	-	0.4	4	mV
	Low gain		-	0.04	0.4	-	0.02	0.2	-	0.08	0.8	-	0.04	0.4	mV
Saturation output voltage *3		Vsat	1.3	1.6	-	1.3	1.6	-	1.3	1.6	-	1.3	1.6	-	V
Saturation exposure *4, 5	High gain	Esat	-	1.2	-	-	5.8	-	-	0.28	-	-	1.2	-	mlx·s
	Low gain		-	12	-	-	58	-	-	2.8	-	-	12	-	mlx·s
Photo sensitivity *5	High gain	S	-	1300	-	-	270	-	-	5700	-	-	1300	-	V/lx·s
	Low gain		-	130	-	-	27	-	-	570	-	-	130	-	V/lx·s
Photo response non-uniformity *6		PRNU	-	-	20	-	-	20	-	-	20	-	-	20	%
Noise *7	High gain	N	-	0.2	-	-	0.2	-	-	0.3	-	-	0.3	-	mVrms
	Low gain		-	0.2	-	-	0.2	-	-	0.2	-	-	0.2	-	mVrms
Output offset voltage *8		Vos	2.5	3	3.5	2.5	3	3.5	2.5	3	3.5	2.5	3	3.5	V

[Ta=25 °C, Vdd=5 V, Vϕ1=Vϕ2=Vϕreset =Vϕhold =Vϕclamp =Vϕsample=5 V, Vgain=5 V (Low gain), 0 V (High gain), Data rate: 200 kHz]

*3: Integration time ts=1 ms

*4: Saturation output voltage and exposure are determined by the upper limit of the charge amplifier.

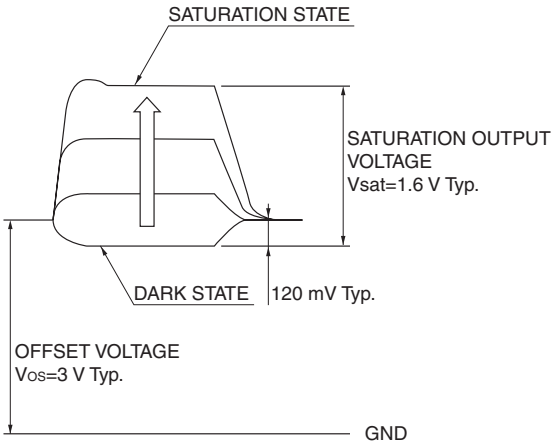
*5: Measured with a 2856 K tungsten lamp.

*6: When the photodiode array is exposed to uniform light which is 50 % of the saturation exposure, the Photo Response Non-Uniformity (PRNU) is defined as follows:
PRNU = (Vmax - Vmin)/Vaverage × 100 (%)
where Vaverage is the average output of all elements, Vmax is the output of the element that provides the maximum output, Vmin is the output of the element that provides the minimum output.

*7: Measured at a data rate of 50 kHz and integration time of 5 ms under dark condition.

*8: The output offset voltage is defined as shown in following figure (Output waveform of one element).

■ Output waveform of one element



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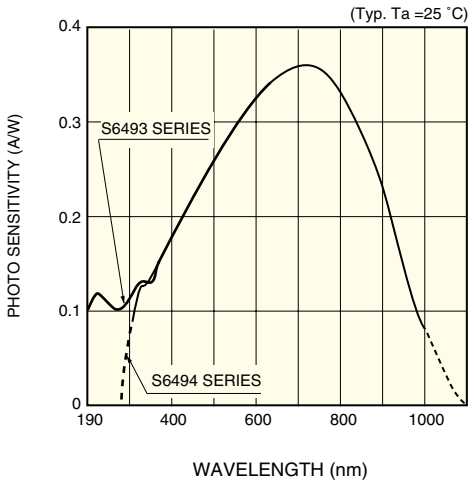
■ Spectral response



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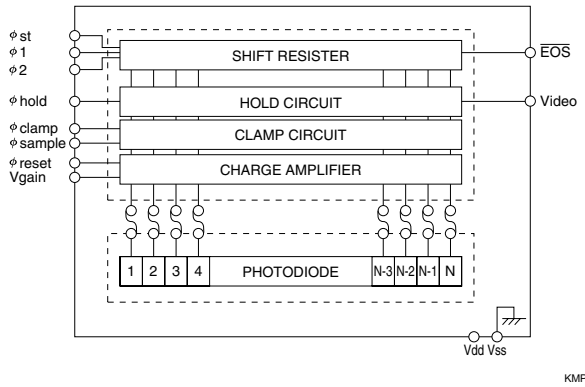
■ Driver circuit consideration

The following points must be taken into account when you use a driver circuit.

- The input pulse must meet the pulse conditions at the input terminal. Each pulse should be amplified by the buffer at a position as close to the input terminal as possible.
- The video output should undergo non-inverting amplification at the external readout circuit.
- Use of a JFET input type op amp is recommended. Make offset adjustment as necessary. In this case, it should be noted that the dark output level appears on the lower voltage side relative to the output offset voltage.

■ Block diagram



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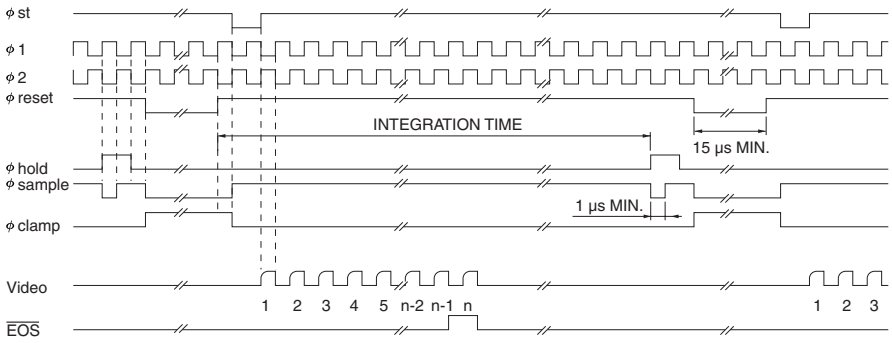
■ Recommended timing chart



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The operations of the S6493 and S6494 series devices can be divided into charge integration and readout operations, as follows:

● Charge integration operation

(1) When a φreset pulse is input, all elements in the integration amplifier are reset to start integration.
(2) When a φhold pulse is input, output from all elements of the integration amplifier is simultaneously sent to the output hold circuit.
(3) The charge integration time is equal to the time interval from the φreset pulse input to the φhold input.
(4) When another φreset pulse is input, the next integration starts.
(5) The φclamp and φsample pulses are needed to operate the clamp circuit.

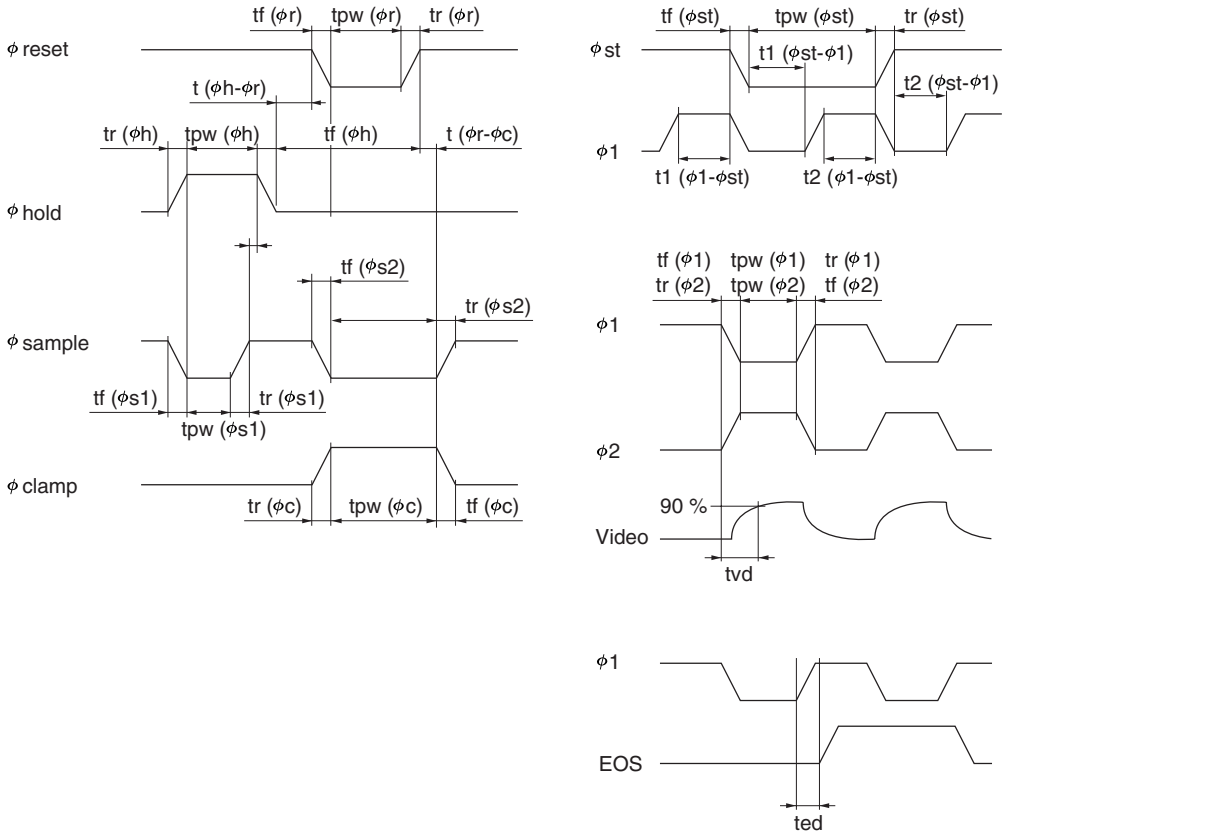
● Readout operation

(1) Under the condition that complimentary clock pulse φ1 and φ2 are being supplied, the shift register starts operation when a φst pulse is loaded. At this point, the φ1 pulse must rise only once while the φst is low.
(2) The shift register generates an address pulse train, and the output signal accumulated in the hold circuit is read out in turn from the first element, as a sequential signal from the Video terminal.
(3) The video signal is obtained as a boxcar waveform in synchronization with the positive-going edge of φ2.
(4) The φhold pulse cannot be loaded during readout operation (shift register operation).
(5) The EOS (end-of-scan) signal is output in synchronization with the negative-going edge of φ1 immediately before the output timing of the last element.

● Serial readout for multistage arrangement (S6493 series)

When multiple photodiode arrays are used in a serial arrangement, charge integration of each board can be performed at the same time, but the shift register of each board should be operated in sequence. The EOS pulse can be used as a start pulse for the next stage when it is inverted.
The video output terminal from all boards shoud be combined as one line via an analog switch and then connected to the external readout circuit. The analog switch should be used to select the video output only of the board being read out.

■ Timing chart



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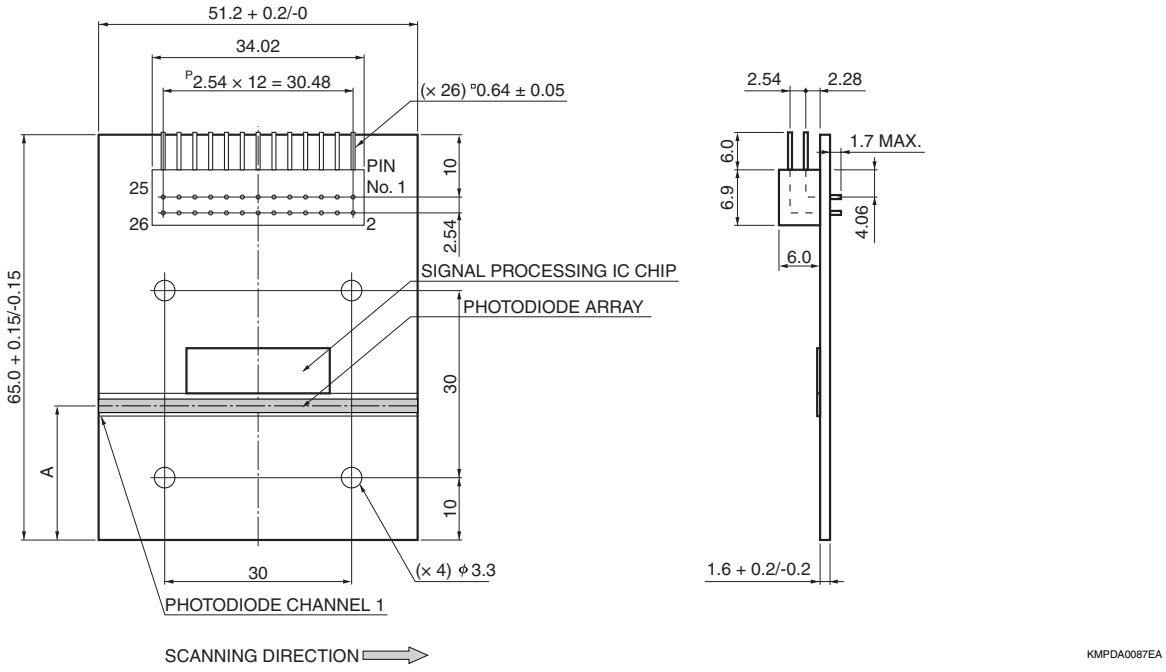
Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse width	tpw (ϕst)	300	-	-	ns
Rise/fall time of start pulse	tr (ϕst), tf (ϕst)	0	20	100	
Clock pulse (ϕ1, ϕ2) width	tpw (ϕ1, 2)	200	-	-	
Rise/fall time of clock pulse (ϕ1, ϕ2)	tr (ϕ1, 2), tf (ϕ1, 2)	0	20	100	
Hold pulse width	tpw (ϕh)	1	-	-	µs
Rise/fall time of hold pulse	tr (ϕh), tf (ϕh)	0	20	100	ns
Reset pulse width	tpw (ϕr)	15	-	-	µs
Rise/fall time of reset pulse	tr (ϕr), tf (ϕr)	0	20	100	ns
Sample pulse (1) width	tpw (ϕs1)	500	-	-	
Rise/fall time of sample pulse (1)	tr (ϕs1), tf (ϕs1)	0	20	100	
Sample pulse (2) width	tpw (ϕs2)	tpw (ϕr)	-	-	µs
Rise/fall time of sample pulse (2)	tr (ϕs2), tf (ϕs2)	0	20	100	ns
Clamp pulse width	tpw (ϕc)	tpw (ϕr)	-	-	µs
Rise/fall time of clamp pulse	tr (ϕc), tf (ϕc)	0	20	100	ns
Sample pulse (1) - hold pulse timing	t (ϕs1-ϕh)	0	-	-	
Hold pulse - reset pulse timing	t (ϕh-ϕr)	0	-	-	
Reset pulse - clamp pulse timing	t (ϕr-ϕc)	0	-	-	
Start pulse - clock pulse (ϕ1, ϕ2) timing 1	t1 (ϕst-ϕ1)	0	-	-	
Start pulse - clock pulse (ϕ1, ϕ2) timing 2	t2 (ϕst-ϕ1)	0	-	-	
Clock pulse (ϕ1, ϕ2) - start pulse timing 1	t1 (ϕ1-ϕst)	0	-	-	
Clock pulse (ϕ1, ϕ2) - start pulse timing 2	t2 (ϕ1-ϕst)	0	-	-	
Video delay time	tvd	-	1	-	µs
EOS pulse delay time	ted	-	100	-	ns

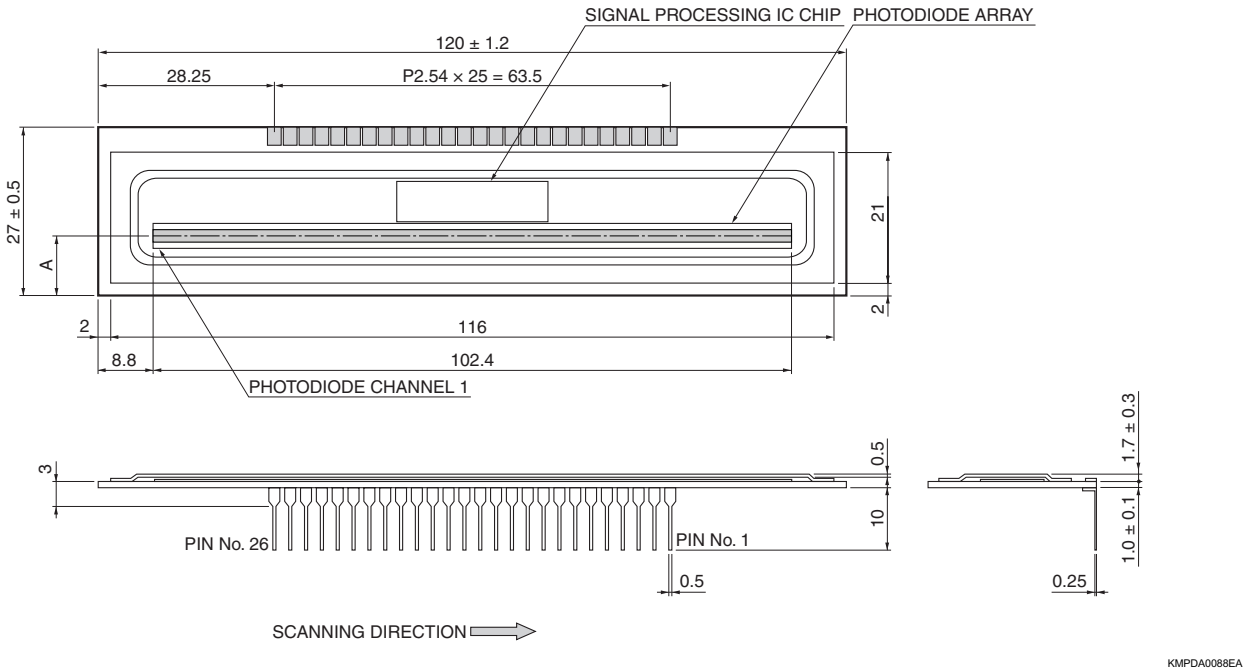
■ Dimensional outlines (unit: mm, tolerance unless otherwise noted: ±0.2)

S6493 series



A: Distance from the bottom of the board to the center of the active area S6493-64: 21.15 ± 0.2, S6493-128: 21.35 ± 0.2
Board: G10 glass epoxy
Connector: PS-26PE-D4LT1-PN1 (made by Japan Aviation Electronics)

S6494 series



A: Distance from the bottom of the board to the center of the active area S6494-64: 9.35 ± 0.2, S6494-128: 9.05 ± 0.2
Board: white ceramic
Window: borosilicate glass

■ Pin connections

● S6493 series

No.	Symbol
1	Vdd
2	Vdd
3	Vss
4	NC
5	Video
6	Vss
7	NC
8	ϕ1
9	NC
10	NC
11	Vdd
12	Vss
13	EOS
14	ϕ1
15	ϕ2
16	Vdd
17	ϕst
18	Vss
19	ϕ1
20	ϕhold
21	ϕ1
22	ϕclamp
23	ϕsample
24	ϕreset
25	Vgain
26	Vss

● S6494 series

No.	Symbol
1	Vss
2	Vdd
3	Vdd
4	Vdd
5	Vss
6	Video
7	Vss
8	ϕ1
9	Vdd
10	Vss
11	EOS
12	ϕ1
13	ϕ2
14	Vdd
15	ϕst
16	Vss
17	ϕ1
18	ϕhold
19	ϕ1
20	ϕclamp
21	ϕsample
22	ϕreset
23	Vgain
24	Vdd
25	Vdd
26	Vss

■ Pin assignment

Symbol	Assignment	Description
Vdd	Supply voltage	Voltage input
Vss	Ground	
ϕst	Start pulse	Negative-going pulse input
ϕ1	Clock pulse 1	Pulse input
ϕ2	Clock pulse 2	Pulse input $\overline{\phi 1}$
ϕreset	Reset pulse	Negative-going pulse input
ϕhold	Hold pulse	Positive-going pulse input
ϕsample	Sample pulse	Negative-going pulse input
ϕclamp	Clamp pulse	Positive-going pulse input
Vgain	Gain selection terminal voltage	Voltage input Vdd : low gain setting Vss : high gain setting
Video	Video output	Positive-going output from positive potential, boxcar waveform
EOS	End of scan	Positive-going pulse output

■ Precautions for use

(1) The signal processing circuit chips of the S6493 and S6494 series are protected against static electricity. However, in order to prevent possible damage to the chip, implement electrostatic countermeasures such as grounding of the operator, work table and tools. Furthermore, the devices must be protected against surge voltages from external equipment.

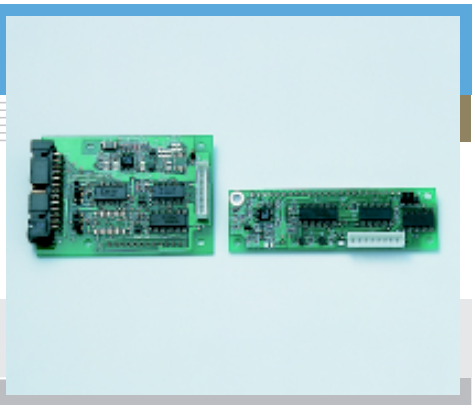
(2) S6493 series

Since the photodiode array chip is not protected, handle it carefully so it will not become contaminated or scratched.Photodiode array performance may deteriorate if operated at high temperatures and humidity, so the housing should be designed to be airtight. The signal processing circuit chip and its wire bonding are covered with a resin coating for protection, but never touch these portions. In addition, take care when installing the board so that it does not warp.

(3) S6494 series

If the input window becomes dirty or scratched, the output uniformity may deteriorate. Avoid touching the window with bare hands. Cleaning the window surface before use with cloth, cotton swab or paper moistened with ethyl alcohol is advised. Wiping the window with dry cloth may generate static electricity and therefore should be avoided.

Driver circuit for photodiode array with amplifier
C6785, C6495



Drive a photodiode array with amplifier by simple signal inputs

The C6785 and C6495 are driver circuits specifically designed for use with Hamamatsu photodiode arrays with amplifier. (The C6785 is for the S6493 series and the C6495 is for the S6494 series.) Both the C6785 and C6495 include a signal generator that provides timing pulses used to drive the sensor and a signal processing circuit that performs video signal amplification and DC restoration. The signal inputs required are start pulse (START), clock pulse (CLK) and +5 V.

Features

- Ideally suited for use with a photodiode array with amplifier
  C6785: for S6493 series
  C6495: for S6494 series
- Simple operation (with start pulse, clock pulse and +5 V)
- Can be installed on the reverse side of a photodiode array with amplifier
- Compact size
- Gain of a photodiode array with amplifier is selectable from PC board

Applications

- Operation of a photodiode array with amplifier

■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage	Vd	7	V
Operating temperature	Topr	50	°C
Storage temperature	Tstg	60	°C

■ Electrical characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit
Input	Supply Voltage (for digital circuit)	Vd	4.9	5	5.5	V
	Start pulse (start) voltage	Vst (H)	3.5	-	-	V
		Vst (L)	-	-	1.5	
	Start pulse width	tpw-st	1/f-CLK	-	-	s
	Start pulse rise/fall time	tr-st, tf-st	-	-	500	ns
	Clock pulse (clk) voltage	Vclk (H)	3.5	-	-	V
		Vclk (L)	-	-	1.5	
	Clock pulse frequency	f-CLK	30	-	500	kHz
	Clock pulse width	Tpw-CLK	30	-	-	ns
	Clock pulse rise/fall time	tr-c, tf-c	-	-	500	ns
output	Trigger pulse (trigger) voltage	Vtrig (H)	4.5	5	5.5	V
		Vtrig (L)	0	-	0.8	
	Trigger pulse rise /fall time	tr-tri, tf-tri	-	-	500	ns
	Data video data rate	DVRATE	-	100	250	kHz

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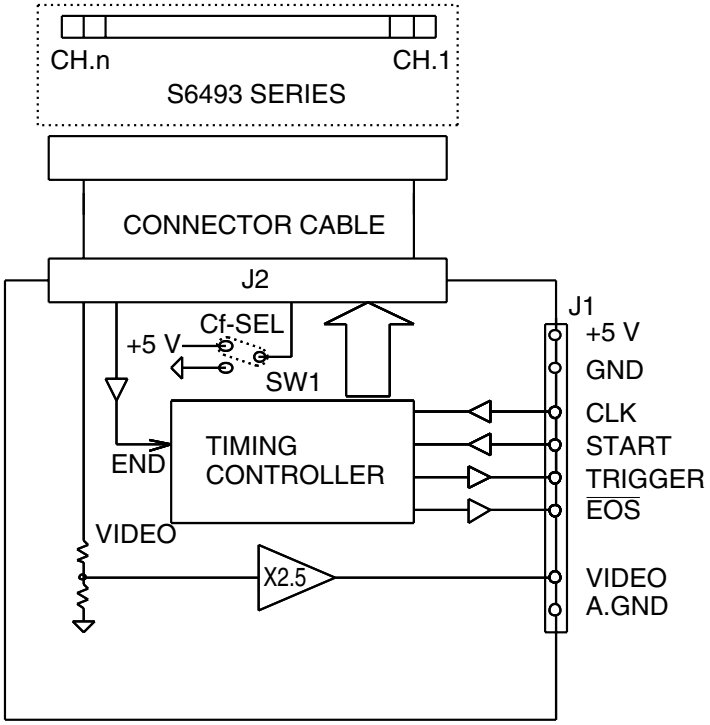
■ Block diagram

C6785



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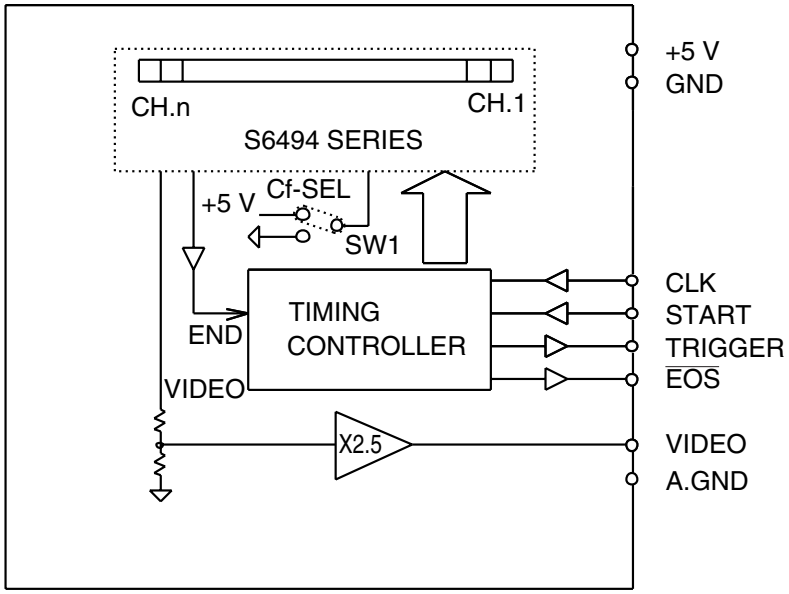
C6495



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■ Pin connections

● J1, CN1: 5483-08AX (made by Molex)

Pin No.	Signal	Input/Output	Description
1	CLK	Input	HCMOS compatible pulse for synchronizing the circuit and sensor
2	START	Input	HCMOS compatible positive logic pulse for initializing the circuit
3	TRIGGER	Output	HCMOS compatible positive logic pulse for A/D conversion
4	$\overline{\text{EOS}}$	Output	HCMOS compatible negative logic pulse used as end-of-scan signal
5	+5 V	Input	Supply voltage: +5 V Max. 70 mA
6	GND	-	Circuit ground
7	VIDEO	Output	Video signal output positive-going pulse
8	A.GND	-	Circuit ground used to ground the coaxial line of VIDEO

A connector 5480-08 that mates with the 5483-08AX connector is supplied with the C6785 and C6495.

● J2: XG4C-2634 (made by OMRON)

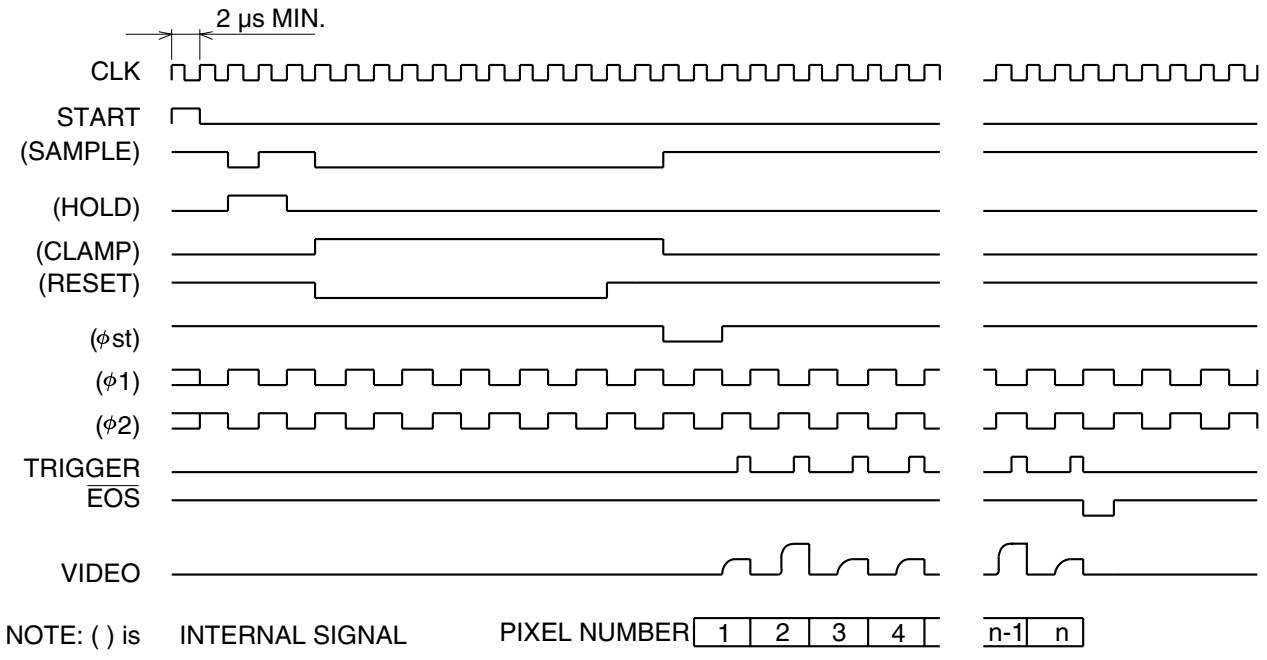
Pin No.	Signal	Input/Output	Description
1	Vdd	Output	Sensor: supply voltage for CMOS IC
2	Vdd	Output	Sensor: supply voltage for CMOS IC
3	Vss	Output	Sensor ground
4	NC	-	No connection
5	Video	Input	Sensor video signal output
6	Vss	Output	Sensor ground
7	NC	-	No connection
8	ϕ1	Output	Sensor: clock pulse for shift register scan, HCMOS compatible
9	NC	-	No connection
10	NC	-	No connection
11	Vdd	Output	Sensor: supply voltage for CMOS IC
12	Vss	Output	Sensor ground
13	EOS	Input	Sensor: end-of-scan signal
14	ϕ1	Output	Sensor: clock pulse for shift register scan, HCMOS compatible
15	ϕ2	Output	Output sensor: clock pulse for shift register scan, HCMOS compatible
16	Vdd	Output	Output sensor: supply voltage for CMOS IC
17	ϕst	Output	Output sensor: video signal output start pulse, HCMOS compatible
18	Vss	-	Sensor ground
19	ϕ1	Output	Sensor: clock pulse for shift register scan, HCMOS compatible
20	ϕhold	Output	Sensor: charge amplifier output hold signal, HCMOS compatible
21	ϕ1	Output	Sensor: clock pulse for shift register scan, HCMOS compatible
22	ϕclamp	Output	Sensor: charge amplifier output clamp signal, HCMOS compatible
23	ϕsample	Output	HCMOS compatible, positive logic pulse for initializing the circuit
24	ϕreset	Output	Sensor: charge amplifier output reset signal, HCMOS compatible
25	Vgain	Output	Sensor gain switching: H=gain “low”, L=gain “high”
26	Vss	-	Sensor ground

A connector XG4M-2630-T that mates with the XG4C-2634 connector is supplied with the C6785 and C6495.

● CN2: XR2C (made by OMRON)

Pin No.	Signal	Input/Output	Description
1	Vss	-	Sensor ground
2	Vdd	Output	Sensor: supply voltage for CMOS IC
3	Vdd	Output	Sensor: supply voltage for CMOS IC
4	Vdd	Output	Sensor: supply voltage for CMOS IC
5	Vss	-	Sensor ground
6	Video	Input	Sensor video signal output
7	Vss	-	Sensor ground
8	ϕ1	Output	Sensor: clock pulse for shift register scan
9	Vdd	Output	Sensor: supply voltage for CMOS IC
10	Vss	-	Sensor ground
11	EOS	Input	Sensor: end-of-scan signal
12	ϕ1	Output	Sensor: clock pulse for shift register scan
13	ϕ2	Output	Sensor: clock pulse for shift register scan
14	Vdd	Output	Sensor: supply voltage for CMOS IC
15	ϕst	Output	Sensor: shift register scan start pulse
16	Vss	-	Sensor ground
17	ϕ1	Output	Sensor: clock pulse for shift register scan
18	ϕhold	Output	Sensor: charge amplifier output hold signal
19	ϕ1	Output	Sensor: clock pulse for shift register scan
20	ϕclamp	Output	Sensor: charge amplifier output clamp signal
21	ϕsample	Output	Sensor: charge amplifier output sample signal
22	ϕreset	Output	Sensor: charge amplifier output reset signal
23	Vgain	Output	Sensor gain switching: H=gain “low”, L=gain “high”
24	Vdd	Output	Sensor: supply voltage for CMOS IC
25	Vpd	Output	Reverse voltage for photodiode array
26	Vss	-	Sensor ground

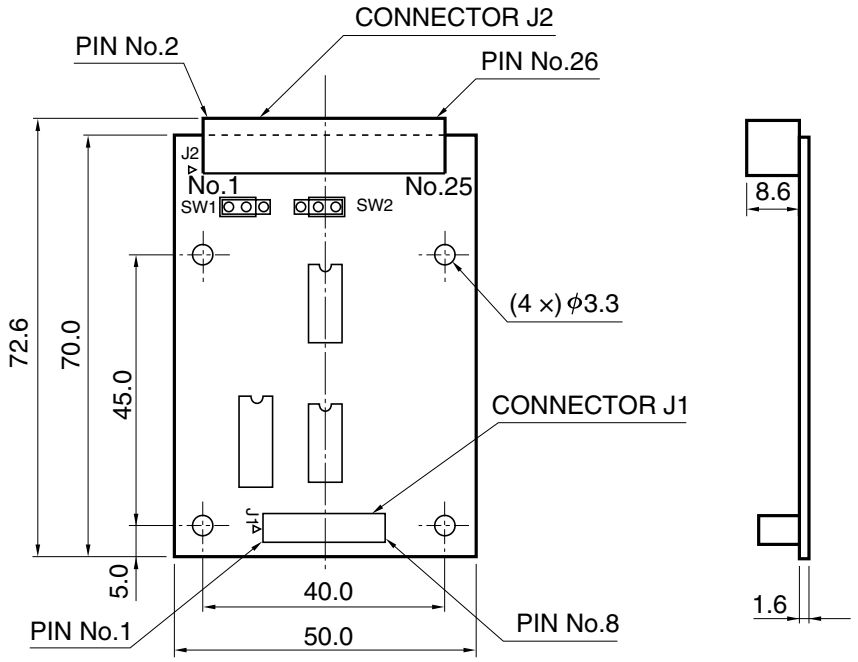
■ Pulse timing



KACCC0058EA

■ Dimensional outlines (unit: mm, tolerance unless otherwise noted: ±0.2)

C6785



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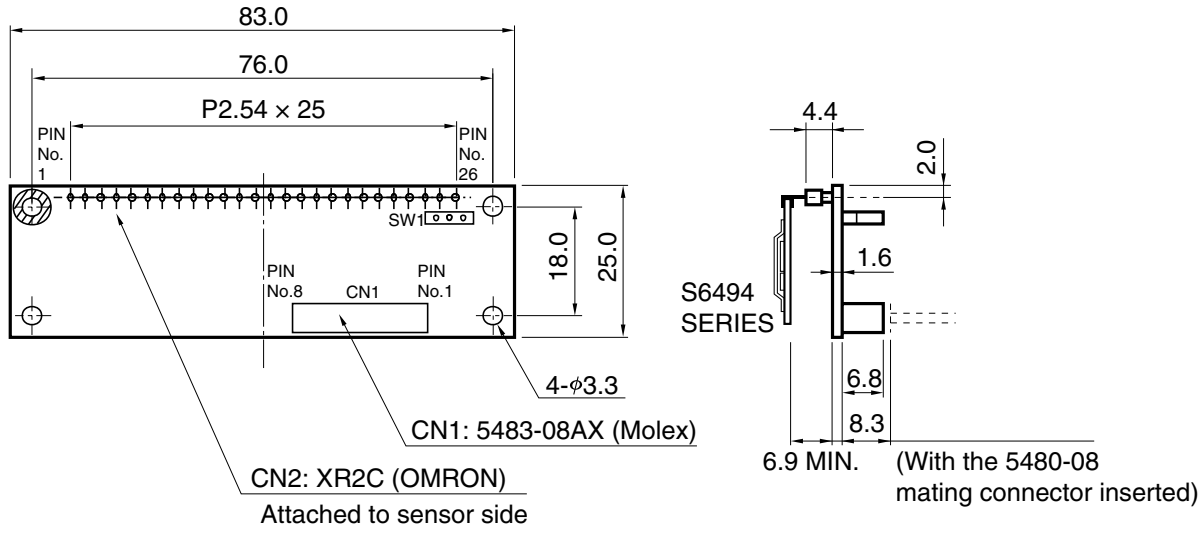
C6495

COMPONENT SIDE



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