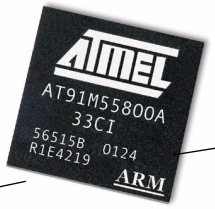
Errata Sheet V1.0

This Errata Sheet refers to:

- The following datasheets:
  AT91M55800A Summary, Rev. 1745AS–07/01
  AT91M55800A, Rev. 1745A–07/01
  AT91M55800A, Electrical Characteristics Rev. 1776A–07/01
- 176-lead TQFP and 176-ball BGA devices with the following markings:



AT91M55800A-33AI
AT91M55800A-33CI

Internal Product
Reference 56515B

6. Warning: Additional NWAIT Constraints

When the NWAIT signal is asserted during an external memory access, the following EBI behavior is correct:

– NWAIT is asserted before the first rising edge of the master clock and respects the NWAIT to MCKI rising setup timing as defined in the Electrical Characteristics datasheet.

– NWAIT is sampled inactive and at least one standard wait state remains to be executed, even if NWAIT does not meet the NWAIT to first MCKI rising setup timing (i.e., NWAIT is asserted only on the second rising edge of MCKI).

In these cases, the access is delayed as required by NWAIT and the access operations are correctly performed.

In other cases, the following erroneous behavior occurs:

– 32-bit read accesses are not managed correctly and the first 16-bit data sampling takes into account only the standard wait states. 16- and 8-bit accesses are not affected.

– During write accesses of any type, the NWE rises on the rising edge of the last cycle as defined by the programmed number of wait states. However, NWAIT assertion does affect the length of the total access. Only the NWE pulse length is inaccurate.

At maximum speed, asserting the NWAIT in the first access cycle is not possible, as the sum of the timings “MCKI Falling to Chip Select” and “NWAIT setup to MCKI rising” are generally higher than one half of a clock period. This leads to using at least one standard wait state. However, this is not sufficient except to perform byte or half-word read accesses. Word and write accesses require at least two standard wait states.

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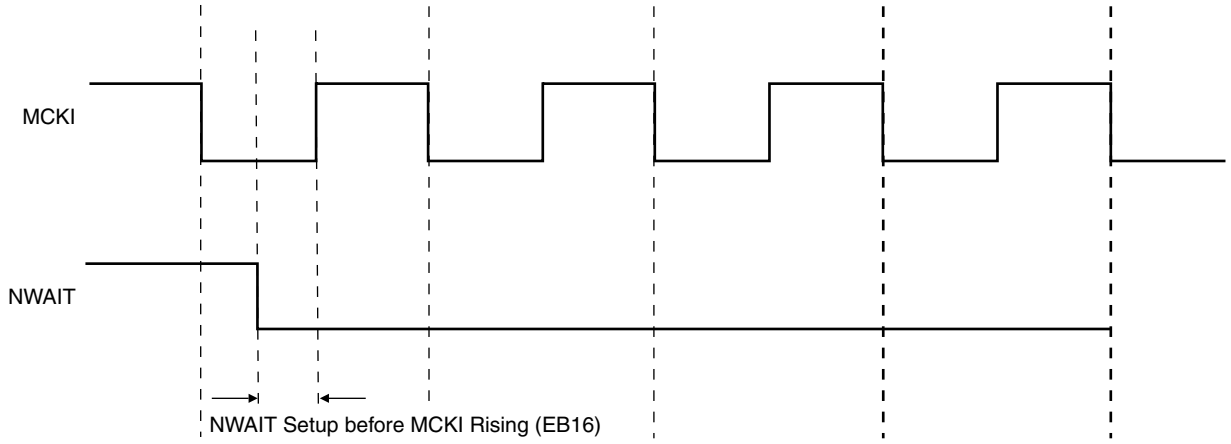
The following waveforms further explain the issue:

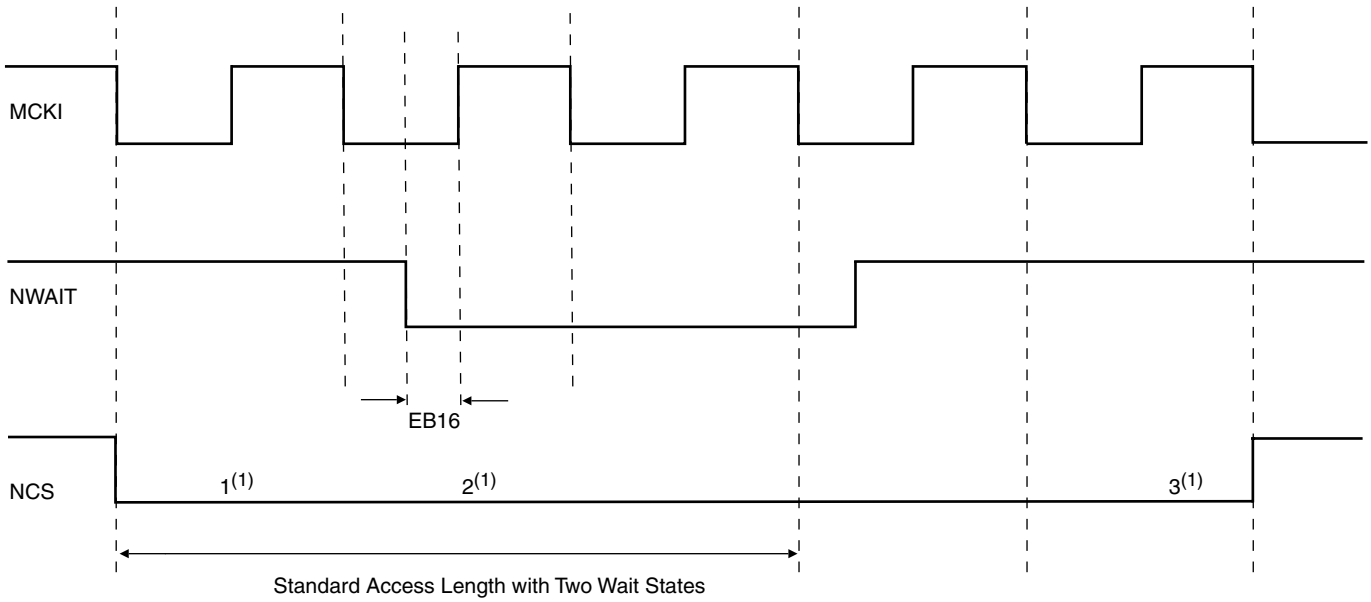
If the NWAIT setup time is satisfied on the first rising edge of MCKI, the behavior is accurate. The EBI operations are not affected when the NWAIT rises.

Figure 1. NWAIT Rising



If the NWAIT setup time is satisfied on the following edges of MCKI and if at least one standard wait state remains to be executed, the behavior is accurate. In the following example, the number of standard wait states is two. The NWAIT setup time on the second rising edge of MCKI must be met.

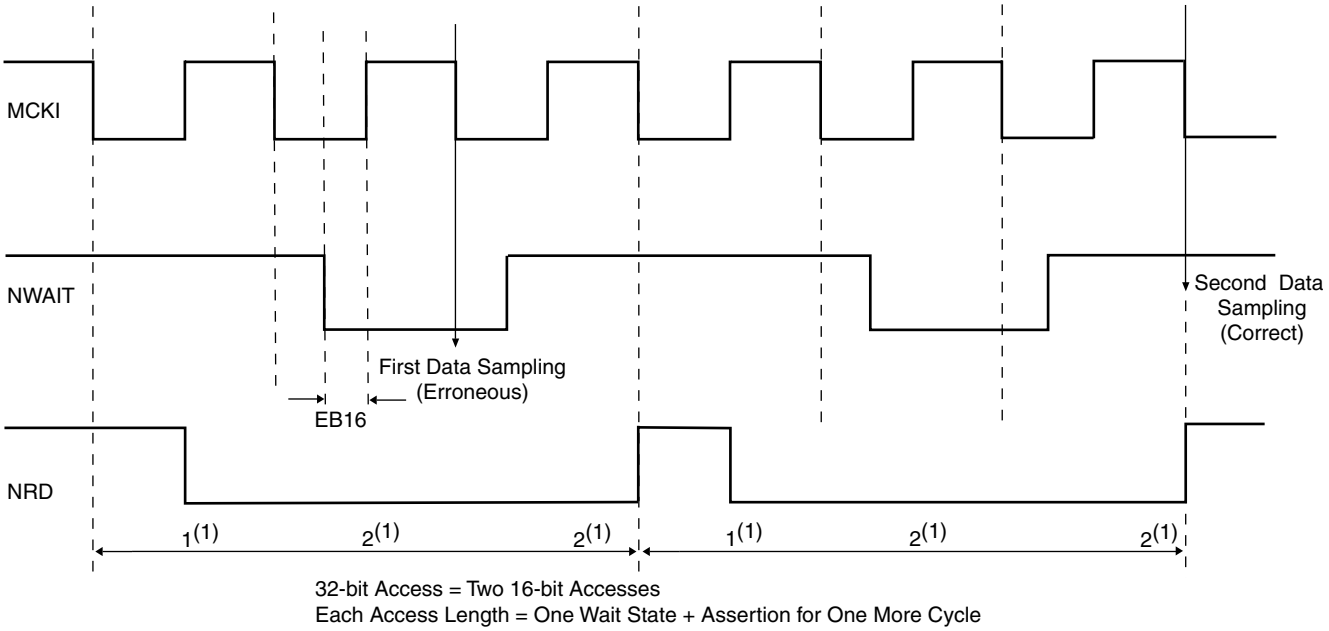
Figure 2. Number of Standard Wait States is Two



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during a 32-bit read access, the first 16-bit data is read at the end of the standard 16-bit read access. In the following example, the number of standard waits is one. NWAIT assertions do affect both NRD pulse lengths, but first data sampling is not delayed. The second data sampling is correct.

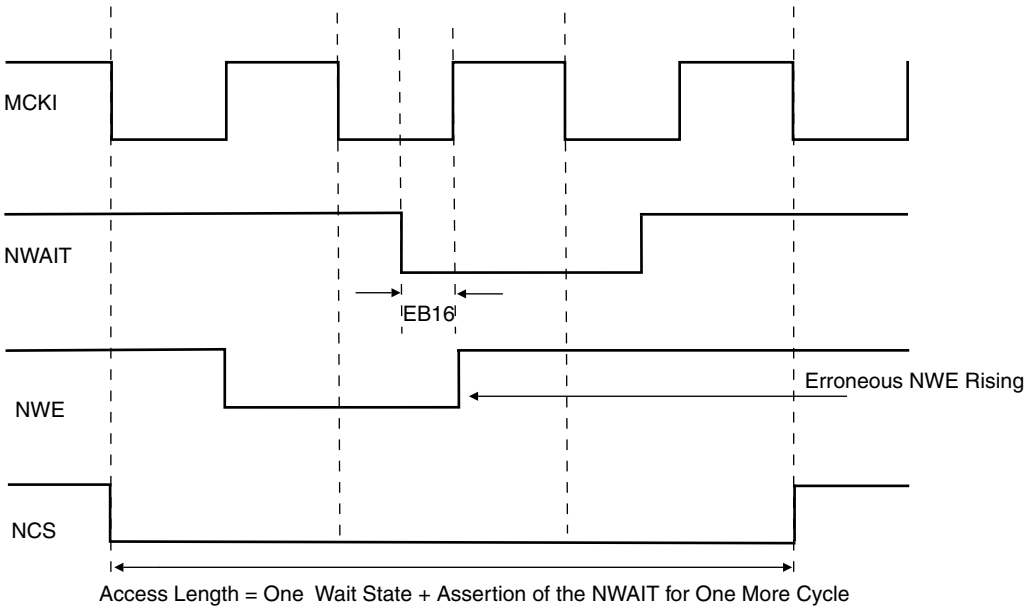
Figure 3. Number of Standard Wait States is One



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during write accesses, the NWE signal is not affected by the NWAIT assertion. The following example illustrates the number of standard wait states. NWAIT is not asserted during the first cycle, but is asserted at the second and last cycle of the standard access. The access is correctly delayed as the NCS line rises accordingly to the NWAIT assertion. However, the NWE signal waveform is unchanged, and rises too early.

Figure 4. Description of the Number of Standard Wait States



5. Unpredictable Result in APMC State Machine on Switch from Oscillator to PLL

An automatic switch from the main oscillator output (CSS = 1) may cause an unpredictable result in the APMC state machine. The automatic PLL to PLL transition is also effected by this problem.

Problem Fix/Workaround

The user must either wait for the PLL lock flag to be set in the APMC status register or switch to an intermediate 32 kHz oscillator output (CSS = 0).

4. Clock Switching with the Prescaler in the APMC is not Permitted

Switching from the selected clock (PRES = 0) to the selected clock divided by 4 (PRES = 2), 8 (PRES = 3) or 64 (PRES = 6) may lead to unpredictable results.

Problem Fix/Workaround

First, the user should switch to any other value (PRES = 1, 4 or 5) and wait for the actual switch to perform (at least 64 cycles of the selected clock). Then, the user can write the final prescaler value.

3. Initializing SPI in Master Mode May Cause a Mode Fault Detection

Problem Fix/Workaround

In order to prevent this error, the user must pull up the PA26/NPCS0/NSS pin to the V_{DDIO} power supply.

2. V_{DDBU} Consumption is not Guaranteed

The battery supply voltage consumption is not guaranteed in the case of internal peripheral accesses.

Problem Fix/Workaround

The user should minimally access the Advanced Peripheral Bus by using an interrupt-driven driver rather than polling methods.

1. SPI in Slave Mode does not Work

In transmission, the data to be transmitted (written in SP_TDR) is transferred in the shift register and, consequently, the TDRE bit in SP_SR is set to 1. Though the transfer has not begun, when the following data are written in SP_TDR, they are also transferred into the shift register, crushing the precedent data and setting the bit TDRE to 1.

Problem Fix/Workaround

No problem fix/workaround to propose.

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