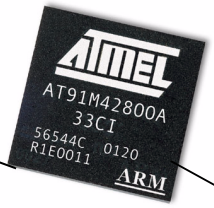
Errata Sheet V1.0

This Errata Sheet refers to:

- The following datasheets:
  AT91M42800A Summary, Rev. 1779AS–06/01
  AT91M42800A, Rev. 1779A–06/01
  AT91M42800A, Electrical Characteristics, Rev. 1776A–08/01
- 144-lead TQFP and 144s-ball BGA devices with the following markings:



Internal Product Reference 56544C

AT91M42800A-33AI
AT91M42800A-33CI

9. Warning: Additional NWAIT Constraints

When the NWAIT signal is asserted during an external memory access, the following EBI behavior is correct:

– NWAIT is asserted before the first rising edge of the master clock and respects the NWAIT to MCKI rising setup timing as defined in the Electrical Characteristics datasheet.

– NWAIT is sampled inactive and at least one standard wait state remains to be executed, even if NWAIT does not meet the NWAIT to first MCKI rising setup timing (i.e., NWAIT is asserted only on the second rising edge of MCKI).

In these cases, the access is delayed as required by NWAIT and the access operations are correctly performed.

In other cases, the following erroneous behavior occurs:

– 32-bit read accesses are not managed correctly and the first 16-bit data sampling takes into account only the standard wait states. 16- and 8-bit accesses are not affected.

– During write accesses of any type, the NWE rises on the rising edge of the last cycle as defined by the programmed number of wait states. However, NWAIT assertion does affect the length of the total access. Only the NWE pulse length is inaccurate.

At maximum speed, asserting the NWAIT in the first access cycle is not possible, as the sum of the timings “MCKI Falling to Chip Select” and “NWAIT setup to MCKI rising” are generally higher than one half of a clock period. This leads to using at least one standard wait state. However, this is not sufficient except to perform byte or half-word read accesses. Word and write accesses require at least two standard wait states.

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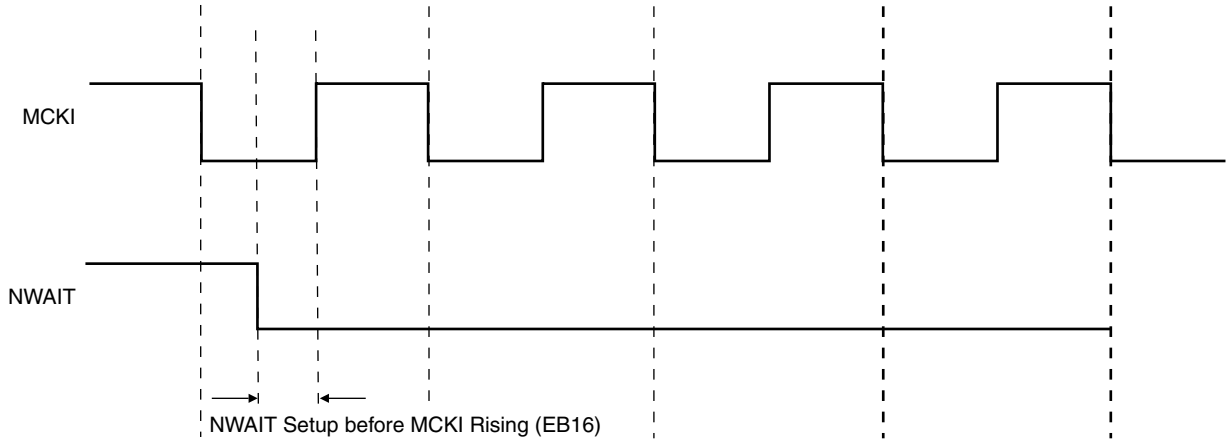
The following waveforms further explain the issue:

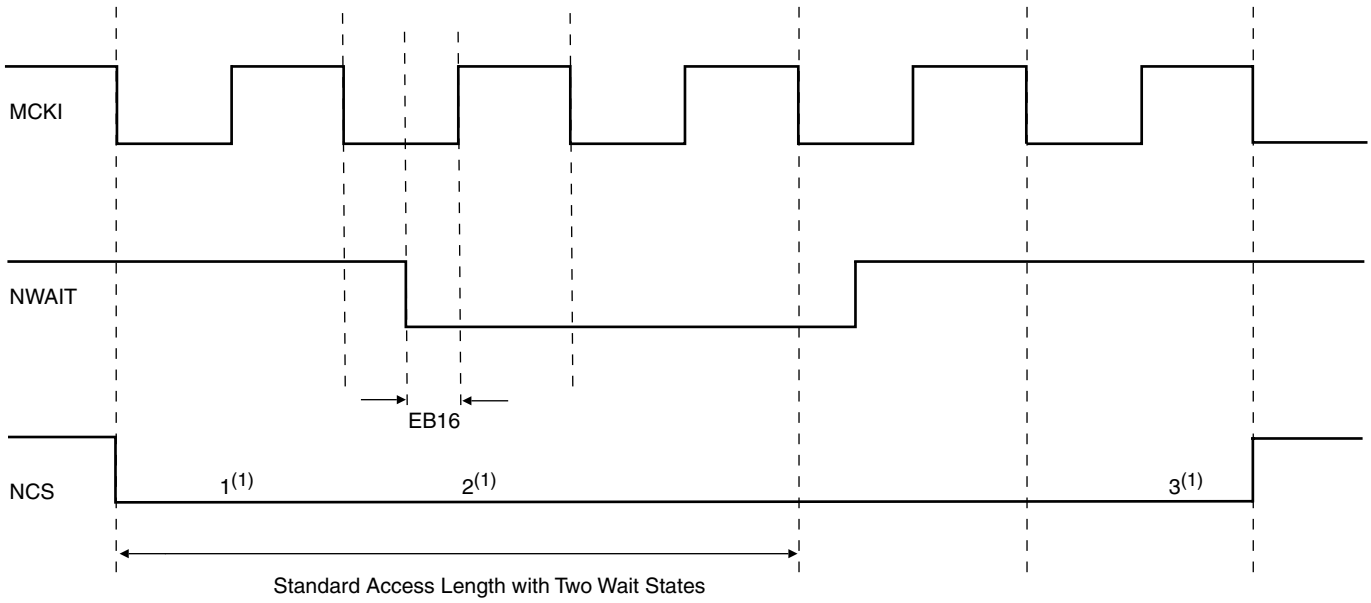
If the NWAIT setup time is satisfied on the first rising edge of MCKI, the behavior is accurate. The EBI operations are not affected when the NWAIT rises.

Figure 1. NWAIT Rising



If the NWAIT setup time is satisfied on the following edges of MCKI and if at least one standard wait state remains to be executed, the behavior is accurate. In the following example, the number of standard wait states is two. The NWAIT setup time on the second rising edge of MCKI must be met.

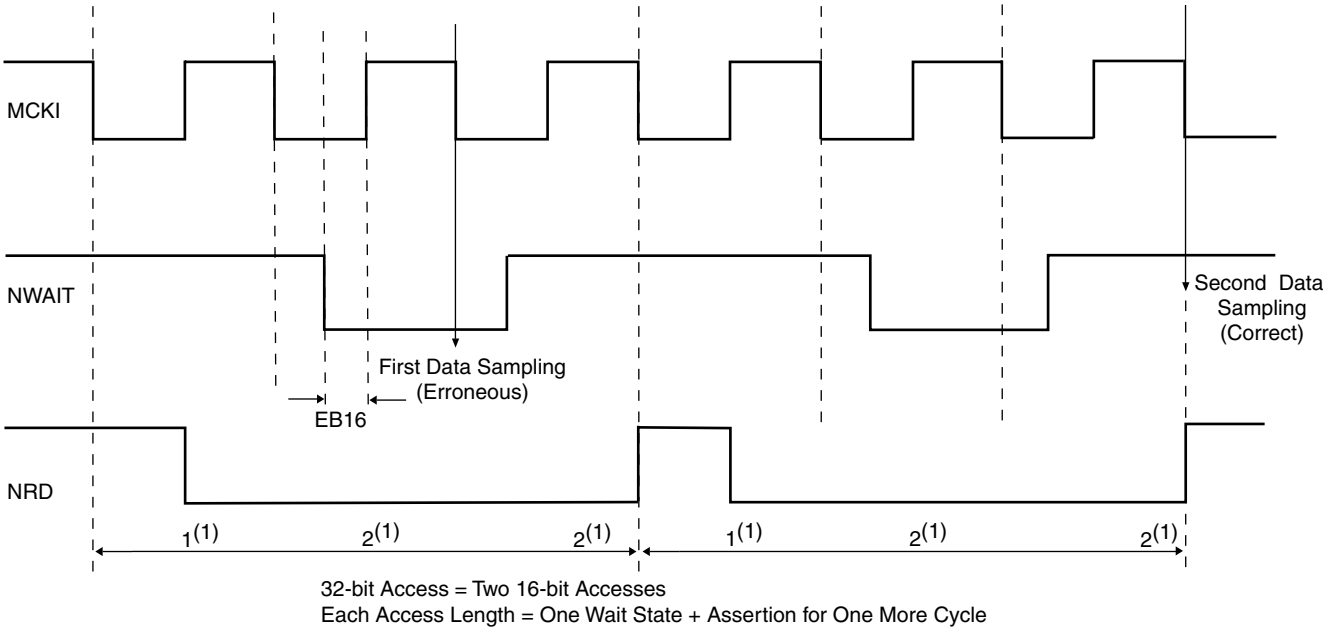
Figure 2. Number of Standard Wait States is Two



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during a 32-bit read access, the first 16-bit data is read at the end of the standard 16-bit read access. In the following example, the number of standard waits is one. NWAIT assertions do affect both NRD pulse lengths, but first data sampling is not delayed. The second data sampling is correct.

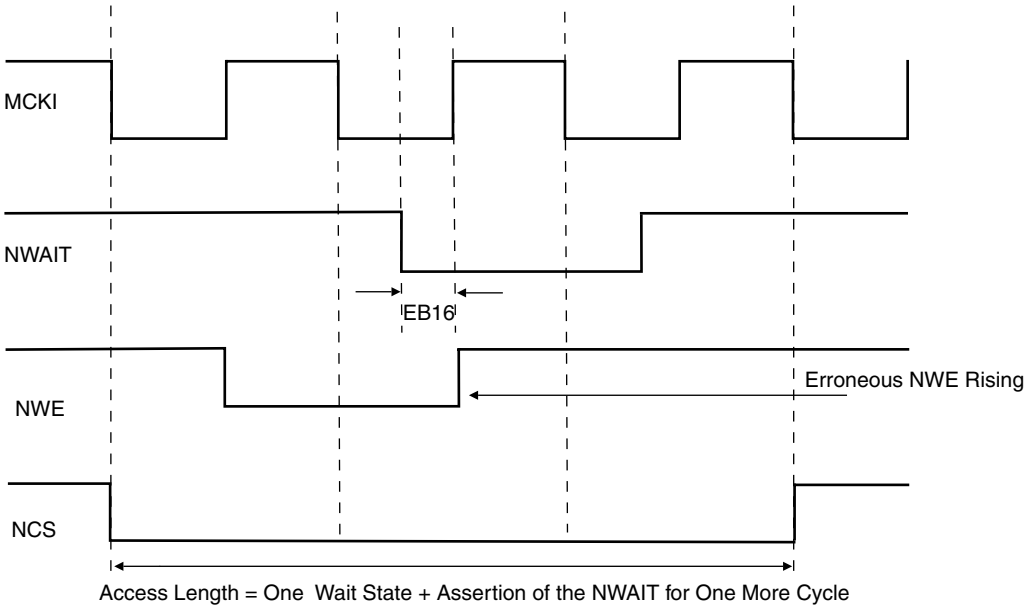
Figure 3. Number of Standard Wait States is One



Note: 1. These numbers refer to the standard access cycles.

If the first two conditions are not met during write accesses, the NWE signal is not affected by the NWAIT assertion. The following example illustrates the number of standard wait states. NWAIT is not asserted during the first cycle, but is asserted at the second and last cycle of the standard access. The access is correctly delayed as the NCS line rises accordingly to the NWAIT assertion. However, the NWE signal waveform is unchanged, and rises too early.

Figure 4. Description of the Number of Standard Wait States



8. Possible Glitches on MCKO while Commuting Clock

Unpredictable transitional pulses may occur on the MCKO pin when modifying the MCKOSS field in the PMC Clock Generator Mode Register. The length of these glitches can be lower than the lowest period of the selected or current clock. When switching from the Slow Clock (i.e., after reset) to any of the PLL outputs (inverted or divided by 2), a pulse of less than 10 ns is output on the pin MCKO.

Problem Fix/Workaround

The glitch description above is merely a user warning/possibility. If the glitches do occur, there is no Problem Fix/Workaround to propose.

7. Initializing SPI in Master Mode May Cause Problems

Initializing the SPI in master mode may cause a mode fault detection.

Problem Fix/Workaround

In order to prevent this error, the user should pull up the PA14/NPCSA0/NSSA pin for SPIA or the PA21/NPCSA0/NSSB pin for SPIB to the V_{DDIO} power supply.

6. Break is Sent before Last Written Character

When the Start Break command is activated in the USART Control Register and while a character is in the USART Transmit Holding Register, the break is transmitted before the character.

Problem Fix/Workaround

The user must wait for the TXEMPTY flag in the USART Status Register before sending a break command.

5. End of Break is not Guaranteed

When performing a Stop Break command, the USART transmitter normally inserts a “12-bit at level 1” sequence after the break. This feature is not guaranteed.

Problem Fix/Workaround

The user must use the Time Guard programmed at the value 12.

4. SCK is Ignored at 32 kHz

If the origin of the Master Clock is the Slow Clock, the USART Channels cannot be synchronized with a clock that comes from the SCK pin.

Problem Fix/Workaround

No problem fix/workaround to propose.

3. SCK Maximum Frequency Relative to MCK in Synchronous Mode

In USART Synchronous Mode, the external clock frequency (SCK) must be at least 10 times lower than the Master Clock.

Problem Fix/Workaround

No problem fix/workaround to propose.

2. PIO Input Filters are not Bit-to-bit Selectable

The PIO input filters are enabled and disabled only for all of the PIO input pins and not individually. To activate them, the user must write 0x0001 in the PIO IFER and 0x0001 in the PIO IFDR to deactivate them.

Problem Fix/Workaround

No problem fix/workaround to propose.

1. PIO Multi-drive Capability not Usable

The PIO multi-drive capability does not work in PIO mode or in peripheral mode.

Problem Fix/Workaround

No practical workaround proposed.

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