Features

- **Low Power Consumption**
- **Calendar from 1900 to 2099**
- **Year 2000 Compliant**
- **Programmable Periodic Interrupt Alarm Interrupt**
- **AVR® User Interface Bus**
- **Full Asynchronous Design**
- **Full Scan Testable**
- **Very Small Silicon Area**
- **Test Vectors: at Least 93% Fault Coverage**
- **Designed for Digital Keypad Applications (Parallel Load)**

Description

The Real Time Clock (RTC) peripheral is designed for use with the AVR embedded RISC core. It combines a complete time-of-day clock with alarm and a two-hundred year Gregorian calendar, complemented by a programmable periodic interrupt. The alarm and calendar registers are accessed by an 8-bit data bus.

The time and calendar values are coded in Binary-Coded Decimal (BCD) format. The time format is 24-hour mode.

Updating time and calendar fields and configuring the alarm fields is performed by a parallel capture on the 8-bit data bus. An entry control is performed to avoid loading registers with incompatible BCD format data or with an incompatible date according to the current month/year/century.

Year 2000 Conformity

The Real Time Clock Macrocell complies fully with the Year 2000 Conformity Requirements as stated in the British Standards Institution Document; Ref. BSI-DISC PD2000-1: “Year 2000 conformity shall mean that neither performance nor functionality is affected by dates prior to, during and after the year 2000”.

It has been tested to be compliant with the four associated rules:

1. No value for current date will cause any interruption in operation.
2. Date-based functionality must behave consistently for dates prior to, during and after year 2000.
3. In all interfaces and data storage, the century in any date must be specified either explicitly or by unambiguous algorithms or inferencing rules.
4. Year 2000 must be recognized as a leap year.

The RTC represents the year as a four-digit number (..., 1998, 1999, 2000, 2001, etc.) so that the century is unambiguously identified, in accordance with Rule 3.

Scan Test Configuration

The fault coverage is maximum if all non-scan inputs can be controlled and all non-scan outputs can be observed. In order to achieve this, the ATPG vectors must be generated on the entire circuit (top level) which includes the RTC or all RTC I/Os must have a top level access and ATPG vectors must be applied to these pins.

Higher fault coverage may be achieved by applying manual vectors to the 32768 divider.

AVR®

Embedded RISC Microcontroller Core Peripheral

Real Time Clock (RTC)

Rev. 1302B–07/01

Figure 1. RTC Pin Configuration

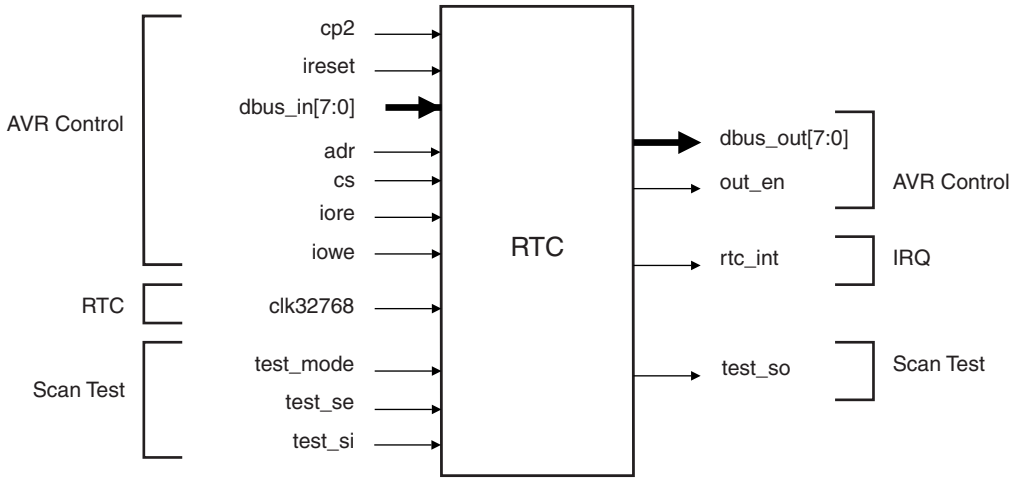


Table 1. Pin Description

Pin Name	Description	Direction	Comments
AVR Control			
cp2	CPU clock	Input	Any register in the RTC will update its contents only on the positive edge of cp2.
ireset	Synchronous reset	Input	When high, ireset will reset internal registers by reading the value on dbus_in which is forced to zero by the AVR Core.
dbus_in[7:0]	Data bus input	Input	
dbus_out[7:0]	Data bus output	Output	Valid only when out_en is high.
out_en	Output enable strobe	Output	When high, out_en indicates that the RTC requires control of the data bus.
cs	Chip Select	Input	When high, adr, iore and iowe are used to access internal RTC I/Os. When low, the RTC cannot be accessed in either read or write mode.
adr	I/O address input	Input	Connects to LSB of AVR adr[5:0] bus. Valid only when accompanied by a strobe on iore or iowe.
iore	I/O read strobe	Input	Used to read the contents of the I/O location addressed by adr. Active high.
iowe	I/O write strobe	Input	Used to update the contents of the I/O location addressed by adr. Active high.
RTC			
clk32768	Main clock for RTC	Input	F = 32.768 kHz (Crystal oscillator).
IRQ			
rtc_int	Interrupt	Output	Programmable from alarm and/or event. Active high.
Scan Test			
test_mode	Clock selection for test purposes	Input	All flip-flops are driven with the same clock (clk32768). Active high/low.
test_si	Test scan inputs	Input	Input of scan chain.
test_so	Test scan outputs	Output	Output of scan chain.
test_se	Test scan enable	Input	Scan shift/scan capture.

Functional Description

The RTC provides a full Binary-Coded Decimal (BCD) clock which includes century (19/20), year (with leap years), month, date, day, hours, minutes and seconds.

The valid year range is 1900 to 2099, a two-hundred year Gregorian calendar achieving full Y2K compliance.

The RTC operates in 24-hour mode.

Corrections for leap years are included (all years divisible by 4 being leap years, including year 2000). This is correct up to the year 2099.

RTC Chip Select (cs)

The RTC has the ability to be remapped inside the AVR I/O address range. A small amount of glue logic must be inserted to generate the cs signal. To access the internal I/O locations of the RTC, the following condition must be true:

cs = 1

Under this condition, iore, iowe and adr are used to access the internal RTC I/O for reading or writing. The cs input is generated from the decoding of the five AVR adr MSBs. To obtain the Base Address (BaseAdr) for RTC addressing, use the following logic:

cs = (adr[5:1] = = cs_adr[4:0])

Where the value of cs_adr is assigned by the designer; the binary value {cs_adr[4:0], 0} is the Base Address (BaseAdr) for RTC addressing.

The BaseAdr and corresponding restrictions for each value of cs_adr are shown in Table 2.

Table 2. cs_adr/BaseAdr

cs_adr	BaseAdr	Comment
0x00	0x00	Allowed
0x01	0x02	–
.	.	.
.	.	.
.	.	.
.	.	.
0x0F	0x1E	–
0x10	0x20	–
.	.	.
.	.	.
.	.	.
0x1b	0x36	–
0x1c	0x38	Not Allowed
.	.	.
.	.	.
.	.	.
0x1F	0x3E	Not Allowed

The 1-bit adr provides the offset which locates the RTC registers, as shown in Table 3..

Table 3. RTC Address/Data Registers

adr	RTC Register
0	RTC Internal Address Register
1	RTC Internal Data Register

Timing

The RTC is updated in real time at one second intervals in normal mode for the seconds counter, at 1 minute intervals for the minutes counter and so on.

Due to the asynchronous operation of the RTC with respect to the rest of the chip, to be certain that the values read in the RTC registers (century, year, month, date, day, hours, minutes, seconds) are valid and stable, it is necessary to read these registers twice. If the data is the same both times, then it is valid. Therefore, a minimum of two and a maximum of three accesses is required.

Alarm

The RTC has four programmable fields: date, hours, minutes and seconds. Each of these fields can be enabled or disabled to match the alarm condition.

- If all the fields are enabled, an alarm flag is generated (the corresponding flag is asserted and an interrupt generated if enabled) at a given date/hour/minute/second.
- If only the seconds field is enabled, then an alarm is generated every minute.
- Depending on the combination of fields enabled, a large number of possibilities are available to the user ranging from minutes to 365/366 days.

Error Checking

A verification of user interface data is performed when accessing the century, year, month, date, day, hours, minutes, seconds and alarms. A check is performed for illegal BCD entries such as illegal date of the month with regards to the year and century configured.

If one of the time fields is not correct, the data is not loaded into the register/counter and a flag is set in the validity register. This flag cannot be reset by the user. It is reset as soon as an acceptable value is programmed. This avoids any further side effects in the hardware. The same procedure is done for the alarm.

The following checks are performed:

1. Century (check if it is in range 19-20)
2. Year (BCD entry check)
3. Date (check range 01-31)
4. Month (check if it is in BCD range 01-12, check validity regarding “date”)
5. The order of the following steps can be random.
6. Day (check range 1-7)
7. Hour (BCD check, check range 00-23)
8. Minute (check BCD and range 00-59)
9. Second (check BCD and range 00-59)

Updating Time/Calendar

To update any of the time/calendar fields, the user must first stop the RTC by setting the corresponding field in the Control Register (RTC_CR). Bit UPDTIM must be set to update time fields (hour, minute, second) and bit UPDCAL must be set to update calendar fields (century, year, month, date, day).

Then the user must poll or wait for the interrupt (if enabled) of bit ACKUPD in the Status Register. Once the bit reads 1, the user can write to the appropriate register.

Once the update is finished, the user must reset (0) UPDTIM and/or UPDCAL in the control register.

When programming the calendar fields, the time fields remain enabled. This avoids a time slip in case the user stays in the calendar update phase for several tens of seconds or more.

Read/Write Access from the AVR

Only two registers can be directly accessed by the user:

- The Internal Address Register (BaseAdr+0) stores the offset of the targeted RTC register
- The Internal Data Register (BaseAdr+1) loads the data to the dedicated RTC register identified by the offset.

Timing Diagram

Figure 2. RTC Write Cycle

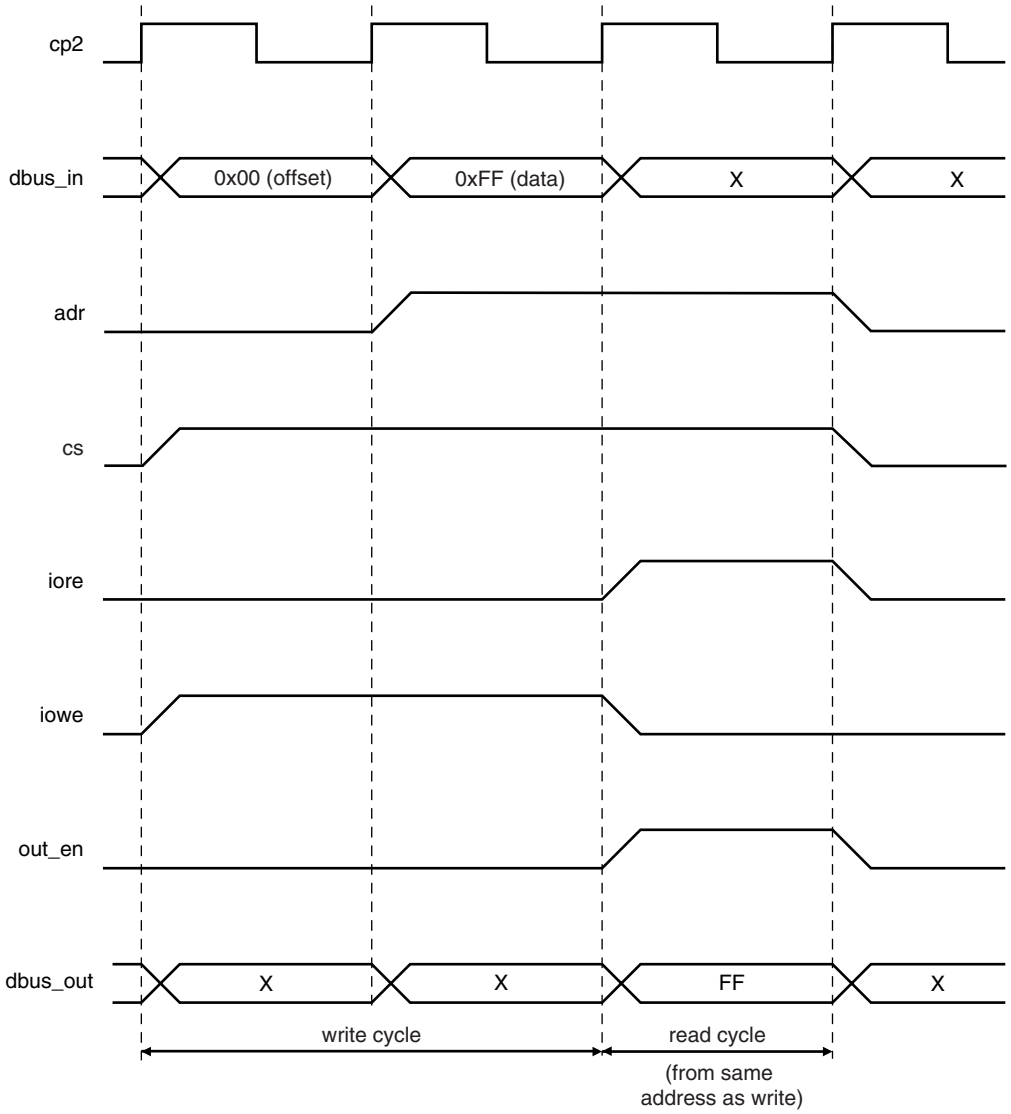
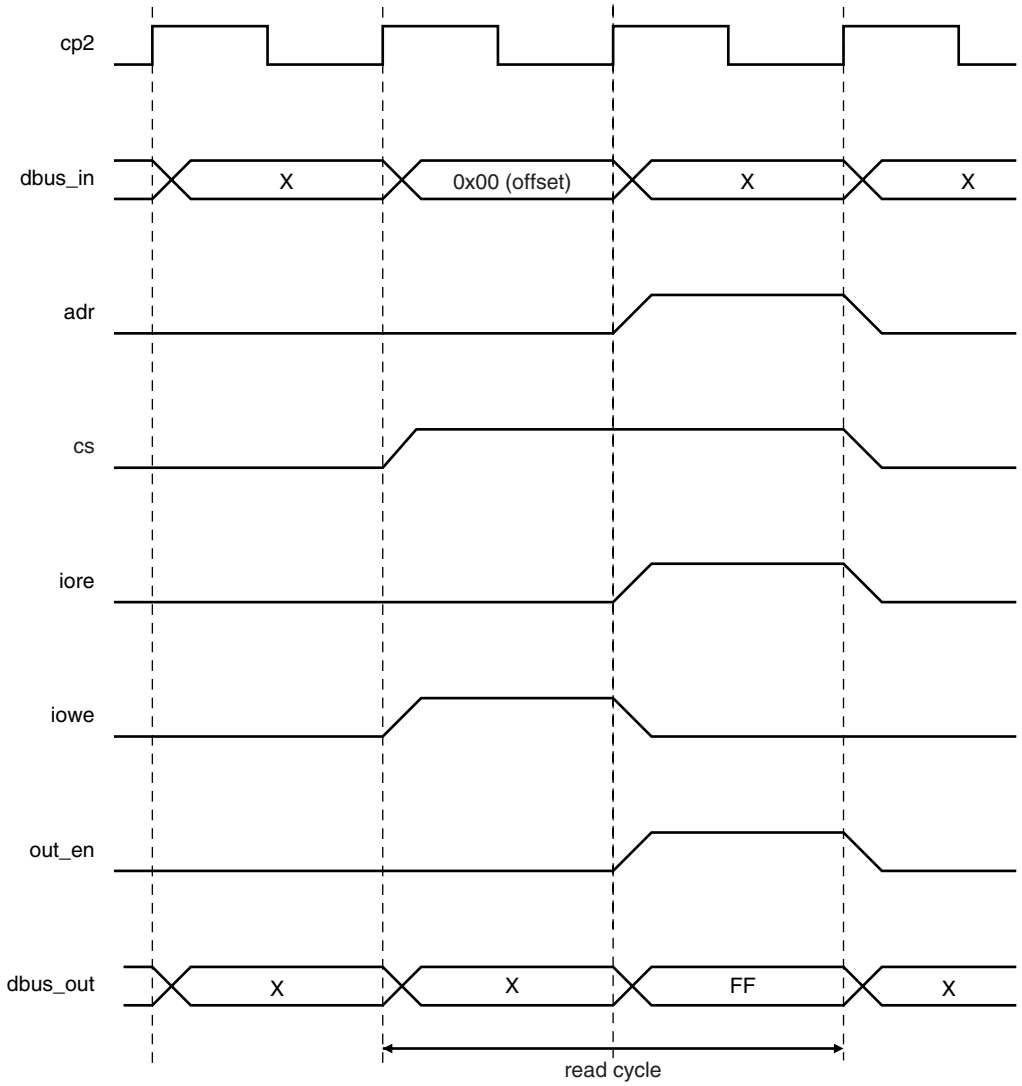


Figure 3. RTC Read Cycle



Reset

When high, the ireset signal initializes the RTC registers with the following values:

Time	00:00:00
Calendar	Thursday, 01 January 1998
Alarm	00:00:00 Date: 01 January
Alarm enable	All fields disabled
Interrupt	Disabled

RTC Software User Interface

Table 4. RTC Internal Memory Map

Offset	Register	Name	Access	Reset State
0x00	Control Register	RTC_CR	Read/Write	0x00
0x04	Seconds Register	RTC_SEC	Read/Write	0x00
0x05	Minutes Register	RTC_MIN	Read/Write	0x00
0x06	Hours Register	RTC_HOUR	Read/Write	0x00
0x08	Day Register	RTC_DAY	Read/Write	0x04
0x09	Date Register	RTC_DATE	Read/Write	0x01
0x0A	Month Register	RTC_MONTH	Read/Write	0x01
0x0B	Year Register	RTC_YEAR	Read/Write	0x98
0x0C	Century Register	RTC_CENTURY	Read/Write	0x19
0x10	Seconds Alarm Register	RTC_AL_SEC	Read/Write	0x00
0x11	Minutes Alarm Register	RTC_AL_MIN	Read/Write	0x00
0x12	Hours Alarm Register	RTC_AL_HOUR	Read/Write	0x00
0x14	Date Alarm Register	RTC_AL_DATE	Read/Write	0x01
0x13	Month Alarm Register	RTC_AL_MONTH	Read/Write	0x01
0x18	Status Register	RTC_SR	Read-only	0x00
0x1C	Status Clear Register	RTC_CLR_ST	Write-only	0x00
0x20	Interrupt Control Register	RTC_INT_CR	Read/Write	0x00
0x24	Interrupt Select Register	RTC_INT_SEL	Read/Write	0x00
0x28	Time Validity Register	RTC_TC_VALID	Read-only	0x00
0x29	Alarm Validity Register	RTC_ALR_VALID	Read-only	0x00

Note: All time and date registers are binary coded decimal (BCD).

RTC Control Register

Name: RTC_CR

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	---	---	---	---	UPDCAL	UPDTIM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **UPDTIM: Update Request Time Register**

0 = No effect.

1 = Stops the RTC Time counting.

Time counting consists of second, minute and hour counters. Time counters can then be programmed.

It also stops any processing of the calendar to avoid any calendar counter change while the seconds/minutes/hours are being changed.

- **UPDCAL: Update Request Calendar Register**

0 = No effect.

1 = Stops the RTC calendar counting.

Calendar counting consists of day, date, month, year and century counters. Calendar counters can be programmed once this bit is set.

The time counters (hours/minutes/seconds) are not stopped to avoid any slip during the update of the calendar.

RTC Seconds Register

Name: RTC_SEC

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	SEC						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **SEC: Current Second**

The range that can be set is 0-59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

All non-significant bits read zero.

RTC Minutes Register

Name: RTC_MIN

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	MIN						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **MIN: Current Minute**

The range that can be set is 0-59 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

RTC Hours Register

Name: RTC_HOUR

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	HOUR					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **HOUR: Current Hour**

The range that can be set is 0-23 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

All non-significant bits read zero.

RTC Day Register

Name: RTC_DAY

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	---	---	---	DAY		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **DAY: Current Day**

The range that can be set is 1-7 (BCD).

The significance of the number (which day is which number) is user defined as it has no effect on the date counter.

During reset, this field is set to 4, associated with January 01 1998 for the date. This means that 1 is Monday.

RTC Date Register

Name: RTC_DATE

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	DATE					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **DATE: Current Date**

The range that can be set is 01-31 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

All non-significant bits read zero.

RTC Month Register

Name: RTC_MONTH

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	---	MONTH				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **MONTH: Current Month**

The range that can be set is 01-12 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

All non-significant bits read zero.

RTC Year Register

NAME: RTC_YEAR

ACCESS: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	YEAR							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **YEAR: Current Year**

The range that can be set is 00-99 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

RTC Century Register

NAME: RTC_CENTURY

ACCESS: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	CENTURY					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **CENTURY: Current Century**

The range that can be set is 19-20 (BCD).

The lowest four bits encode the units. The higher bits encode the tens.

RTC Seconds Alarm Register

Name: RTC_AL_SEC

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	SECEN	SEC						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **SEC: Second Alarm**

This field register is an alarm field corresponding to the BCD-coded second counter.
The alarm triggers when the contents of the second alarm field matches the real time in seconds.

- **SECEN: Second Alarm Enable**

0 = The second-matching alarm is disabled.

1 = The second-matching alarm is enabled.

RTC Minutes Alarm Register

Name: RTC_AL_MIN

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	MINEN	MIN						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **MIN: Minute Alarm**

This field register is an alarm field corresponding to the BCD-coded minute counter.
The alarm triggers when the contents of the minute alarm field matches the real time in minutes.

- **MINEN: Minute Alarm Enable**

0 = The minute-matching alarm is disabled.

1 = The minute-matching alarm is enabled.

RTC Hours Alarm Register

Name: RTC_AL_HOUR

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	HOUREN	---	HOUR					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **HOUR: Hour Alarm**

This field register is an alarm field corresponding to the BCD-coded hour counter.
The alarm triggers when the contents of the hour alarm field matches the real time in hours.

- **HOUREN: Hour Alarm Enable**

0 = The hour-matching alarm is disabled.

1 = The hour-matching alarm is enabled.

RTC Date Alarm Register

Name: RTC_AL_DATE

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	DATEN	---	DATE					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **DATE: Date Alarm**

This field register is an alarm field corresponding to the BCD-coded date counter.
The alarm triggers when the contents of the date alarm field matches the real time by date.

- **DATEN: Date Alarm Enable**

0 = The date-matching alarm is disabled.

1 = The date-matching alarm is enabled.

RTC Month Alarm Register

Name: RTC_AL_MONTH

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	MTHEN	---	MONTH					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **MONTH: Month Alarm**

This field register is an alarm field corresponding to the BCD-coded month section counter.
The alarm triggers when the contents of the month alarm field matches the real time in months.

- **MTHEN: Month Alarm Enable**

0 = The month-matching alarm is disabled.

1 = The month-matching alarm is enabled.

RTC Status Register

Name: RTC_SR

Access: Read-only

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	---	CALEV	TIMEV	SEC	ALARM	ACKUPD
Read/Write	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

- **ACKUPD: Acknowledge for Update flag**

0 = Time and Calendar registers cannot be updated.

1 = Time and Calendar registers can be updated.

If enabled on this flag, the interrupt is set.

- **ALARM: Alarm flag**

0 = No Alarm matching condition occurred.

1 = An Alarm matching condition has occurred.

If enabled on this flag, the interrupt is set.

- **SEC: Second Event flag**

0 = No second event has occurred since the last clear.

1 = At least one second event has occurred since the last clear.

If enabled on this flag, the interrupt is set.

- **TIMEV: Time Event**

0 = No time event has occurred since the last clear

1 = At least one time event has occurred since the last clear.

The time event is selected in the SELTIM field in RTC_INT_SEL (Interupt Select Register) and can be any one of the following events: minute change, hour change, noon, midnight (day change).

- **CALEV: Calendar Event**

0 = No calendar event has occurred since the last clear

1 = At least one calendar event has occurred since the last clear.

RTC Status Clear Register

Name: RTC_CLR_SR

Access: Write-Only

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	---	CALEVCLR	TIMEVCLR	SECCLR	ALRCLR	ACKCLR
Read/Write	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

- **ACKCLR: ACKUPD Clear**

0 = No effect.

- **1 = Clears ACKUPD flag in the Status Register.**

It also clears the interrupt if the interrupt is only generated with this flag.

- **ALRCLR: Alarm Clear**

0 = No effect.

1 = Clears ALARM flag in the Status Register.

It also clears the interrupt if the interrupt is only generated with this flag.

- **SECCLR: Second Clear**

0 = No effect.

1 = Clears Second flag in the Status Register.

It also clears the interrupt if the interrupt is only generated with this flag.

- **TIMEVCLR: Time Event Alarm Clear**

0 = No effect.

1 = Clears TIMEV flag in the Status Register.

It also clears the interrupt if the interrupt is only generated with this flag.

- **CALEVCLR: Second Clear**

0 = No effect.

1 = Clears CALEV flag in the Status Register.

It also clears the interrupt if the interrupt is generated with this flag only.

RTC Interrupt Control Register

Name: RTC_INT_CR

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	---	CALEV_EN	TIMEV_EN	SEC_EN	ALR_EN	ACK_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **ACK_EN: Acknowledge Update Interrupt Enabled**

0 = Disables the generation of the Interrupt when the ACKWR flag of Status Register is active.

1 = Enables the generation of the Interrupt when the ALARM flag of Status Register is active.

- **ALR_EN: Alarm Interrupt Enabled**

0 = Disables the generation of the Interrupt when the ALARM flag of the Status Register is active.

1 = Enables the generation of the Interrupt when the ALARM flag of the Status Register is active.

- **SEC_EN: Second Interrupt Enabled**

0 = Disables the generation of the Interrupt when the SEC flag of the Status Register is active.

1 = Enables the generation of the Interrupt when the SEC flag of the Status Register is active.

- **TIMEV_EN: Time Event Interrupt Enabled**

0 = Disables the generation of the Interrupt when the TIMEV flag of the Status Register is active.

1 = Enables the generation of the Interrupt when the TIMEV flag of the Status Register is active.

- **CALEV_EN: Calendar Event Interrupt Enabled**

0 = Disables the generation of the Interrupt when the CALEV flag of the Status Register is active.

1 = Enables the generation of the Interrupt when the CALEV flag of the Status Register is active.

Interrupt Select Register

Name: RTC_INT_SEL

Access: Read/Write

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	SELCAL		---	---	SELTIM	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **SELTIM: Select Time Interrupt**

00 = An interrupt will be set every minute (if enabled)

01 = An interrupt will be set every hour (if enabled)

10 = An interrupt will be set every day at midnight (if enabled)

11 = An interrupt will be set every day at noon (if enabled)

- **SELCAL: Select Calendar Interrupt**

00 = An interrupt will be set every week (on Sunday at 00:00:00)

01 = An interrupt will be set every month (on 1st of the month at 00:00:00)

10 = An interrupt will be set every year (on January 1st at 00:00:00)

11 = Reserved

RTC Time/Calendar Valid Register

Name: RTC_TC_VALID

Access: Read-only

Bit	7	6	5	4	3	2	1	0
BaseAdr	NVCENT	NVYEAR	NVMONTH	NVDATE	NVDAY	NVHOUR	NVMIN	NVSEC
Read/Write	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

- **NVSEC: Non-Valid Second**

0 = No invalid data was detected when programming the RTC_SEC register.

1 = Invalid data was detected when programming the RTC_SEC registers.

- **NVMIN: Non-Valid Minute**

0 = No invalid data was detected when programming the RTC_MIN register.

1 = Invalid data was detected when programming the RTC_MIN registers.

- **NVHOUR: Non-Valid Hour**

0 = No invalid data was detected when programming the RTC_HOUR Register.

1 = Invalid data was detected when programming the RTC_HOUR Registers.

- **NVDAY: Non-Valid Day**

0 = No invalid data was detected when programming the RTC_DAY Register.

1 = Invalid data was detected when programming the RTC_DAY Register.

- **NVDATE: Non-Valid Date**

0 = No invalid data was detected when programming the RTC_DATE Register.

1 = Invalid data was detected when programming the RTC_DATE Register.

The Century, Year, Month field must be programmed before programming the date because the NVDATE could be set incorrectly. For example, if RTC_CENTURY = 19, RTC_YEAR = 98, RTC_MONTH = 02 (FEB) and the user attempts to enter 29 into RTC_DATE.

- **NVMONTH: Non-Valid Month**

0 = No invalid data was detected when programming the RTC_MONTH Register.

1 = Invalid data was detected when programming the RTC_MONTH Register.

- **NVYEAR: Non-Valid Year**

0 = No invalid data was detected when programming the RTC_YEAR Register.

1 = Invalid data was detected when programming the RTC_YEAR Register.

- **NVCENT: Non-Valid Century**

0 = No invalid data was detected when programming the RTC_CENT Register.

1 = Invalid data was detected when programming the RTC_CENT Register.

These flags are reset only when the data to be programmed is correct.

RTC Time/Calendar Alarm Valid Register

Name: RTC_ALR_VALID

Access: Read-only

Bit	7	6	5	4	3	2	1	0
BaseAdr	---	---	---	NVMONTH	NVDATE	NVHOUR	NVMIN	NVSEC
Read/Write	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

- **NVSEC: Non-Valid Second**

0 = No invalid data was detected when programming the RTC_AL_SEC register.

1 = Invalid data was detected when programming the RTC_AL_SEC registers.

- **NVMIN: Non-Valid Minute**

0 = No invalid data was detected when programming the RTC_AL_MIN register.

1 = Invalid data was detected when programming the RTC_AL_MIN registers.

- **NVHOUR: Non-Valid Hour**

0 = No invalid data was detected when programming the RTC_AL_HOUR Register.

1 = Invalid data was detected when programming the RTC_AL_HOUR Registers.

- **NVDATE: Non-Valid Date**

0 = No invalid data was detected when programming the RTC_AL_DATE Register.

1 = Invalid data was detected when programming the RTC_AL_DATE Register.

- **NVMONTH: Non-Valid Month**

0 = No invalid data was detected when programming the RTC_AL_MONTH Register.

1 = Invalid data was detected when programming the RTC_AL_MONTH Register.

These flags are reset only when the data to be programmed is correct.

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