



### FEATURES

Sixth-order filters with selectable cutoff frequencies

36 MHz, 18 MHz, 9 MHz

Many video standards supported

GBR/YPbPr/YUV/SD/YC/CV

Ideal for resolutions up to 1080i

-1 dB bandwidth of 30 MHz for HD

2:1 multiplexers on all inputs

Selectable gain:  $\times 2$  or  $\times 4$

Output dc adjust

Excellent video specifications

NTSC differential gain: 0.11%

NTSC differential phase: 0.25°

Low input bias current: 6.6  $\mu$ A

Wide supply range: +4.5 V to  $\pm 5$  V

Rail-to-rail output

Disable feature

### APPLICATIONS

Set-top boxes

DVD players and recorders

HDTV

### GENERAL DESCRIPTION

The ADA4410-6 is a comprehensive integrated filtering solution that is carefully designed to give designers the flexibility to easily filter and drive many types of video signals, including high definition video. In the GBR/component channels, the cutoff frequencies of the sixth-order filters can be selected by two logic pins to obtain four filter combinations that are tuned for GBR, high definition, and standard definition video. Cutoff frequencies range from 36 MHz to 9 MHz.

The ADA4410-6 also provides filtering for the legacy standard S-video and composite video signals. With a differential gain of 0.11% and a differential phase of 0.25°, the ADA4410-6 is an excellent choice for any composite video (CV) application.

The ADA441-6 offers gain and output offset voltage adjustments. The gain of the part can be  $\times 2$  or  $\times 4$ , and the output offset voltage is continuously adjustable up to  $\pm 2$  V by applying a differential voltage to an independent offset control input.

The ADA4410-6 offers 2:1 multiplexers on its inputs that can be used in applications where multiple sources of video exist.

#### Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

### FUNCTIONAL BLOCK DIAGRAM

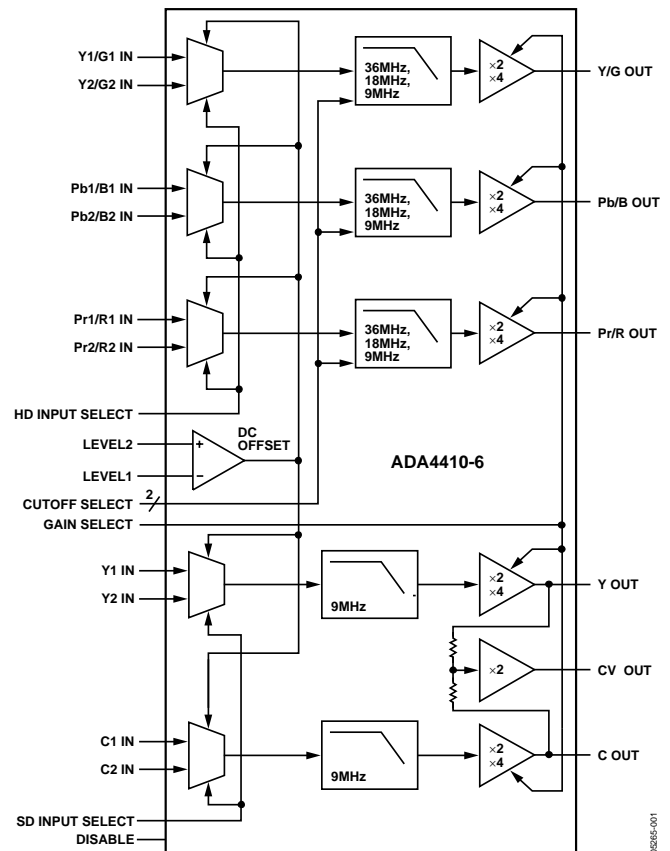


Figure 1.

The ADA4410-6 can operate on a single +5 V supply as well as  $\pm 5$  V supplies. Single-supply operation is ideal for applications where power consumption is critical. A disable feature allows for further power conservation.

Dual-supply operation is for applications where the negative-going excursions of the signal must swing at or below ground while maintaining excellent video performance. The output buffers have the ability to drive two 75  $\Omega$  terminated loads that are either dc- or ac-coupled.

The ADA4410-6 is available in a 32-lead LFCSP and operates in the commercial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

05055-001

**TABLE OF CONTENTS**

Specifications.....	3	Gain Select.....	13
Absolute Maximum Ratings.....	7	Disable .....	13
Thermal Resistance .....	7	Cutoff Frequency Selection.....	13
ESD Caution.....	7	Output DC Offset Control.....	13
Pin Configuration and Function Descriptions.....	8	Input and Output Coupling.....	14
Typical Performance Characteristics .....	9	Printed Circuit Board Layout .....	14
Theory of Operation .....	12	Video Encoder Reconstruction Filter.....	15
Applications.....	13	Outline Dimensions .....	16
Overview.....	13	Ordering Guide .....	16
Multiplexer Select Inputs.....	13		

**REVISION HISTORY**

**1/05—Revision 0: Initial Version**

## SPECIFICATIONS

$V_S = 5\text{ V}$ , @  $T_A = 25^\circ\text{C}$ ,  $V_O = 1.4\text{ V p-p}$ ,  $G = \times 2$ ,  $R_L = 150\ \Omega$ , unless otherwise noted.

**Table 1.**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>OVERALL PERFORMANCE</b>					
Offset Error	Input referred, all channels except CV		10	34	mV
	Input referred, CV		12	44	mV
Offset Adjust Range (see the Output DC Offset Control section)	Input Referred		$\pm 500$		mV
Input Voltage Range, All Inputs		$V_{S-} - 0.1$		$V_{S+} - 2.0$	V
Output Voltage Range, All Outputs	$I_O = 15\text{ mA}$ , positive swing	$V_{S+} - 0.5$	$V_{S+} - 0.25$		V
	$I_O = 15\text{ mA}$ , negative swing	$V_{S-} + 0.4$	$V_{S-} + 0.12$		V
Linear Output Current per Channel			30		mA
Integrated Voltage Noise, Referred to Input	All channels except CV		500		$\mu\text{V}_{\text{rms}}$
Filter Input Bias Current	All channels		6.6	9.5	$\mu\text{A}$
Total Harmonic Distortion at 1 MHz	$f_C = 36\text{ MHz}$ , $f_C = 18\text{ MHz}/f_C = 9\text{ MHz}$		0.01/0.07		%
<b>GBR/YPbPr CHANNEL DYNAMIC PERFORMANCE</b>					
-1 dB Bandwidth	Cutoff frequency select = 36 MHz		30		MHz
	Cutoff frequency select = 18 MHz		15		MHz
	Cutoff frequency select = 9 MHz		8		MHz
-3 dB Bandwidth	Cutoff frequency select = 36 MHz	34	36		MHz
	Cutoff frequency select = 18 MHz	16	18		MHz
	Cutoff frequency select = 9 MHz	8	9		MHz
Out-of-Band Rejection	$f = 75\text{ MHz}$	-27	-32		dB
Crosstalk	$f = 5\text{ MHz}$ , $f_C = 36\text{ MHz}$		-68		dB
Input MUX Isolation	$f = 1\text{ MHz}$ , $R_{\text{SOURCE}} = 300\ \Omega$		86		dB
Propagation Delay	$f = 16\text{ MHz}$ , $f_C = 36\text{ MHz}$		20		ns
Group Delay Variation	Cutoff frequency select = 36 MHz		8		ns
	Cutoff frequency select = 18 MHz		15		ns
	Cutoff frequency select = 9 MHz		26		ns
<b>Y/C SD CHANNEL DYNAMIC PERFORMANCE</b>					
-1 dB Bandwidth			8		MHz
-3 dB Bandwidth		8	9		MHz
Out-of-Band Rejection	$f = 27\text{ MHz}$		-54		dB
Propagation Delay	$f = 1\text{ MHz}$		70		ns
Group Delay Variation			26		ns
Crosstalk	$f = 1\text{ MHz}$		-72		dB
Input MUX Isolation	$f = 1\text{ MHz}$ , $R_{\text{SOURCE}} = 75\ \Omega$		77		dB
<b>Y/C, CV OUTPUT VIDEO PERFORMANCE</b>					
Differential Gain	NTSC		0.09		%
Differential Phase	NTSC		0.37		Degrees
<b>CONTROL INPUT PERFORMANCE</b>					
Input Logic 0 Voltage	All inputs except DISABLE			0.8	V
Input Logic 1 Voltage	All inputs except DISABLE	2.0			V
Input Bias Current	All inputs except DISABLE		7	9.5	$\mu\text{A}$
<b>DISABLE PERFORMANCE</b>					
DISABLE Assert Voltage			$V_{S+} - 0.5$		V
DISABLE Assert Time			100		ns
DISABLE De-Assert Time			130		ns
DISABLE Input Bias Current			12	20	$\mu\text{A}$
Input-to-Output Isolation—Disabled			100		dB

# ADA4410-6

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		12	V
Quiescent Current			81	92	mA
Quiescent Current—Disabled			15	150	μA
PSRR, Positive Supply	All channels except CV	60	72		dB
	CV channel	54	66		dB
PSRR, Negative Supply	All channels except CV	55	62		dB
	CV channel	49	56		dB

$V_S = \pm 5\text{ V}$ , @  $T_A = 25^\circ\text{C}$ ,  $V_O = 1.4\text{ V p-p}$ ,  $G = \times 2$ ,  $R_L = 150\ \Omega$ , unless otherwise noted.

**Table 2.**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>OVERALL PERFORMANCE</b>					
Offset Error	Input referred, all channels except CV		14	35	mV
	Input referred, CV		15	48	mV
Offset Adjust Range (see the Output DC Offset Control section)	Input Referred		$\pm 500$		mV
Input Voltage Range, All Inputs		$V_{S-} - 0.1$		$V_{S+} - 2.0$	V
Output Voltage Range, All Outputs	$I_O = 30\text{ mA}$ , positive swing	$V_{S+} - 0.6$	$V_{S+} - 0.3$		V
	$I_O = 30\text{ mA}$ , negative swing	$V_{S-} + 0.6$	$V_{S-} + 0.3$		V
Linear Output Current per Channel			30		mA
Integrated Voltage Noise, Referred to Input	All channels except CV		500		$\mu\text{V}_{\text{rms}}$
Filter Input Bias Current	All channels		6.3	9.5	$\mu\text{A}$
Total Harmonic Distortion at 1 MHz	$f_C = 36\text{ MHz}$ , $f_C = 18\text{ MHz}/f_C = 9\text{ MHz}$		0.01/0.07		%
<b>GBR/YPbPr CHANNEL DYNAMIC PERFORMANCE</b>					
-1 dB Bandwidth	Cutoff frequency select = 36 MHz		28		MHz
	Cutoff frequency select = 18 MHz		15		MHz
	Cutoff frequency select = 9 MHz		8		MHz
-3 dB Bandwidth	Cutoff frequency select = 36 MHz	33.5	35.5		MHz
	Cutoff frequency select = 18 MHz	16	18		MHz
	Cutoff frequency select = 9 MHz	8	9.5		MHz
Out-of-Band Rejection	$f = 75\text{ MHz}$	-27	-32		dB
Crosstalk	$f = 5\text{ MHz}$ , $f_C = 36\text{ MHz}$		-68		dB
Input MUX Isolation	$f = 1\text{ MHz}$ , $R_{\text{SOURCE}} = 300\ \Omega$		86		dB
Propagation Delay	$f = 5\text{ MHz}$ , $f_C = 36\text{ MHz}$		21		ns
Group Delay Variation	Cutoff frequency select = 36 MHz		6		ns
	Cutoff frequency select = 18 MHz		13		ns
	Cutoff frequency select = 9 MHz		23		ns
<b>Y/C SD CHANNEL DYNAMIC PERFORMANCE</b>					
-1 dB Bandwidth			8		MHz
-3 dB Bandwidth		8	9		MHz
Out-of-Band Rejection	$f = 27\text{ MHz}$		-51		dB
Propagation Delay	$f = 1\text{ MHz}$		67		ns
Group Delay Variation			22.5		ns
Crosstalk	$f = 1\text{ MHz}$		-72		dB
Input MUX Isolation	$f = 1\text{ MHz}$ , $R_{\text{SOURCE}} = 75\ \Omega$		77		dB
<b>Y/C, CV OUTPUT VIDEO PERFORMANCE</b>					
Differential Gain	NTSC		0.11		%
Differential Phase	NTSC		0.25		Degrees
<b>CONTROL INPUT PERFORMANCE</b>					
Input Logic 0 Voltage	All inputs except DISABLE			0.8	V
Input Logic 1 Voltage	All inputs except DISABLE	2.0			V
Input Bias Current	All inputs except DISABLE		7	9.5	$\mu\text{A}$
<b>DISABLE PERFORMANCE</b>					
DISABLE Assert Voltage			$V_{S+} - 0.5$		V
DISABLE Assert Time			75		ns
DISABLE De-Assert Time			125		ns
DISABLE Input Bias Current			35	45	$\mu\text{A}$
Input-to-Output Isolation—Disabled			100		dB

# ADA4410-6

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		4.5		12	V
Quiescent Current			85	95	mA
Quiescent Current—Disabled			15	150	μA
PSRR, Positive Supply	All channels except CV	60	72		dB
	CV channel	54	66		dB
PSRR, Negative Supply	All channels except CV	55	62		dB
	CV channel	49	56		dB

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12 V
Power Dissipation	See Figure 2
Storage Temperature	-65°C to +125°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad on the PCB surface that is thermally connected to a copper plane.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5 mm × 5 mm, 32-Lead LFCSP	43	5.1	°C/W

### Maximum Power Dissipation

The maximum safe power dissipation in the ADA4410-6 package is limited by the associated rise in junction temperature ( $T_J$ ) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4410-6. Exceeding a junction temperature of 150°C for an extended period of time can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package ( $P_D$ ) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins ( $V_S$ ) times the quiescent current ( $I_S$ ). The power dissipated due to load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipations due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing  $\theta_{JA}$ . Also, more metal directly in contact with the package leads from metal traces, through-holes, ground, and power planes reduces the  $\theta_{JA}$ . The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane in order to achieve the specified  $\theta_{JA}$ .

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 32-lead LFCSP (43°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane.  $\theta_{JA}$  values are approximations.

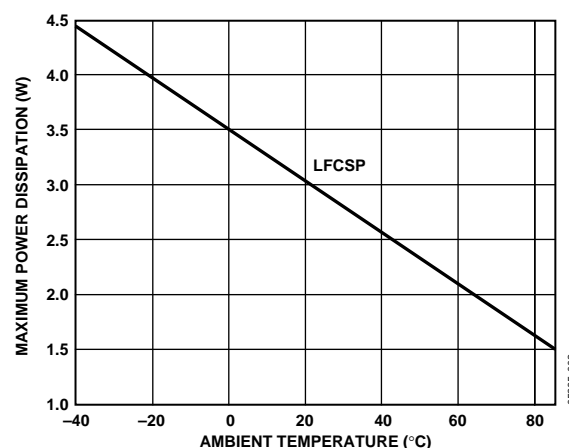


Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

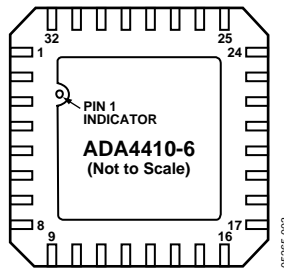


Figure 3. 32-Lead LFCSP, Top View

Table 5. Pin Function Descriptions

Pin No.	Name	Description
1	Pb1/B1_HD	Channel 1 Pb/B High Definition Input
2	GND	Signal Ground Reference
3	Pr1/R1_HD	Channel 1 Pr/R High Definition Input
4	F_SEL_A	Filter Cutoff Select Input A
5	F_SEL_B	Filter Cutoff Select Input B
6	Y2/G2_HD	Channel 2 Y/G High Definition Input
7	GND	Signal Ground Reference
8	Pb2/B2_HD	Channel 2 Pb/B High Definition Input
9	GND	Signal Ground Reference
10	Pr2/R2_HD	Channel 2 Pr/R High Definition Input
11	MUX_SD	Standard Definition Input MUX Select Line
12	Y1_SD	Channel 1 Y Standard Definition Input
13	Y2_SD	Channel 2 Y Standard Definition Input
14	C1_SD	Channel 1 C Standard Definition Input
15	C2_SD	Channel 2 C Standard Definition Input
16	VCC	Positive Power Supply
17	VEE	Negative Power Supply
18	CV_OUT	Composite Video Output
19	C_SD_OUT	C Standard Definition Output
20	Y_SD_OUT	Y Standard Definition Output
21	G_SEL	Gain Select
22	Pr/R_HD_OUT	Pr/R High Definition Output
23	Pb/B_HD_OUT	Pb/B High Definition Output
24	Y/G_HD_OUT	Y/G High Definition Output
25	VEE	Negative Power Supply
26	VCC	Positive Power Supply
27	DISABLE	Disable/Power Down/Logic Reference
28	LEVEL2	DC Level Adjust Pin 2
29	LEVEL1	DC Level Adjust Pin 1
30	MUX_HD	High Definition Input MUX Select Line
31	Y1/G1_HD	Channel 1 Y/G High Definition Input
32	GND	Signal Ground Reference



# TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted,  $G = \times 2$ ,  $R_L = 150 \Omega$ ,  $V_O = 1.4 \text{ V p-p}$ ,  $V_S = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

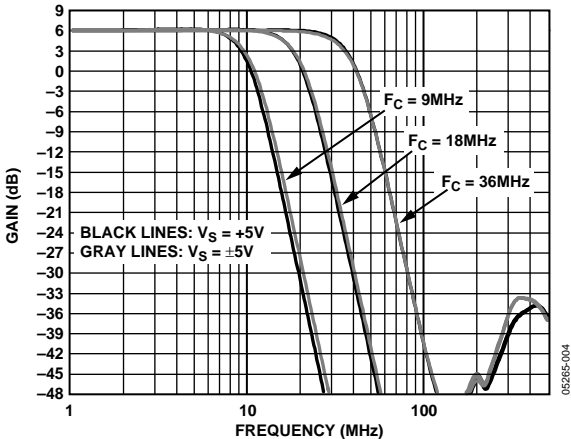


Figure 4. Frequency Response vs. Power Supply and Cutoff Frequency ( $G = \times 2$ )

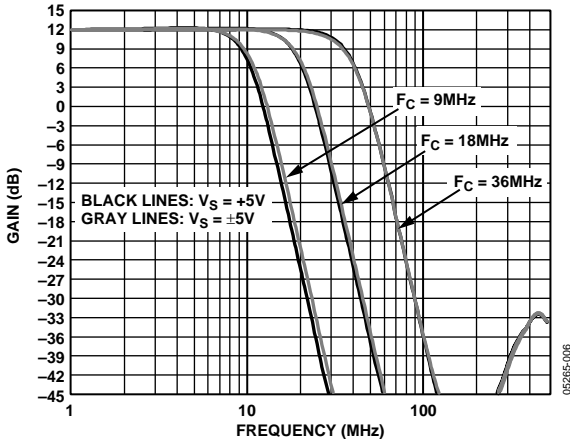


Figure 7. Frequency Response vs. Power Supply and Cutoff Frequency ( $G = \times 4$ )

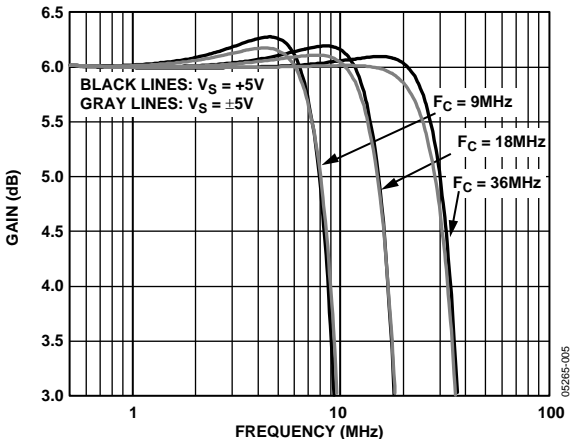


Figure 5. Frequency Response Flatness vs. Cutoff Frequency ( $G = \times 2$ )

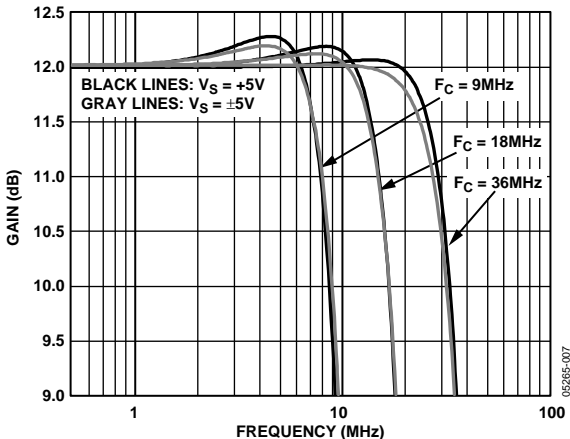


Figure 8. Frequency Response Flatness vs. Cutoff Frequency ( $G = \times 4$ )

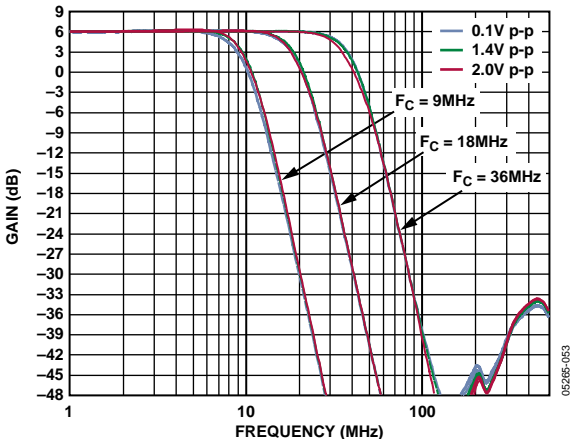


Figure 6. Frequency Response vs. Cutoff Frequency and Output Amplitude

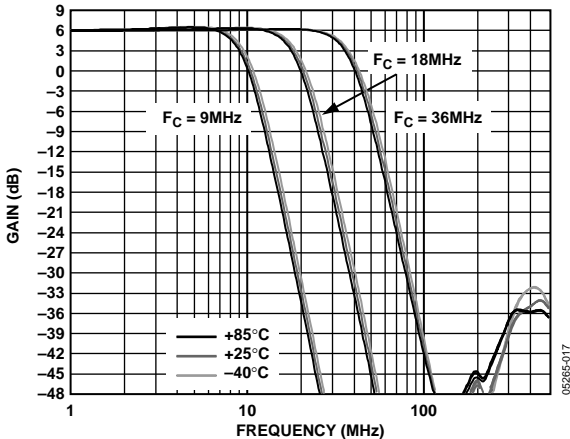


Figure 9. Frequency Response vs. Temperature and Cutoff Frequency

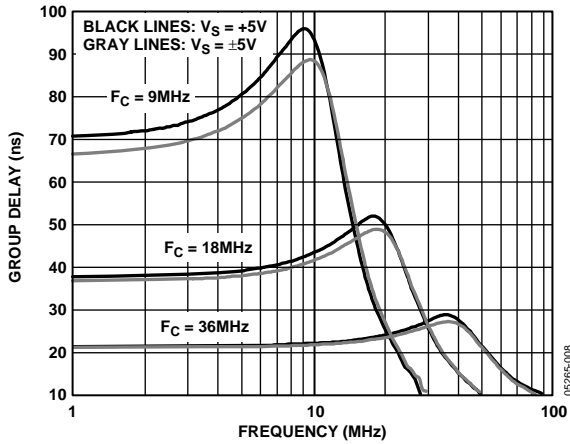


Figure 10. Group Delay vs. Frequency, Power Supply, and Cutoff Frequency

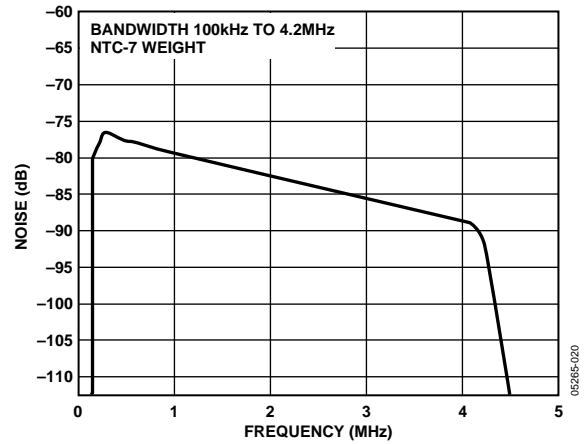


Figure 13. CV Noise Spectrum

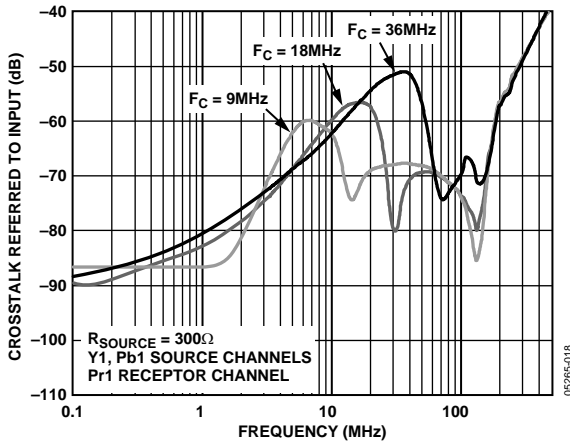


Figure 11. HD Channel Crosstalk vs. Frequency and Cutoff Frequency

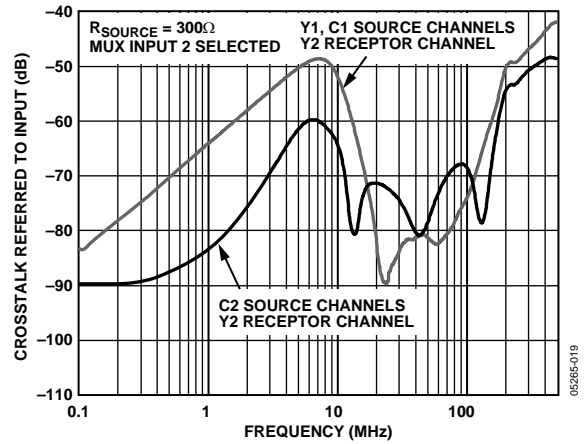


Figure 14. SD Channel Crosstalk vs. Frequency

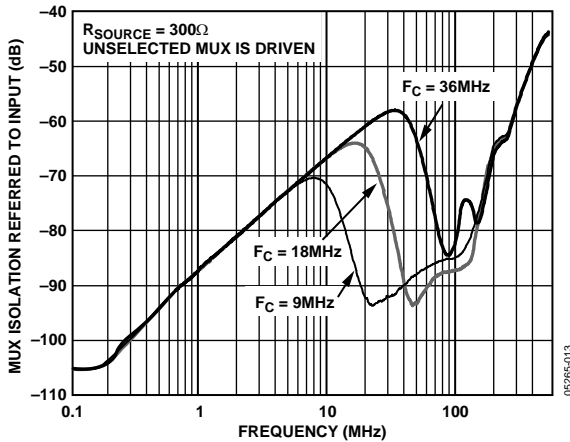


Figure 12. HD MUX Isolation vs. Frequency and Cutoff Frequency

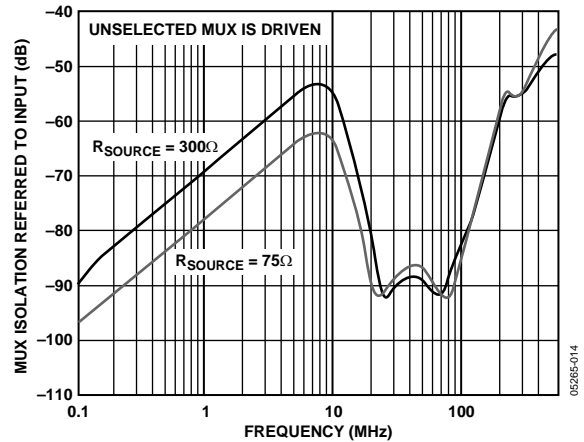


Figure 15. SD MUX Isolation vs. Frequency and Source Resistance

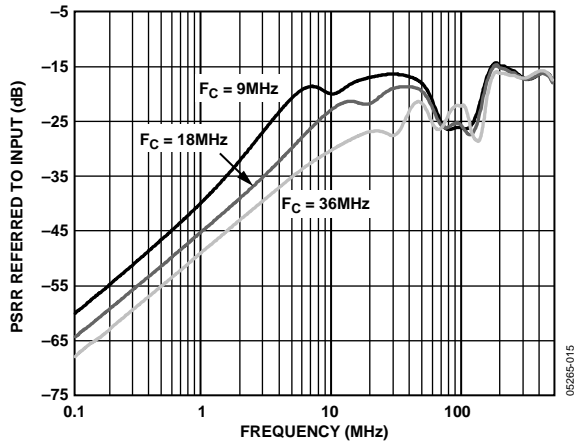


Figure 16. Positive Supply PSRR vs. Frequency and Cutoff Frequency

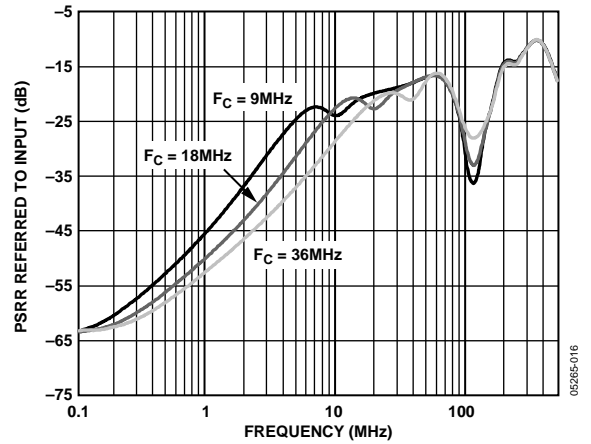


Figure 19. Negative Supply PSRR vs. Frequency and Cutoff Frequency

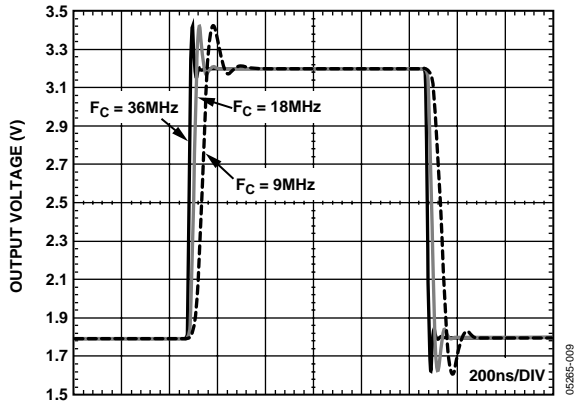


Figure 17. Transient Response vs. Cutoff Frequency ( $G = \times 2$ )

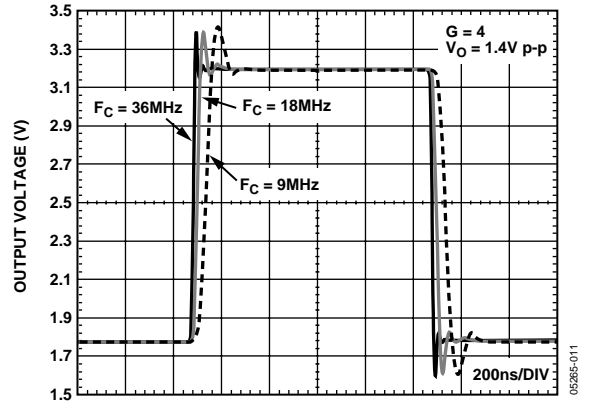


Figure 20. Transient Response vs. Cutoff Frequency ( $G = \times 4$ )

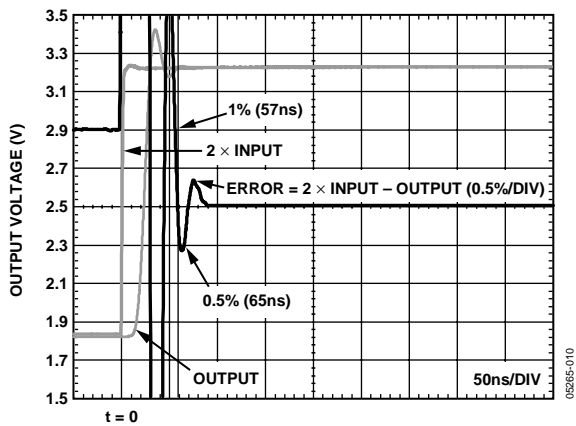


Figure 18. Settling Time

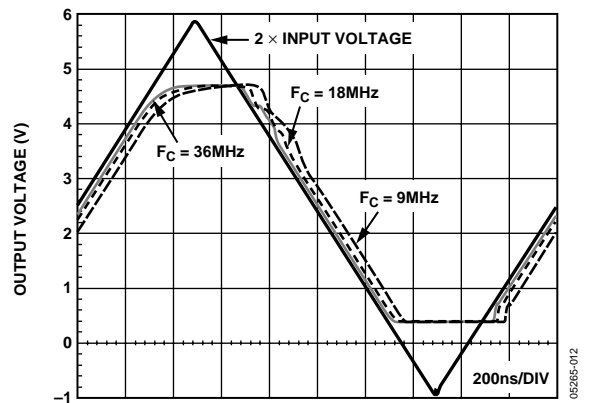


Figure 21. Overdrive Recovery vs. Cutoff Frequency

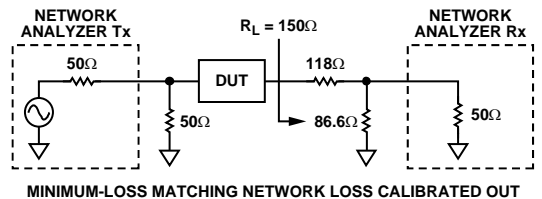


Figure 22. Basic Test Circuit for Swept Frequency Measurements

## THEORY OF OPERATION

The ADA4410-6 is an integrated video filtering and driving solution that offers variable bandwidth to meet the needs of several different video formats. There are a total of five filter sections, three for component video and two for Y/C and composite video. The component video filters have switchable bandwidths for standard definition interlaced, progressive, and high definition systems. The Y/C channels have fixed 9 MHz 3 dB cutoff frequencies and include a summing circuit that feeds an additional buffer for a composite video output. Each filter section has a sixth-order Butterworth response that includes group delay optimization. The group delay variation from 100 kHz to 36 MHz in the 36 MHz section is 8 ns, which produces a fast settling pulse response.

The ADA4410-6 is designed to operate in many different video environments. The supply range is 5 V to 12 V, single supply or dual supply, and requires a relatively low quiescent current of 15 mA per channel. In single-supply applications, the PSRR is greater than 70 dB, providing excellent rejection in systems with supplies that are noisy or underregulated. In applications where power consumption is critical, the part can be powered down to draw less than 10  $\mu$ A by pulling the DISABLE pin to the most positive rail. The ADA4410-6 is also well-suited for high encoding frequency applications because it maintains a stop-band attenuation of 50 dB beyond 200 MHz.

The ADA4410-6 is intended to take dc-coupled inputs from an encoder or other ground referenced video signals. The ADA4410-6 input is high impedance. No minimum or maximum input termination is required, although, input terminations above 1 k $\Omega$  can degrade crosstalk performance at high frequencies. No clamping is provided internally. For applications where dc restoration is required, dual supplies work best. Using a termination resistance of less than a few hundred ohms to ground on the inputs and suitably adjusting the level shift circuitry provides precise placement of the output voltage.

For single-supply applications ( $V_{S-} = \text{GND}$ ), the input voltage range extends from 100 mV below ground to within 2.0 V of the most positive supply. Each filter section has a 2:1 input multiplexer that includes level-shifting circuitry. The level-shifting circuitry adds a dc component to ground-referenced input signals so that they can be reproduced accurately without the output buffers hitting the negative rail. Because the filters have negative rail input and rail-to-rail output, dc level shifting is generally not necessary, unless accuracy greater than that of the saturated output of the driver is required at the most negative edge. This varies with load but is typically 100 mV in a dc-coupled, single-supply application. If ac coupling is used, the saturated output level is higher because the drivers have to sink more current on the low side. If dual supplies are used ( $V_{S-} < \text{GND}$ ), no level shifting is required. In dual-supply applications, the level shifting circuitry can be used to take a ground referenced signal and put the blanking level at ground while the sync level is below ground.

The output drivers on the ADA4410-6 have rail-to-rail output capabilities. They provide either 6 dB or 12 dB of gain with respect to the ground pins. Gain is controlled by the external gain select pin. Each output is capable of driving two ac- or dc-coupled 75  $\Omega$  source-terminated loads. If a large dc output level is required while driving two loads, ac coupling should be used to limit the power dissipation.

Input MUX isolation is primarily a function of the source resistance driving into the ADA4410-6. Higher resistances result in lower isolation over frequency, while a low source resistance, such as 75  $\Omega$ , has the best isolation performance. In the SD channels, the isolation variation is most pronounced due to the stray capacitance that exists between the adjacent input pins. The HD input pins are not adjacent; therefore, this effect is less pronounced on the HD channels. See Figure 15 for a performance comparison of the different source resistances feeding the SD inputs.

# APPLICATIONS

## OVERVIEW

With its high impedance multiplexed inputs and high output drive, the ADA4410-6 is ideally suited to video reconstruction and antialias filtering applications. The high impedance inputs give designers flexibility with regard to how the input signals are terminated. Devices with DAC outputs that feed the ADA4410-6 can be loaded in whatever resistance provides the best performance, and devices with voltage outputs can be optimally terminated as well. The ADA4410-6 outputs can each drive up to two source-terminated 75 Ω loads and can therefore directly drive the outputs from set-top boxes, DVD players, and the like without the need for a separate output buffer.

Binary control inputs are provided to select cutoff frequency, throughput gain, and input signal. These inputs are compatible with 3 V and 5 V TTL and CMOS logic levels, referenced to GND. The disable feature is asserted by pulling the DISABLE pin to the positive supply.

A differential input, comprising of the LEVEL1 and LEVEL2 inputs, controls the dc level at the output pins. The output offset is nominally calculated as

$$V_{Os} (OUT) = (LEVEL2 - LEVEL1)(G) \tag{1}$$

where LEVEL2 and LEVEL1 are the voltages applied to the respective inputs and G is throughput gain.

## MULTIPLEXER SELECT INPUTS

Selection between the two multiplexer inputs is controlled by the logic signals applied to the MUX\_SD and MUX\_HD inputs. The MUX\_SD input controls the standard definition (SD) inputs, and the MUX\_HD input controls the high definition (HD) inputs. Table 6 summarizes the multiplexer operation.

## GAIN SELECT

The throughput gain of the ADA4410-6 signal paths can either be ×2 or ×4. Gain selection is controlled by the logic signal applied to the G\_SEL pin. Table 6 summarizes how the gain is selected.

## DISABLE

The ADA4410-6 includes a disable feature that can be used to save power when a particular device is not in use. As indicated in the Overview section, the disable feature is asserted by pulling the DISABLE pin to the positive supply. Table 6 summarizes the disable feature operation. The DISABLE pin also functions as a reference level for the logic inputs and, therefore, must be connected to ground when the device is not disabled.

Table 6. Logic Pin Function Description

DISABLE	MUX_HD	MUX_SD	G_SEL
V <sub>S+</sub> = Disabled	1 = HD Channel 1 Selected	1 = SD Channel 1 Selected	1 = ×4 Gain
GND = Enabled	0 = HD Channel 2 Selected	0 = SD Channel 2 Selected	0 = ×2 Gain

## CUTOFF FREQUENCY SELECTION

Four combinations of cutoff frequencies are provided for the HD video signals. The cutoff frequencies have been selected to correspond with the most commonly deployed HD scanning systems. Selection between the cutoff frequency combinations is controlled by the logic signals applied to the F\_SEL\_A and F\_SEL\_B inputs. Table 7 summarizes cutoff frequency selection.

Table 7. Filter Cutoff Frequency Selection

F_SEL_A	F_SEL_B	Y/G Cutoff (MHz)	Pb/B Cutoff (MHz)	Pr/R Cutoff (MHz)
0	0	36	36	36
0	1	36	18	18
1	0	18	18	18
1	1	9	9	9

## OUTPUT DC OFFSET CONTROL

The LEVEL1 and LEVEL2 inputs work as a differential input-referred output offset control. In other words, the output offset voltage of a given channel (with the exception of the CV channel) is equal to the difference in voltage between the LEVEL2 and LEVEL1 inputs, multiplied by the overall filter gain. This relationship is expressed in Equation 1. For example, with the G\_SEL input set for ×2 gain, setting LEVEL2 to 300 mV and LEVEL1 to 0 V shifts the offset voltages at the ADA4401-6 outputs to 600 mV. This particular setting can be used in most single-supply applications to keep the output swings safely above the negative supply rail.

The CV output is developed by passively summing the Y and C outputs that have passed through their respective output gain stages, then multiplying this sum by a factor of two to obtain the output (see Figure 1). The offset of this output is therefore equal to two times that of the other outputs. Because of this, in many cases it is necessary to ac-couple the CV output or ensure that it is connected to an input that is ac-coupled. This is generally not an issue because it is common practice to employ ac coupling on composite video inputs.

The maximum differential voltage that can be applied across the LEVEL1 and LEVEL2 inputs is ±500 mV. From a single-ended standpoint, the LEVEL1 and LEVEL2 inputs have the same range as the filter inputs. See the Specifications tables for the limits. The LEVEL1 and LEVEL2 inputs must each be bypassed to GND with a 0.1 μF ceramic capacitor.

In single-supply applications, a positive output offset must be applied to keep the negative-most excursions of the output signals above the specified minimum output swing limit.

Figure 23 and Figure 24 illustrate several ways to use the LEVEL1 and LEVEL2 inputs. Figure 23 shows an example of how to generate fully adjustable LEVEL1 and LEVEL2 voltages from  $\pm 5$  V supplies. Figure 24 illustrates an effective way to produce a 600 mV output offset voltage in a single-supply application. Although the LEVEL1 input could simply be connected to GND, Figure 24 includes bypassed resistive voltage dividers for each input so that the input levels can be changed, if necessary. Additionally, many in-circuit testers require that I/O signals not be tied directly to the supplies or GND. DNP indicates do not populate.

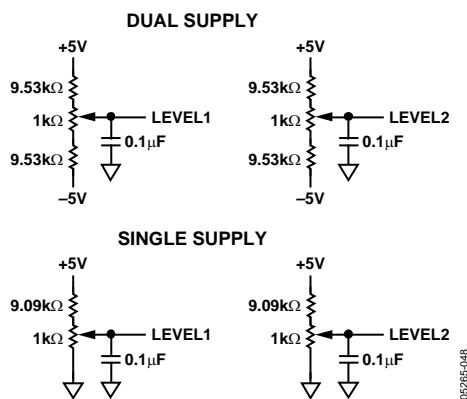


Figure 23. Generating Fully Adjustable Output Offsets

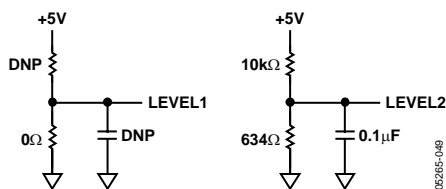


Figure 24. Setting Output Offsets to 600 mV on a Single Supply

## INPUT AND OUTPUT COUPLING

Inputs to the ADA4410-6 are normally dc-coupled. Ac coupling the inputs is not recommended; however, if ac coupling is necessary, a suitable resistive network must be provided following the ac coupling element to provide proper level shifting and bias currents for the ADA4410-6 input stages.

The ADA4410-6 outputs can be either ac- or dc-coupled. As discussed in the Output DC Offset Control section, the CV output offset is different than the other outputs and is generally ac-coupled.

## PRINTED CIRCUIT BOARD LAYOUT

As with all high speed applications, attention to printed circuit board layout is of paramount importance. Standard high speed layout practices should be adhered to when designing with the ADA4410-6. A solid ground plane is recommended, and surface-mount ceramic power supply decoupling capacitors should be placed as close as possible to the supply pins. All of the ADA4410-6 GND pins should be connected to the ground plane with traces that are as short as possible. Controlled impedance traces of the shortest length possible should be used to connect to the signal I/O pins and should not pass over any voids in the ground plane. A 75  $\Omega$  impedance level is typically used in video applications. All signal outputs of the ADA4410-6 should include series termination resistors when driving transmission lines.

When the ADA4410-6 receives its inputs from a device with current outputs, the required load resistor value for the output current is most often different from the characteristic impedance of the signal traces. In this case, if the interconnections are sufficiently short ( $\ll 0.1$  wavelength), the trace does not have to be terminated in its characteristic impedance. Figure 25 shows an example in which the ADA4410-6 input originates from DACs that require 300  $\Omega$  load resistors. Traces of 75  $\Omega$  can be used in this instance, provided their lengths are an inch or two at the most. This is easily achieved because the ADA4410-6 and the device feeding it are usually adjacent to each other, and connections can be made that are less than one inch in length.

**VIDEO ENCODER RECONSTRUCTION FILTER**

The ADA4410-6 is easily applied as a reconstruction filter at the DAC outputs of a video encoder. Figure 25 illustrates how to use the ADA4410-6 in this type of application with an ADV7314 video encoder in a single-supply application with ac-coupled outputs.

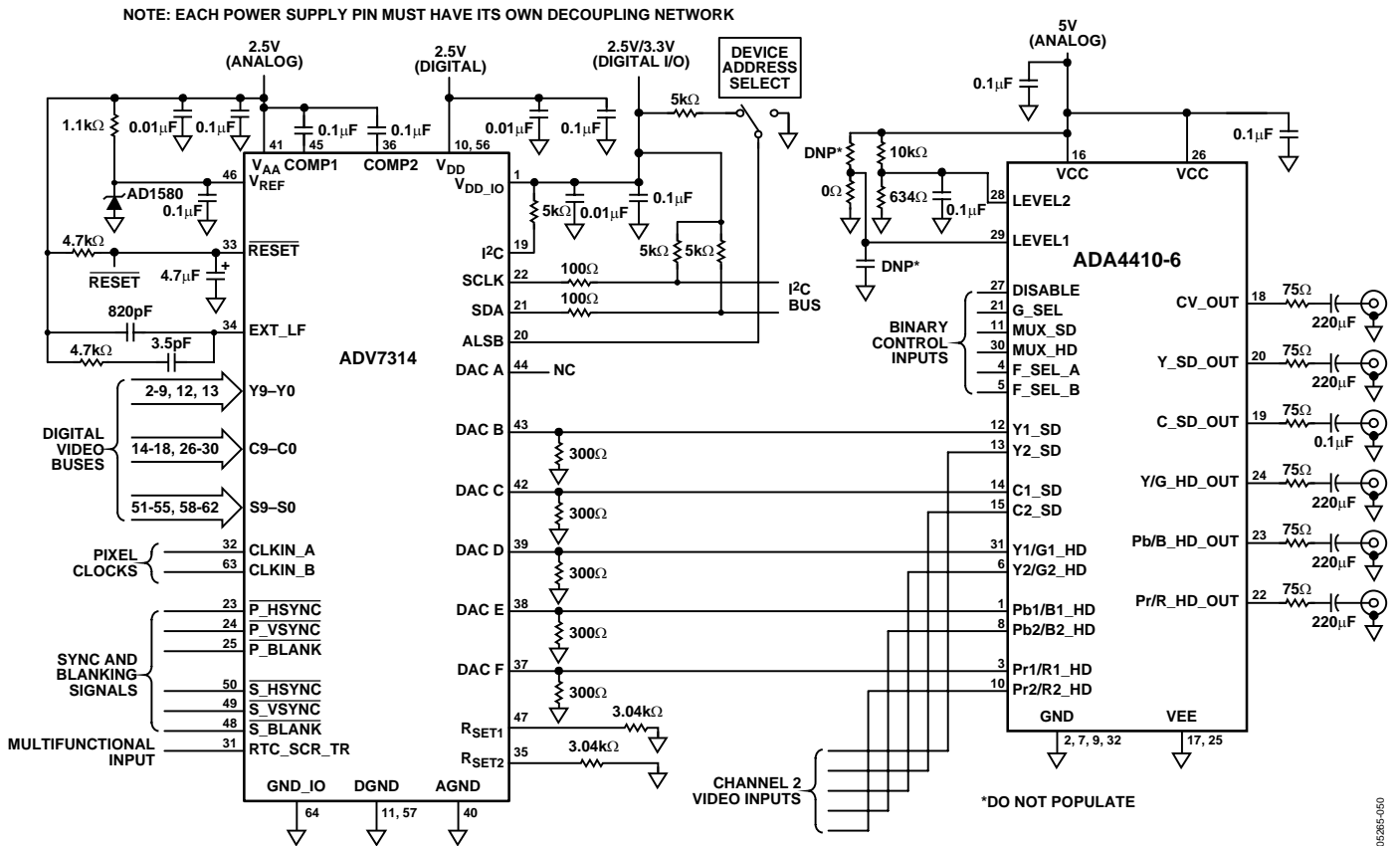
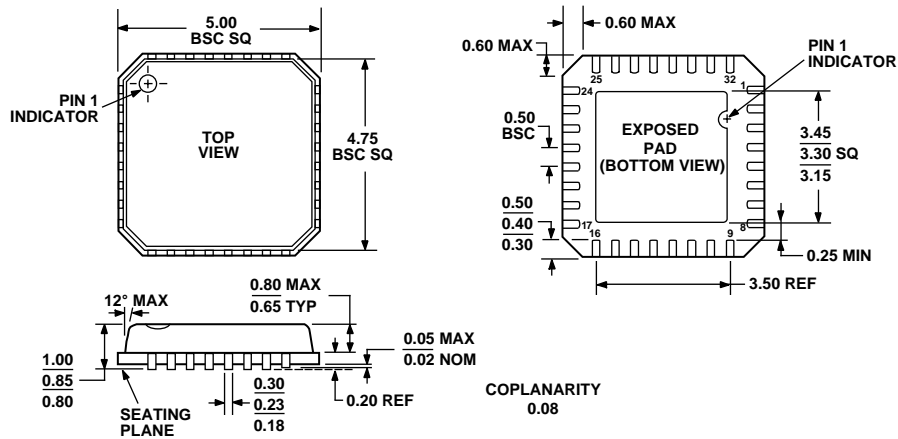


Figure 25. The ADA4410-6 Applied as a Reconstruction Filter Following the ADV7314

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 26. 32-Lead Lead Frame Chip Scale Package [VQ\_LFCSP]  
 5 mm × 5 mm Body, Very Thin Quad (CP-32-3)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4410-6ACPZ-R2 <sup>1</sup>	-40°C to +85°C	32-Lead Lead Frame Chip Scale Package (VQ_LFCSP)	CP-32-3
ADA4410-6ACPZ-R7 <sup>1</sup>	-40°C to +85°C	32-Lead Lead Frame Chip Scale Package (VQ_LFCSP)	CP-32-3
ADA4410-6ACPZ-RL <sup>1</sup>	-40°C to +85°C	32-Lead Lead Frame Chip Scale Package (VQ_LFCSP)	CP-32-3

<sup>1</sup> Z = Pb-free part.