19-0297; Rev 1; 9/95

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

300Msps, 12-Bit DAC with Complementary Voltage Outputs

MAX555

General Description

The MAX555 is an advanced, monolithic, 12-bit digital-to-analog converter (DAC) with complementary 50Ω outputs. Fabricated using an oxide-isolated bipolar process, the MAX555 is designed for signal-reconstruction applications at an output update rate of 300Msps. It incorporates an analog multiplying function with 10MHz useable input bandwidth. The voltage-output DAC uses precision laser trimming to achieve 12-bit accuracy with ±1/2LSB integral and differential linearity (±0.012% FS). Absolute gain error is a low 1% of full scale. Full-scale transitions occur in less than 0.5ns. Internal registers and a unique decoder reduce glitching and allow the MAX555 to achieve precise RF performance with over 73dBc of spurious-free dynamic range at 50Msps with f_{OUT} = 3.1MHz, or 62dBc at 300Msps with f_{OUT} = 18.6MHz.

The MAX555 operates from a single -5.2V supply and dissipates 980mW (nominal). It comes in a 68-pin thermally enhanced PLCC package capable of accepting a heatsink.

Applications

- Direct Digital Synthesis
- Arbitrary Waveform Generation
- HDTV/High-Resolution Graphics
- Instrumentation
- Communications Local Oscillators
- Automated Tester Applications

Features

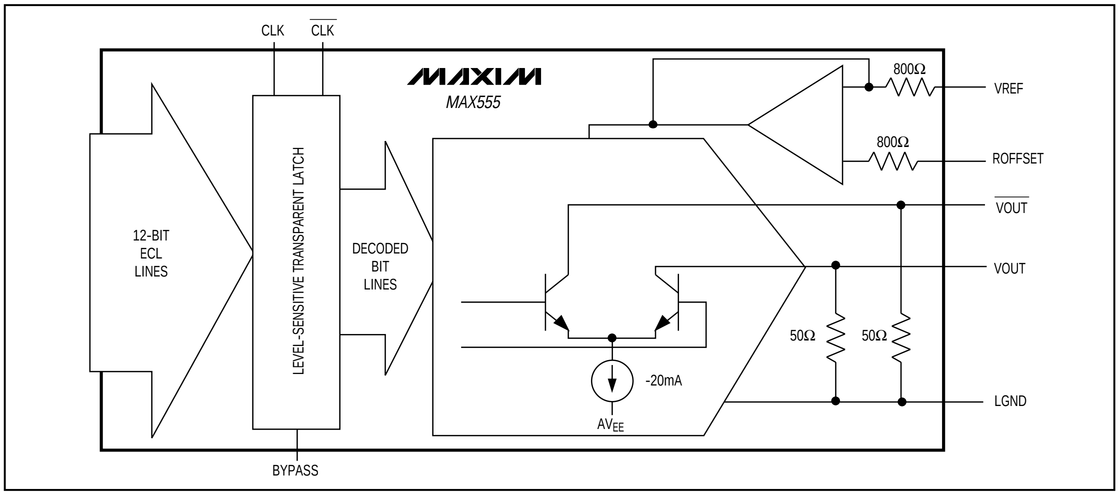
- **12-Bit Resolution**
- **±1/2LSB Integral and Differential Nonlinearity**
- **Capable of 300Msps Min Update Rate**
- **Complementary 50Ω Outputs**
- **Multiplying Reference Input**
- **Low Glitch Energy (5.6pVs)**
- **Single -5.2V Power Supply**
- **On-Chip Data Registers**
- **ECL-Compatible Inputs with Differential Clock**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX555CQK	0°C to +70°C	68 Thermally Enhanced PLCC

Pin Configuration appears at end of data sheet.

Simplified Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (AV_{EE}) ....-7V to +0.3V
Digital Supply Voltage (DV_{EE}) ....-7V to +0.3V
Digital Input Voltage (D0–D11) ....-5.5V to 0V
Reference Input Voltage (V_{IN}) ....0V to +1.25V
Reference Input Current...................................0mA to +1.56mA
Output Compliance Voltage (V_{OC})......................-1.25V to +1.0V
Output Common-Mode Voltage (V_{CM}) ....-0.25V to +1.0V

Continuous Power Dissipation (T_A = +70°C)
(without additional heatsink) 1.3W
Operating Temperature Range..............................0°C to +70°C
Junction Temperature Range (Note 1) ....0°C to +150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Note 1: Typical thermal resistance, junction-to-case $R_{\theta JC}$ = 28°C/W. See *Package Information.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{EE} = DV_{EE} = -5.2V, V_{REF} = 1.000V, T_{MIN} to T_{MAX} = 0°C to +70°C, unless otherwise noted.) (Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Differential Linearity Error	DLE1	V_{REF} = 1.000V, current out, into virtual ground, end-point linearity	$\overline{VOUT}$	-0.012	±0.003	0.012	% Full Scale
	DLE2		VOUT	-0.05	±0.01	0.05	
Integral Linearity Error	ILE1	V_{REF} = 1.000V, current out, into virtual ground, end-point linearity	$\overline{VOUT}$	-0.012	±0.006	0.012	% Full Scale
	ILE2		VOUT	-0.05	±0.01	0.05	
Absolute Gain Error	EG	V_{REF} = 1.000V, voltage out, $\overline{VOUT}$/VIN (Note 3)		-1.0	±0.2	1.0	% Full Scale
12-Bit Monotonicity					Guaranteed		
Output Offset Current	I_{OS}	D0–D11 = logic 1, V_{REF} = 1.000V, measured at $\overline{VOUT}$			40	100	µA
Output Leakage Current	I_{LEAK}	D0–D11 = logic 0, V_{REF} = 0V, measured at $\overline{VOUT}$			3	50	µA
TIME-DOMAIN PERFORMANCE (Note 4)							
Fall Time	t_{FALL}	90% to 10%, T_A = +25°C			510		ps
Rise Time	t_{RISE}	10% to 90%, T_A = +25°C			450		ps
Glitch Energy		Major carry, T_A = +25°C			5.6		pVs
Settling Time		±0.1% FSR			4		ns
		±0.024% FSR, 1LSB change			15		
DYNAMIC PERFORMANCE (Notes 4, 5)							
Spurious-Free Dynamic Range		f_{OUT} = 5MHz, f_{CLK} = 50MHz			70		dBc
		f_{OUT} = 10MHz, f_{CLK} = 50MHz			70		
		f_{OUT} = 20MHz, f_{CLK} = 100MHz			65		
		f_{OUT} = 30MHz, f_{CLK} = 100MHz			60		
		f_{OUT} = 30MHz, f_{CLK} = 200MHz			56		
		f_{OUT} = 40MHz, f_{CLK} = 200MHz			53		
		f_{OUT} = 40MHz, f_{CLK} = 250MHz			52		
		f_{OUT} = 50MHz, f_{CLK} = 250MHz			51		
		f_{OUT} = 40MHz, f_{CLK} = 300MHz			52		
		f_{OUT} = 50MHz, f_{CLK} = 300MHz			51		
Output Noise		Bits 0–11 high, T_A = +25°C			10.6		$\frac{nV}{\sqrt{Hz}}$

ELECTRICAL CHARACTERISTICS (continued)

($AV_{EE} = DV_{EE}$ = -5.2V, V_{REF} = 1.000V, T_{MIN} to T_{MAX} = 0°C to +70°C, unless otherwise noted.) (Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input Current, Logic High	I_{IH}	V_{IH} = -0.75V		10	200	µA
Input Current, Logic Low	I_{IL}	V_{IL} = -1.95V		1	2	µA
Logic "1" Voltage	V_{IH}		-1.1	-0.75	0	V
Logic "0" Voltage	V_{IL}		-2.0	-1.95	-1.48	V
DIGITAL TIMING						
Data Update Rate	f_D	Minimum data rate = DC (Note 6)	300			MHz
Data-to-Clock Setup Time	t_{SU}	Bypass = 0, clocked mode (Notes 4, 7)		1		ps
Data-to-Clock Hold Time	t_{HOLD}	Bypass = 0, clocked mode (Notes 4, 7)		1.8		ns
Clock-to-VOUT Propagation Delay	t_{PD3}	Bypass = 0, clocked mode (Notes 4, 7)		2.0		ns
LSBs Data-to-VOUT Propagation Delay	t_{PD2}	Bypass = 1, transparent mode (Notes 4, 7)		1.5		ns
MSBs Data-to-VOUT Propagation Delay	t_{PD1}	Bypass = 1, transparent mode (Notes 4, 7)		2.1		ns
MSBs Decode Delay	t_{DD}	Bypass = 1, transparent mode (Notes 4, 7)		600		ps
CONTROL AMPLIFIER						
Amplifier Input Resistance	R_{IN}	V_{REF} = 1.000V	775	800	825	Ω
Multiplying Input Bandwidth	BW	-3dB		10		MHz
Open-Loop Gain	AV_{OL}	T_A = +25°C	3	20		kV/V
Input Offset Voltage	V_{OS}	T_A = +25°C	-250	0	250	µV
OUTPUT PERFORMANCE						
Full-Scale Output Current	I_{OUT}	V_{REF} = 1.000V, R_L = 0Ω	19.0	20.0	21.0	mA
Output Resistance	R_{OUT}	VOUT, $\overline{VOUT}$	49.5	50.0	50.5	Ω
Output Capacitance	C_{OUT}	VOUT, $\overline{VOUT}$		15		pF
POWER SUPPLIES						
Analog Power-Supply Current	AI_{EE}	$AV_{EE} = DV_{EE}$ = -5.2V	30	46	60	mA
Digital Power-Supply Current	DI_{EE}	$AV_{EE} = DV_{EE}$ = -5.2V	110	150	190	mA
Power Dissipation	PD			0.98	1.3	W
Package Thermal Resistance, Junction to Ambient	T_{JA}			28		°C/W

Note 2: All devices are 100% production tested at +25°C and are guaranteed by design for $T_A = T_{MIN}$ to T_{MAX} as specified.

Note 3: The gain-error method of calculation is shown below:

Definition:

$$EG(\%) = \frac{[V_{MEASURE(FS)} - V_{IDEAL(FS)}] \times 100}{V_{IDEAL(FS)}}$$

where FS indicates full-scale measurements.

EG Method:

$$EG = \frac{[(4096 / 4095)\, V_{MEASURE} - 16(V_{REF} / R_{IN})\,(R_{OUT})] \times 100}{16(V_{REF} / R_{IN})\,(R_{OUT})} \%$$

$$= \frac{[(4096 / 4095)\, V_{MEASURE} - 1] \times 100}{1} \%$$

where: V_{REF} = 1.000V, R_{IN} = 800Ω, R_{OUT} = 50Ω, $V_{MEASURE}$ = $\overline{VOUT}$ (FS).

Note 4: Dynamic and timing specifications are obtained from device characterization and simulation testing and are not production tested.

Note 5: Spurious-free dynamic range is measured from the fundamental frequency to any harmonic or non-harmonic spurs within the bandwidth $f_{CLK}/2$, unless otherwise specified.

Note 6: Guaranteed by design.

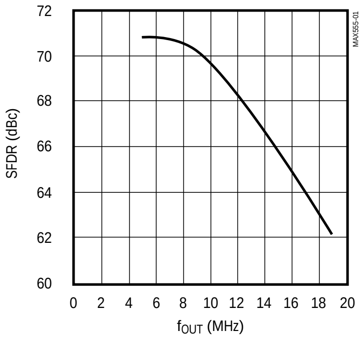
Note 7: Timing definitions are detailed in Figure 2.

300Msps, 12-Bit DAC with Complementary Voltage Outputs

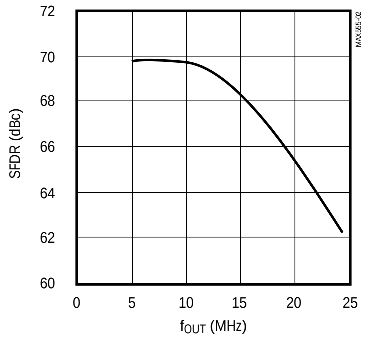
Typical Operating Characteristics

(VREF = 0.75V, T_A = +25°C, unless otherwise noted.)

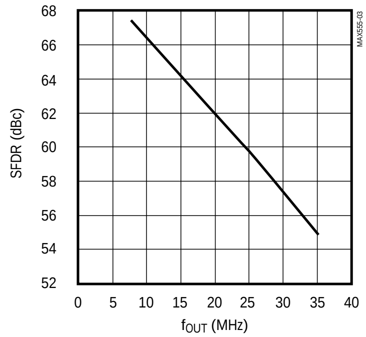
SPURIOUS-FREE DYNAMIC RANGE vs. f_{OUT} (f_{CLK} = 50MHz)



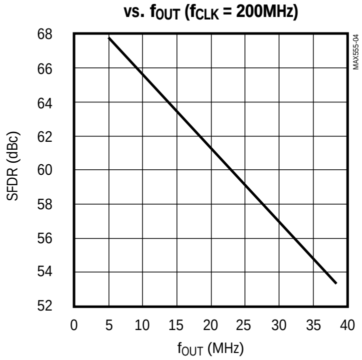
SPURIOUS-FREE DYNAMIC RANGE vs. f_{OUT} (f_{CLK} = 100MHz)



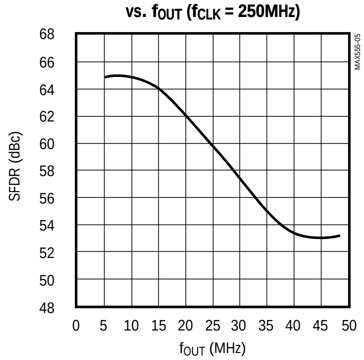
SPURIOUS-FREE DYNAMIC RANGE vs. f_{OUT} (f_{CLK} = 150MHz)



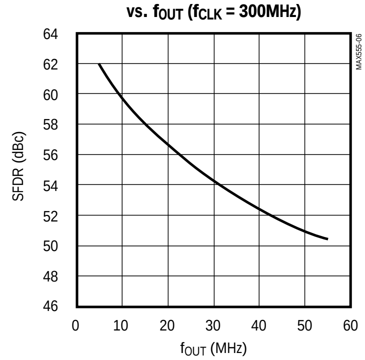
SPURIOUS-FREE DYNAMIC RANGE vs. f_{OUT} (f_{CLK} = 200MHz)



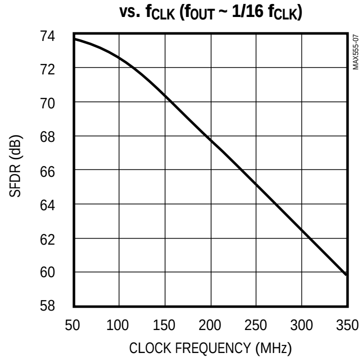
SPURIOUS-FREE DYNAMIC RANGE vs. f_{OUT} (f_{CLK} = 250MHz)



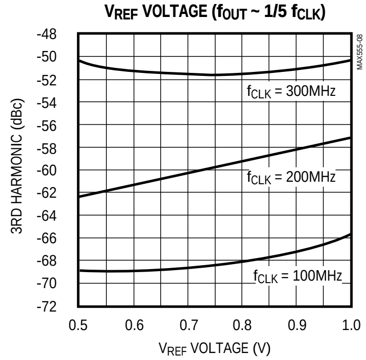
SPURIOUS-FREE DYNAMIC RANGE vs. f_{OUT} (f_{CLK} = 300MHz)



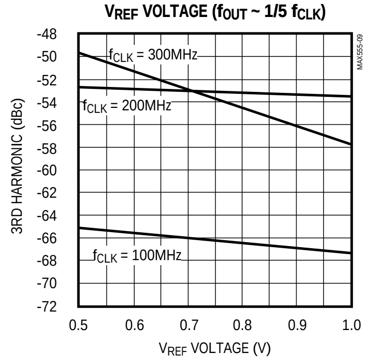
SPURIOUS-FREE DYNAMIC RANGE vs. f_{CLK} (f_{OUT} ~ 1/16 f_{CLK})



3RD HARMONIC DISTORTION vs. V_{REF} VOLTAGE (f_{OUT} ~ 1/5 f_{CLK})



2ND HARMONIC DISTORTION vs. V_{REF} VOLTAGE (f_{OUT} ~ 1/5 f_{CLK})



Pin Description

PIN	NAME	FUNCTION
1	BYPASS	Disables latching of data when high (ECL input)
2	CLK	Data Clock (ECL input)
3	$\overline{CLK}$	Data Clock Not (ECL input)
4, 56, 57, 63, 66	DGND	Digital Signal Grounds
5, 55	DV_{EE}	-5.2V Digital Power Supplies
10, 11, 12, 21–25, 27, 31, 36, 37, 40, 41, 43, 45, 46, 61	N.C.	No Connection
13, 14	VOUT	DAC Outputs
15, 16	LGND	Ladder Grounds
17, 18	$\overline{VOUT}$	DAC Output Complements
19, 49, 51, 52, 53, 68	TN	Test Node—internal test point, do not connect
20, 29, 30, 48	AGND	Analog Signal Grounds
26, 44	HS	Heatspreader Connections—bypass with 0.1µF to AV_{EE}
28	ALTCOMPIB	PTAT-IB Reference Compensation Output (connect bypass capacitor to AV_{EE})
32	LOOPCRNT	Test node—must connect to AGND
33, 34	AV_{EE}	-5.2V Analog Power Supplies
35	VREF/2	Analog Reference Voltage Center-Tap Input
38, 39	VREF	Analog Reference Voltage Inputs (Kelvin connection)
42	ROFFSET	Offset Compensation Input
47	ALTCOMPC	Control-Amplifier PTAT Reference Compensation Input (connect bypass capacitor to AV_{EE})
50	LBIAS	Ladder-Bias Alternate Compensation Output (connect bypass capacitor to AV_{EE})
54, 58, 59, 60, 62, 64, 65, 67, 6, 7, 8, 9	D11(MSB)–D0(LSB)	Data Words (ECL inputs)

Detailed Description

Figure 1's functional diagram shows the MAX555's three major divisions: a digital section, a control-amplifier section, and a resistor-divider network. The digital section consists of a master/slave register, decoding logic, and current switches. The control-amplifier section includes a control amplifier and an array of 23 current sources divided into three groups. The resistor divider scales the currents from these groups to achieve the correct binary weighting at the output. The output of the resistor-divider network is laser trimmed to 50Ω, a key feature for driving into controlled impedance transmission lines.

The first group of current sources comprises the six MSBs, D11–D6 (resulting in 15 identical, plus two binary weighted currents), which are applied directly to the output of the resistor-divider network. The second group, bits D5–D3 (three binary weighted currents), is applied to the middle of the divider network. The middle of the network divides the current seen at the output by 8. The third group, bits D2–D0 (three additional binary weighted current sources), is applied to the input of the resistive network, dividing the current seen at the output by 64.

Glitching is reduced by decoding the four MSBs into 15 identical current sources and synchronizing data with a master/slave register at every current switch. Data bits are transferred to the output on the positive-going edge of the clock, with the BYPASS input asserted low. In the asynchronous mode with the BYPASS input asserted high, the latches are transparent and data is transferred to the output regardless of the clock state. All digital inputs are ECL compatible. The clock input is differential.

The control amplifier forces a reference current, which is replicated in the current sources. This reference current is nominally 1.25mA. It can be supplied by an external current source, or by an external voltage source of 1.000V applied to the VREF input.

A reference input of V_{REF} = 1.000V will produce a full-scale output voltage of V_{FS} = -1.000V, where:

$$V_{FS} = 4096 / 4095 \times \overline{VOUT} \text{ (code 0)}$$

for the $\overline{VOUT}$ output. The output coding is summarized in Table 1.

The DAC's control amplifier has a typical open-loop voltage gain of 85dB, and its gain-magnitude bandwidth is flat up to 10MHz. When the control amplifier is not being used for high-speed multiplying applications, it is recommended that a 0.4µF capacitor be connected from LBIAS to AV_{EE} to increase control-amplifier stability and reduce current-source noise.

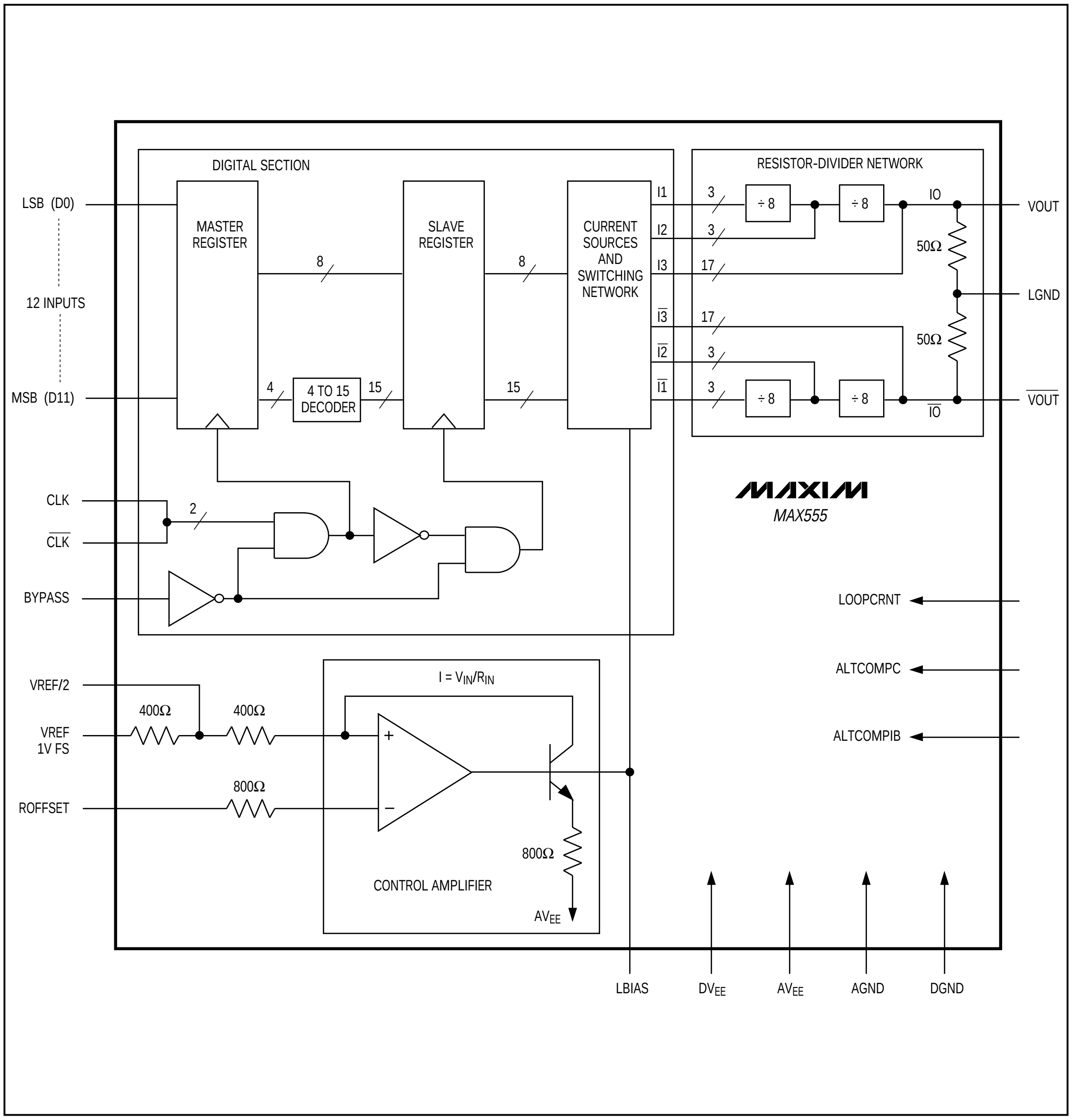


Figure 1. Functional Diagram

Table 1. Output Coding

DIGITAL CODE (D11–D0)	$\overline{VOUT}$ (V)	VOUT (V)
000000000000	-0.999756	0
000000000001	-0.999512	-0.000244
011111111111	-0.500000	-0.499756
100000000000	-0.499756	-0.500000
111111111111	0	-0.999756

Timing Information

The MAX555 features a differential ECL clock input with selective transparent operation (BYPASS = 1). It is possible to drive the MAX555 clock single-ended if desired by tying the $\overline{CLK}$ input to an external voltage of -1.3V (ECL V_{BB}). However, using a differential clock provides greater noise immunity and improved dynamic performance.

In the clocked mode (BYPASS = 0), when the clock line is low, the slave register is locked out and information on the digital inputs is permitted to enter the master register. The clock transition from low to high locks the master register in its present state and ignores further changes on the digital inputs. This transition simultaneously transfers the contents of the master register to the slave register, causing the DAC output to change.

Figure 2's timing diagram illustrates the importance of operating the MAX555 in the clocked mode. In the transparent mode (BYPASS = 1), both the master and slave registers are transparent, and changes in input data ripple directly to the output. Because the four MSBs are decoded into 15 identical currents, there is a decode delay for these bits that is longer than for the eight LSBs. For the full-scale transition case shown, an intermediate output of 1/16 full-scale occurs until the four MSBs are properly decoded. This decode delay seriously degrades the device's spurious performance. In addition, skew in the timing of the input data also directly appears at the DAC output, further degrading high-speed performance.

MAX555 operation in the clocked mode (BYPASS = 0) with a differential clock precludes both of these potential problems and is required for high-speed operation. Since input data can only enter the master register when the clock is low (while the slave register is locked out), data-bus timing skew and the internal MSB decode delay will not appear at the DAC output. The DAC currents are switched only when the clock transitions from low to high, after the internal data stabilizes.

Layout and Power Supplies

The MAX555 has separate pins for analog and digital supplies. AV_{EE} and DV_{EE} are connected to each other through the substrate of the IC. These potentials should be derived from the same supply to minimize voltage mismatch, which would cause substrate current flow and possible latchup. Appropriate decoupling is needed to prevent digital-section current spikes from affecting the analog section (Figure 4).

It is recommended that a multilayer PC board be used, containing a solid ground and power planes. All analog

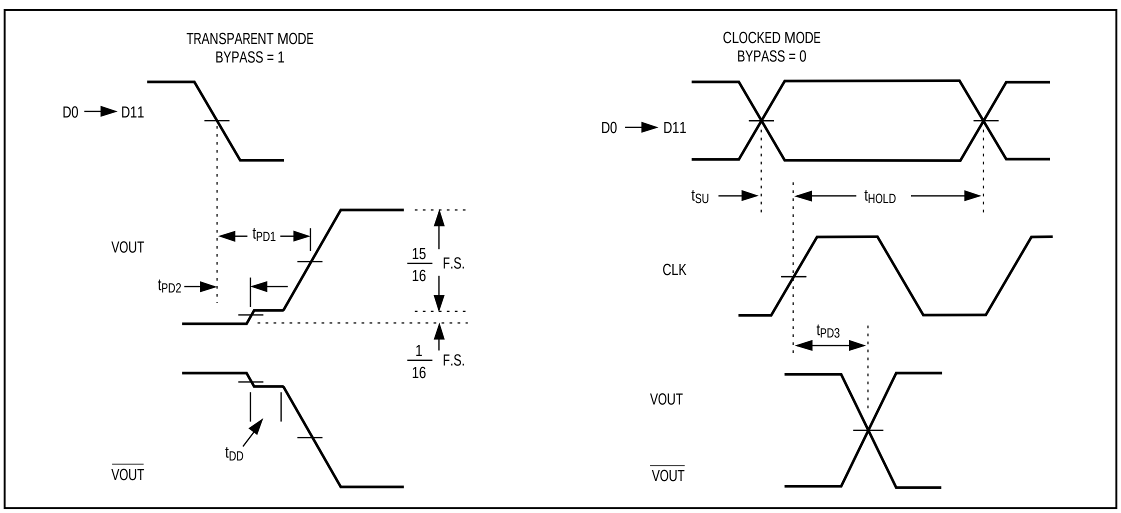


Figure 2. Timing Diagram

and digital ground pins must be connected directly to the analog ground plane at the MAX555, preferably with a "star connection" at the LGND pins (15 and 16).

High-speed ECL inputs, as well as the output from the MAX555, should employ good transmission-line techniques, with terminations close to the device pins. Separate power-supply buses for analog and digital power supplies are recommended as good general practice. Best results will be achieved by bypassing the device pins with high-quality ceramic chip capacitors connected physically close to the pins.

Applications Information

Reference Input

The MAX555 uses an internal op-amp circuit to buffer the reference current. The input to the op amp may be driven with a 1.25mA external current source or a 1V external voltage reference. The reference input is the VREF pin. The input impedance to the op amp is 800Ω. As shown in Figure 1, VREF/2 is brought out externally with 400Ω of impedance to the op amp. These reference inputs can be used to vary the full-scale output for high-speed multiplying applications. R_{OFFSET} must be connected to analog ground. In addition, a 0.1µF capacitor should be connected from VREF/2 to analog ground to reduce reference current noise.

Outputs

The analog outputs are laser trimmed to 50Ω. They can be used either as a voltage drive with 50Ω impedance, or to drive into a virtual null using a transimpedance amplifier. Greater speed is achieved driving into 50Ω loads. The differential outputs of the MAX555 may be used to drive a balun for conversion to a single-ended output, while at the same time greatly reducing the second-harmonic content of the output.

Dynamic Performance

The *Typical Operating Characteristics* graphs show the MAX555's performance when used in direct digital synthesis (DDS) applications for generating RF sine waves. The first six graphs show the MAX555's spurious-free dynamic range (SFDR) for clock frequencies of 50MHz to 300MHz at various output frequencies. The seventh graph shows the SFDR for clock frequencies from 50MHz to 350MHz while producing an output frequency of about 1/16 the clock frequency.

The last two graphs show the MAX555's third and second harmonic distortion while producing an output frequency of about 1/5 f_{CLK} for clock frequencies from 100MHz to 300MHz as a function of the reference voltage. The third harmonic content of the output can be reduced at clock frequencies below about 200MHz by reducing the reference voltage from its 1.000V nominal value. At clock frequencies above about 200MHz, the output's third harmonic content is dominated by coupling from the high-speed digital inputs to the output. Reducing the reference voltage at these high clock rates actually increases the third harmonic distortion in the output, since the carrier amplitude drops but the third harmonic level remains relatively constant.

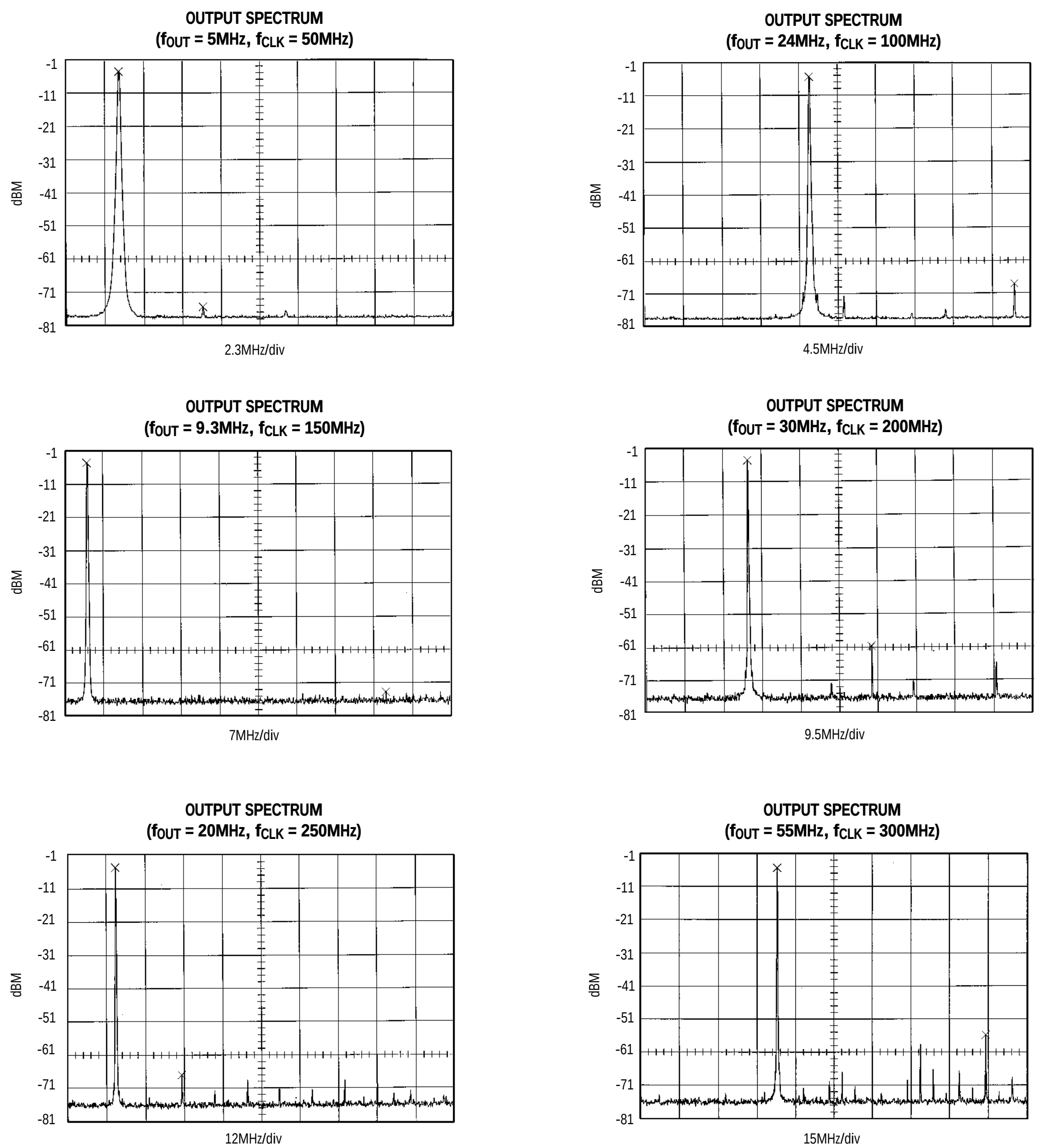
The second harmonic distortion of the outputs is shown as a function of clock frequency and reference voltage. It is relatively constant for clock frequencies below about 200MHz at different V_{REF} values. As with the third harmonic distortion, however, the second harmonic distortion also increases at clock frequencies over 200MHz for lower V_{REF} values. Minimize these effects by bypassing the MAX555 heatspreader (pins 26 and 44) to V_{EE} with a good-quality RF chip capacitor. Reducing the swing of the input logic levels and/or decreasing the rise time of the digital signals can also improve the output's harmonic content. Combining these techniques achieves the best results. Some experimentation may be required to optimize the MAX555's performance for a particular application.

Figure 3 shows the spectrum analyzer plots of the MAX555 when used in DDS applications. These plots show the MAX555's output spectrum at clock frequencies from 50MHz to 300MHz while producing various output frequencies. Observing the output spectrum while adjusting the reference voltage or varying the logic levels is a sensitive method of optimizing MAX555 performance. The plots shown were obtained with a +0.75V reference voltage with 500mV ECL logic swings.

Typical Application

Figure 4 shows a typical connection. With $\overline{VOUT}$ used to drive a 50Ω line, the unused complementary output, VOUT, should also be terminated to 50Ω. A 1V reference voltage at VREF gives a -0.5V full-scale voltage at $\overline{VOUT}$ (when doubly terminated with 50Ω on the output). Because some loads may represent a complex impedance, be sure to match the output impedance with the load. Mismatching the impedances can cause reflections that will affect AC-performance parameters.

In all applications, the LOOPCRNT pin is always connected to AGND, and compensation capacitors are connected to pins ALTCOMPC, ALTCOMPIB, and LBIAS. The LBIAS compensation is recommended for non-multiplying applications. AC grounding the heat spreader on the package (with pins 26 and 44) reduces digital noise feedthrough and improves the MAX555's spurious performance at high data rates.



Measurement Conditions: 10dB/div vertical display, 300Hz video filter, TEK2755AP spectrum analyzer VREF = 0.75V, T_A = +25°C, unless otherwise noted.

Figure 3. Spectrum Analyzer Plots

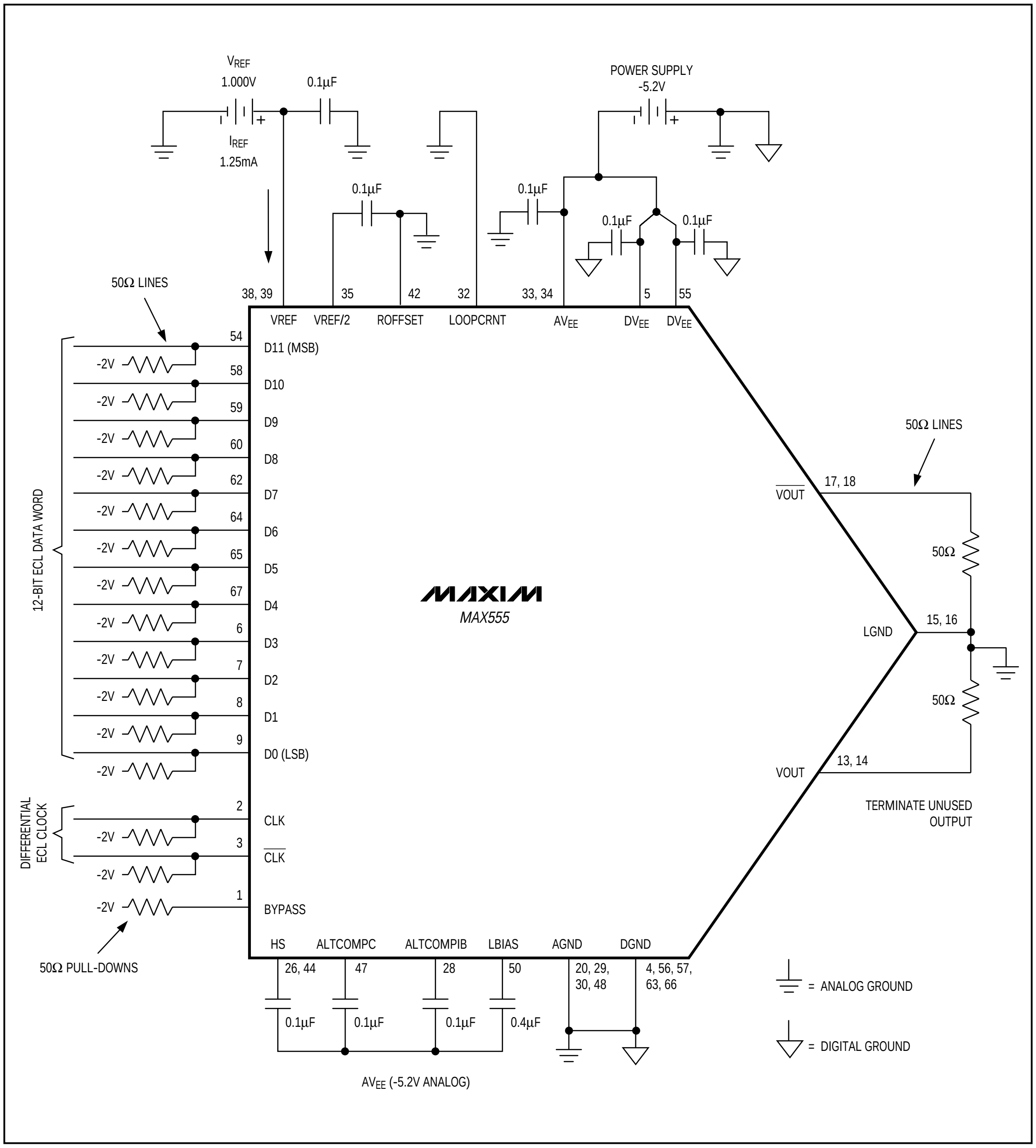
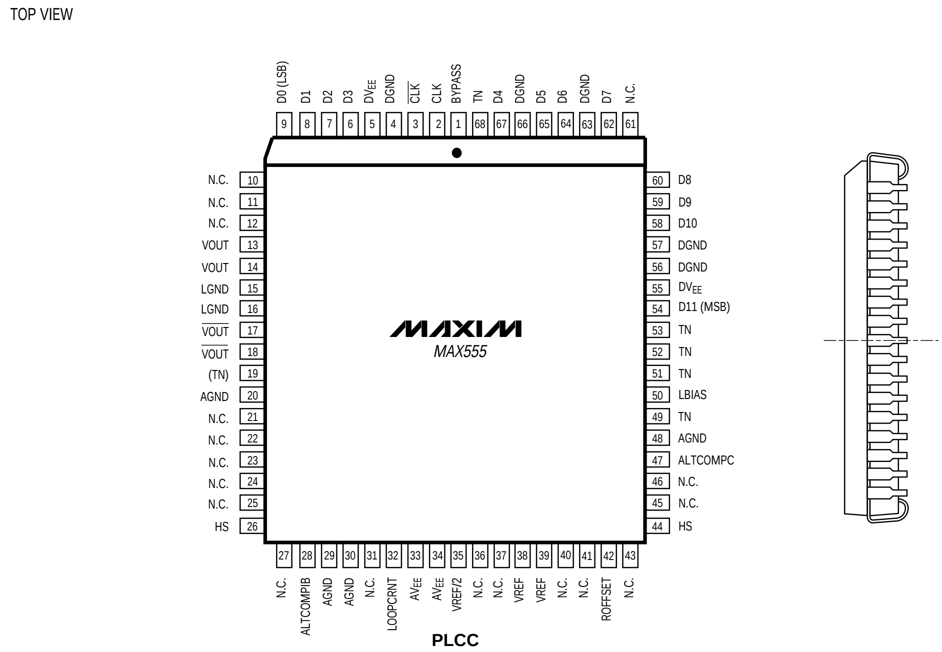
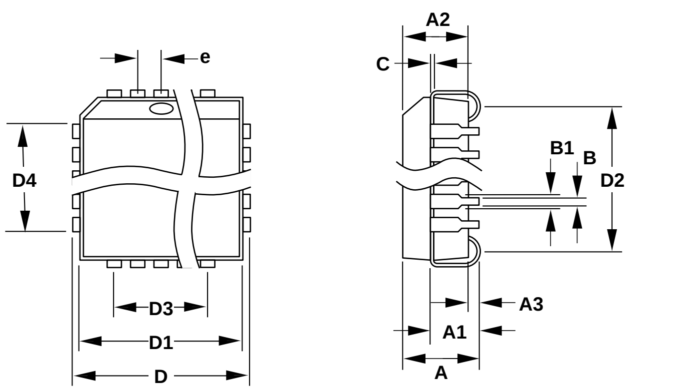


Figure 4. Typical Application

Pin Configuration



Package Information



Q PACKAGE
PLASTIC
LEADED CHIP CARRIER

NOTES:
1. D1 DOES NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR THE PROTRUSIONS NOT TO EXCEED .20mm (.008") PER SIDE
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MO047-XX AS SHOWN IN TABLE
6. N = NUMBER OF PINS
7. D4 APPLIES TO THERMALLY ENHANCED PACKAGES ONLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3		0.200 REF		5.08 REF	
D	28	0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2		0.390	0.430	9.91	10.92
D3		0.300 REF		7.62 REF	
D4		0.300	–	7.62	–
D	44	0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2		0.590	0.630	14.99	16.00
D3		0.500 REF		12.70 REF	
D4		0.470	–	11.94	–
D	68	0.985	0.995	25.02	25.27
D1		0.950	0.958	24.13	24.33
D2		0.890	0.930	22.61	23.62
D3		0.800 REF		20.32 REF	
D4		0.625	–	15.87	–