19-3119; Rev 0; 12/03

MAXIM

±10V, 12-Bit, Serial, Voltage-Output DAC

General Description

The MAX5312 12-bit, serial-interface, digital-to-analog converter (DAC) provides bipolar ±5V to ±10V outputs from ±12V to ±15V power-supply voltages, or a unipolar 5V to 10V output from a single 12V to 15V power-supply voltage.

The MAX5312 features excellent linearity with both integral nonlinearity (INL) and differential nonlinearity (DNL) guaranteed to ±1 LSB (max). The device also features a fast 10µs to 0.5 LSB settling time, and a hardware-shutdown feature that reduces current consumption to 3.5µA. The output goes to midscale at power-up in bipolar mode (0V), and to zero scale at power-up in unipolar mode (0V). A clear input ($\overline{CLR}$) asynchronously clears the DAC register and sets the output to 0V. The output can be asynchronously updated with the load DAC ($\overline{LDAC}$) input.

The device features a 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial interface that operates with 3V or 5V logic. Additional features include a serial-data output (DOUT) for daisy chaining and readback functions. The MAX5312 requires a 2V to 5.25V external reference voltage and is available in a 16-pin SSOP package that operates over the extended -40°C to +85°C temperature range.

Applications

Motor Control

Industrial Process Controls

Industrial Automation

Automatic Test Equipment (ATE)

Analog I/O Boards

Data-Acquisition Systems

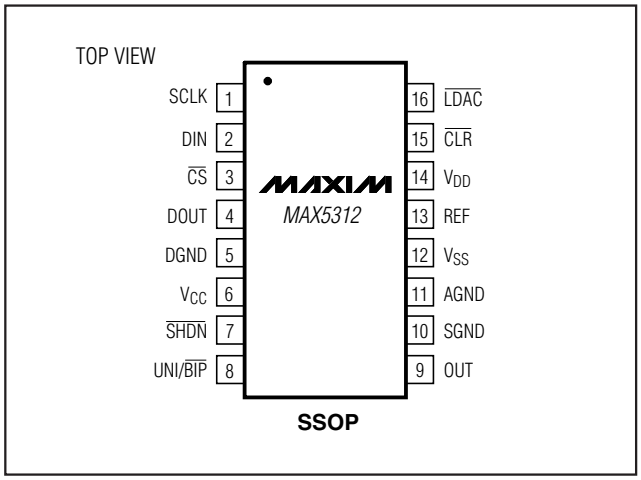
Features

- **Unipolar or Bipolar Output-Voltage Ranges**
  Unipolar: 0 to (+2 x V_{REF}) (Single or Dual Supply)
  Bipolar: (-2 x V_{REF}) to (+2 x V_{REF}) (Dual Supply)
- **Guaranteed INL ≤ ±1 LSB (max)**
- **Guaranteed Monotonic: DNL ≤ ±1 LSB (max)**
- **10µs Settling Time to 0.5 LSB**
- **Low 3.5µA Shutdown Current**
- **10MHz SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- **Power-On Reset Sets DAC Output to 0V**
- **Schmitt Trigger Inputs for Direct Optocoupler Interface**
- **Serial-Data Output Allows Daisy Chaining of Devices**
- **Small 16-Pin SSOP**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5312EAE	-40°C to +85°C	16 SSOP

Pin Configuration



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MICROWIRE is a trademark of National Semiconductor Corp.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND.....-0.3V to +17V
V_{SS} to AGND .....-17V to +0.3V
V_{DD} to V_{SS} .....+34V
V_{CC} to DGND .....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
SGND to AGND.....-0.3V to +0.3V
SCLK, DIN, $\overline{CS}$, $\overline{SHDN}$, UNI/$\overline{BIP}$, $\overline{CLR}$, $\overline{LDAC}$, DOUT to DGND .....-0.3V to (V_{CC} + 0.3V)
OUT to AGND .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
REF to AGND.....-0.3V to +6V
Maximum Current into REF.....±10mA
Maximum Current into Any Pin Excluding REF.....±50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin SSOP (derate 7.1mW/°C above +70°C) 571mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (DUAL SUPPLY)

(V_{DD} = +15V ±5%, V_{SS} = -15V ±5%, V_{CC} = +5V ±10%, AGND = DGND = SGND = 0V, V_{REF} = 5V, R_{LOAD} = 2kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Zero-Scale Error		Bipolar, code = 800hex			±1	LSB
		Unipolar, code = 000hex			±2	
Zero-Scale Temperature Coefficient		Bipolar		0.3		ppm FSR/°C
		Unipolar		0.5		
Gain Error		Bipolar, no load			±2	LSB
		Unipolar, no load			±2	
Gain-Error Temperature Coefficient		Bipolar, no load		2		ppm FSR/°C
		Unipolar, no load		2		
ANALOG OUTPUT (OUT)						
Output Voltage Range		(V_{SS} + 1.5V) < V_{OUT} < (V_{DD} - 1.5V)	-2 x V_{REF}		+2 x V_{REF}	V
Resistive Load to GND	R_{LOAD}		2			kΩ
Capacitive Load to GND	C_{LOAD}				250	pF
DC Output Resistance				0.5		Ω
SGND INPUT (SGND)						
Input Impedance				92		kΩ
REFERENCE INPUT (REF)						
Reference-Voltage Input Range			2.00		5.25	V
Input Resistance	R_{REF}	Code = 555hex, worst-case code	15	22		kΩ
		Shutdown		22		
Reference Bandwidth		V_{REF} = 200mV_{P-P} + 5VDC		200		kHz

ELECTRICAL CHARACTERISTICS (DUAL SUPPLY) (continued)

(V_{DD} = +15V ±5%, V_{SS} = -15V ±5%, V_{CC} = +5V ±10%, AGND = DGND = SGND = 0V, V_{REF} = 5V, R_{LOAD} = 2kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{SHDN}$, UNI/$\overline{BIP}$, $\overline{CLR}$, $\overline{LDAC}$)						
Input-Voltage High	V_{IH}	+2.7V ≤ V_{CC} ≤ +3.6V	0.7 x V_{CC}			V
		+4.5V ≤ V_{CC} ≤ +5.5V	2.4			
Input-Voltage Low	V_{IL}	+2.7V ≤ V_{CC} ≤ +3.6V			0.6	V
		+4.5V ≤ V_{CC} ≤ +5.5V			0.8	
Input Capacitance	C	+2.7V ≤ V_{CC} ≤ +3.6V		10		pF
		+4.5V ≤ V_{CC} ≤ +5.5V		10		
Input Current (Note 1)		0 ≤ all digital inputs ≤ V_{CC}, +2.7V ≤ V_{CC} ≤ +3.6V			±1	µA
		0 ≤ all digital inputs ≤ V_{CC}, +4.5V ≤ V_{CC} ≤ +5.5V			±1	
DIGITAL OUTPUT (DOUT)						
Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{CC} - 0.5			V
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Tri-State Leakage Current				0.2		µA
Tri-State Capacitance				10		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate				2.5		V/µs
Output Settling Time		To ±0.5 LSB of full scale, code 000 to code FFF		10		µs
Digital Feedthrough		$\overline{CS}$ = high, f_{SCLK} = 10MHz, V_{OUT} = 0V		10		nV-s
Output-Noise Spectral Density at 10kHz				130		nV/√Hz
POWER SUPPLIES						
Positive Analog-Supply Voltage	V_{DD}		10.80		15.75	V
Negative Analog-Supply Voltage	V_{SS}		-10.80		-15.75	V
Positive Digital-Supply Voltage	V_{CC}		2.7		5.5	V
Positive Analog-Supply Current	I_{DD}	Output unloaded, V_{OUT} = FS		1.8	4	mA
Negative Analog-Supply Current	I_{SS}	Output unloaded, V_{OUT} = FS		0.75	-2	mA
Digital-Supply Current	I_{CC}	All digital inputs = 0 or V_{CC}		30	200	µA
Power-Supply Rejection Ratio (Note 2)	PSRR	Positive analog supply		0.4		LSB/V
		Negative analog supply		0.6		
Shutdown Current		Positive analog supply		1.7	50	µA
		Negative analog supply		2.4	50	
		Digital supply		3.5	10	

ELECTRICAL CHARACTERISTICS (SINGLE SUPPLY)

(V_{DD} = +15V ±5%, V_{SS} = 0V, V_{CC} = +5V ±10%, AGND = DGND = SGND = 0V, V_{REF} = 5V, R_{LOAD} = 10kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12			Bits
Integral Nonlinearity	INL	(Note 3)			±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Zero-Scale Error		Code = 14hex			±2	LSB
Unipolar Zero-Scale Temperature Coefficient		Code = 14hex		0.05		ppm FSR/°C
Gain Error		No load			±2	LSB
Gain-Error Temperature Coefficient		No load		2		ppm FSR/°C
ANALOG OUTPUT (OUT)						
Output Voltage Range			0		+2 x V_{REF}	V
Resistive Load to GND	R_{LOAD}		10			kΩ
Capacitive Load to GND	C_{LOAD}				250	pF
DC Output Resistance				0.5		Ω
SGND INPUT (SGND)						
Input Impedance				92		kΩ
REFERENCE INPUT (REF)						
Reference-Voltage Input Range			2.00		5.25	V
Input Resistance		Code = 555hex, worst-case code	15	22		kΩ
Reference Input Bandwidth		V_{REF} = 200mV_{P-P} + 5V_{DC}		150		kHz
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{SHDN}$, UNI/$\overline{BIP}$, $\overline{CLR}$, $\overline{LDAC}$)						
Input-Voltage High	V_{IH}	+2.7V ≤ V_{CC} ≤ +3.6V	0.7 x V_{CC}			V
		+4.5V ≤ V_{CC} ≤ +5.5V	2.4			
Input-Voltage Low	V_{IL}	+2.7V ≤ V_{CC} ≤ +3.6V			0.6	V
		+4.5V ≤ V_{CC} ≤ +5.5V			0.8	
Input Capacitance	C_{IN}	+2.7V ≤ V_{CC} ≤ +3.6V		10		pF
		+4.5V ≤ V_{CC} ≤ +5.6V		10		
Input Current	I_{IN}	0 ≤ V_{IN} ≤ V_{CC}, +2.7V ≤ V_{CC} ≤ +3.6V			±1	µA
		0 ≤ V_{IN} ≤ V_{CC}, +4.5V ≤ V_{CC} ≤ +5.5V			±1	
DIGITAL OUTPUT (DOUT)						
Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{CC} - 0.5			V
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Tri-State Leakage Current				0.2		µA

ELECTRICAL CHARACTERISTICS (SINGLE SUPPLY) (continued)

(V_{DD} = +15V ±5%, V_{SS} = 0V, V_{CC} = +5V ±10%, AGND = DGND = SGND = 0V, V_{REF} = 5V, R_{LOAD} = 10kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tri-State Capacitance				10		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate				2.5		V/µs
Output Settling Time		To ±0.5 LSB of full scale, code 14hex to code FFF		10		µs
Digital Feedthrough		$\overline{CS}$ = high, f_{SCLK} = 10MHz, V_{OUT} = 0V		10		nV-s
Output-Noise Spectral Density at 1kHz				130		nV/√Hz
POWER SUPPLIES						
Positive Analog-Supply Voltage	V_{DD}		10.80		15.75	V
Negative Analog-Supply Voltage	V_{SS}			0		V
Positive Digital-Supply Voltage	V_{CC}		2.7		5.5	V
Positive Analog-Supply Current	I_{DD}	Output unloaded, V_{OUT} = 0		1.8	4	mA
Negative Analog-Supply Current	I_{SS}	Output unloaded, V_{OUT} = 0		0.75	-2	mA
Digital-Supply Current	I_{CC}	All digital inputs = 0 or V_{CC}		30	200	µA
Power-Supply Rejection Ratio	PSRR	ΔV_{DD} = 14.5V to 15.5V, code FFF		0.04		LSB/V
Shutdown Current		Analog supply		1.7	50	µA
		Digital supply		3.5	10	

TIMING CHARACTERISTICS

(V_{DD} = +15V, V_{SS} = -15V or 0V, V_{CC} = +2.7V to +5.5V, AGND = DGND = SGND = 0, V_{REF} = 5V, R_{LOAD} = 2kΩ, C_{LOAD} = 250pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

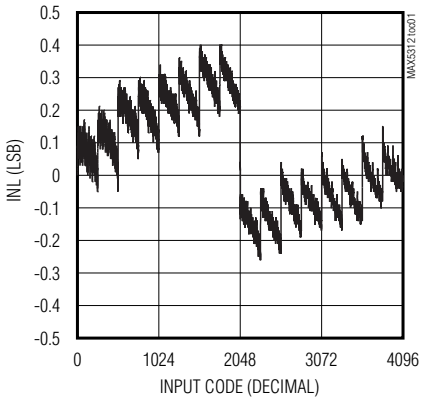
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency					10	MHz
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse-Width High	t_{CH}	For nondaisy-chain use	45			ns
SCLK Pulse-Width Low	t_{CL}	For nondaisy-chain use	45			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}	+2.7V ≤ V_{CC} ≤ +3.6V	15			ns
		+4.5V ≤ V_{CC} ≤ +5.5V	10			
DIN Setup Time	t_{DS}		20			ns
DIN Hold Time	t_{DH}		10			ns
$\overline{LDAC}$ Pulse Width	t_{LD}		50			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Low Setup Time	t_{LDS}	+2.7V ≤ V_{CC} ≤ +3.6V		100		ns
		+4.5V ≤ V_{CC} ≤ +5.5V		50		
SCLK Fall to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 20pF, +2.7V ≤ V_{CC} ≤ +3.6V			100	ns
		C_{LOAD} = 20pF, +4.5V ≤ V_{CC} ≤ +5.5V			80	
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}			10		ns
$\overline{CS}$ Low to DOUT Valid Time	t_{CSE}	C_{LOAD} = 20pF			120	ns
$\overline{CS}$ High to DOUT Disabled Time	t_{CSD}				120	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		50			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}	+2.7V ≤ V_{CC} ≤ +3.6V	200			ns
		+4.5V ≤ V_{CC} ≤ +5.5V	100			
$\overline{CLR}$ Pulse-Width Low	t_{CLR}			50		ns

Note 1: Output unloaded, digital inputs = V_{CC} or DGND.
Note 2: ΔV_{DD} = +14.5V to +15.5V, ΔV_{SS} = -15.5V to -14.5V, code = FFF.
Note 3: Measured from code 14hex to FFFhex.

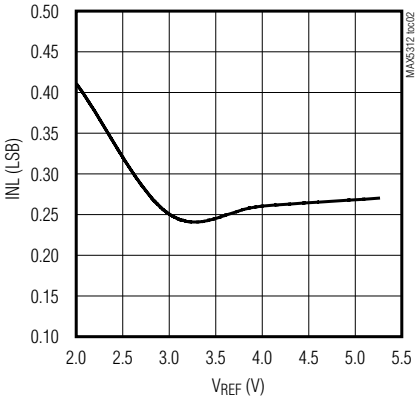
Typical Operating Characteristics

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND = 0, V_{REF} = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

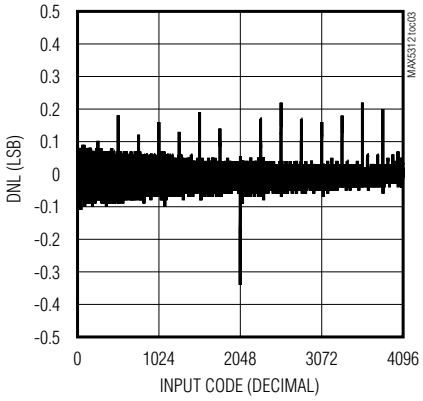
INTERGRAL NONLINEARITY vs. INPUT CODE



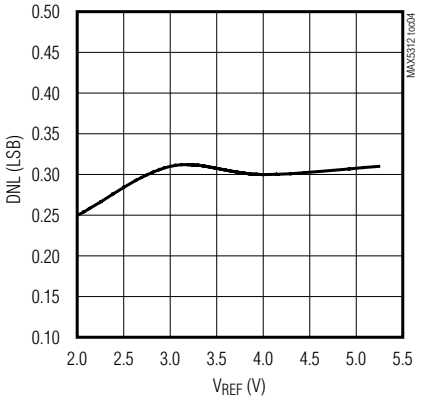
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



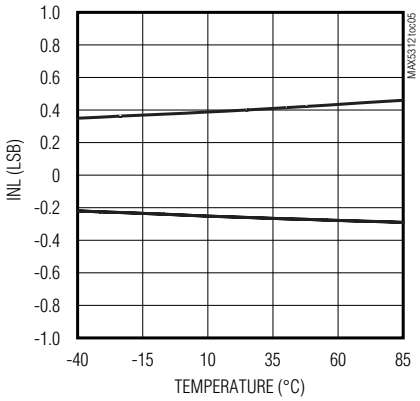
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



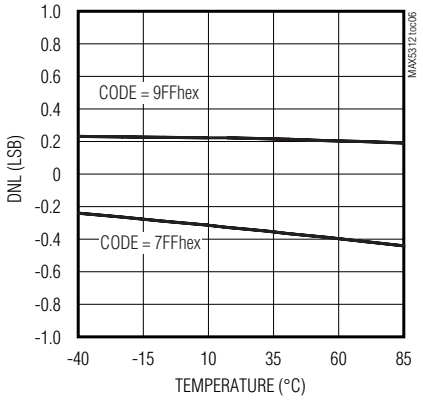
DIFFERENTIAL NONLINEARITY vs. REFERENCE VOLTAGE



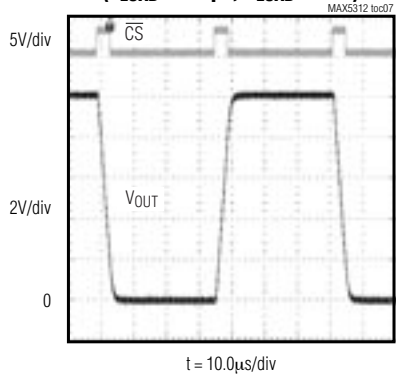
INTEGRAL NONLINEARITY vs. TEMPERATURE



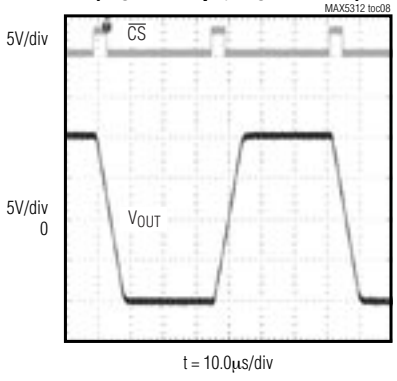
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE (WORST-CASE CODES)



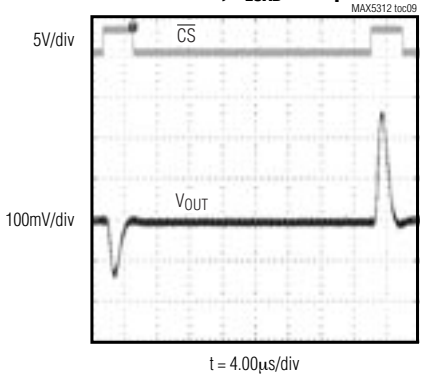
UNIPOLAR SETTLING TIME (C_{LOAD} = 250pF, R_{LOAD} = 2kΩ)



BIPOLAR SETTLING TIME (C_{LOAD} = 250pF, R_{LOAD} = 10kΩ)



BIPOLAR MAJOR CARRY GLITCH ENERGY, C_{LOAD} = 250pF

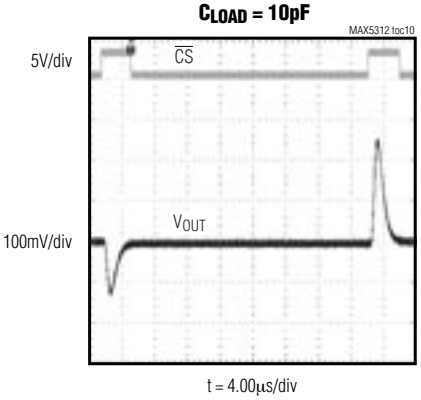


±10V, 12-Bit, Serial, Voltage-Output DAC

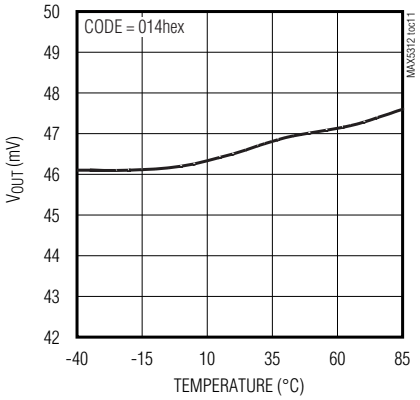
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND = 0, V_{REF} = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

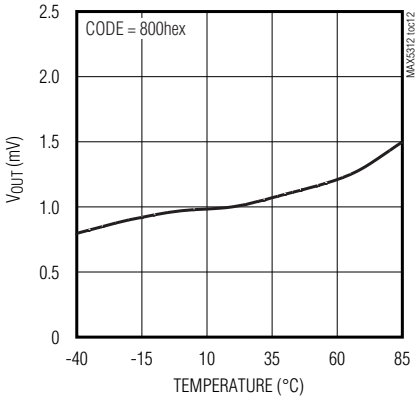
BIPOLAR MAJOR CARRY GLITCH
C_{LOAD} = 10pF



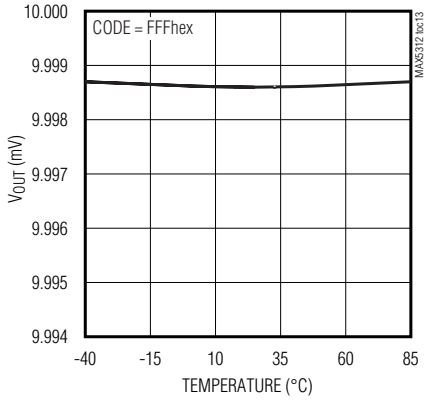
UNIPOLAR ZERO-SCALE VOLTAGE vs. TEMPERATURE



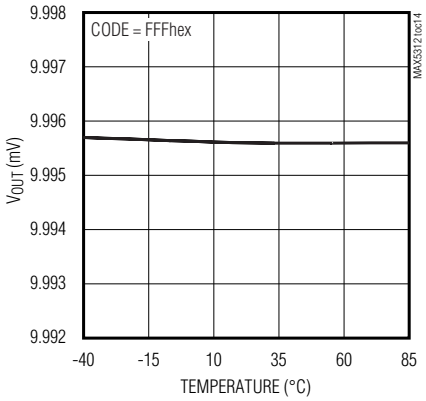
BIPOLAR MIDSCALE VOLTAGE vs. TEMPERATURE



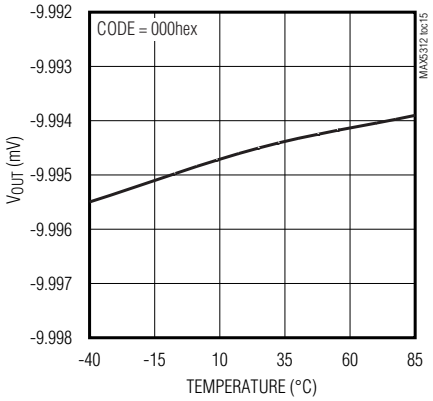
UNIPOLAR FULL-SCALE VOLTAGE vs. TEMPERATURE



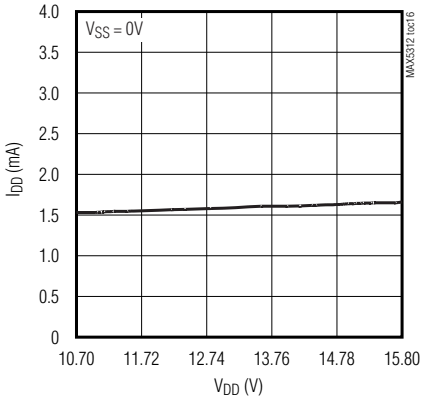
BIPOLAR POSITIVE FULL-SCALE VOLTAGE vs. TEMPERATURE



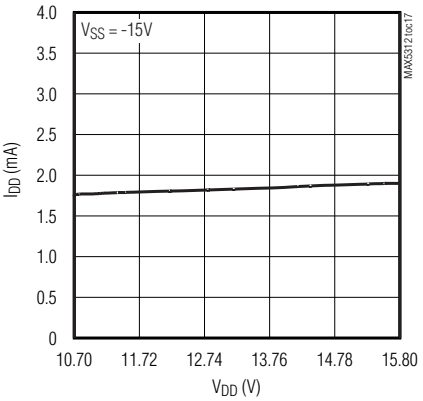
BIPOLAR NEGATIVE FULL-SCALE VOLTAGE vs. TEMPERATURE



UNIPOLAR SUPPLY CURRENT vs. SUPPLY VOLTAGE



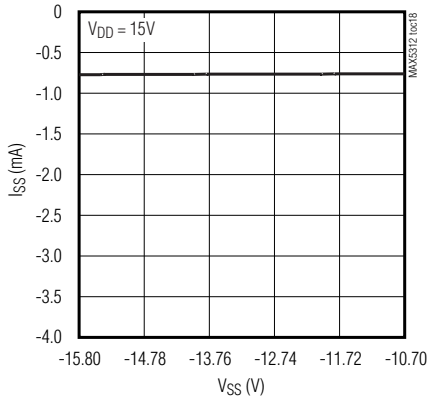
BIPOLAR POSITIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



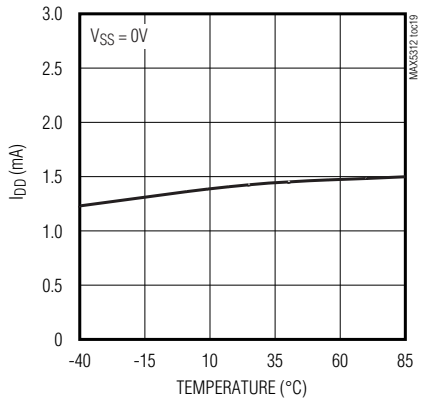
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND = 0, V_{REF} = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

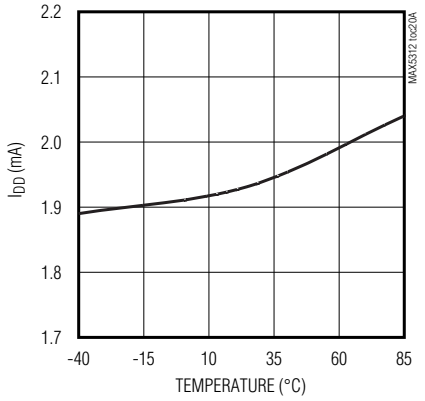
BIPOLAR NEGATIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



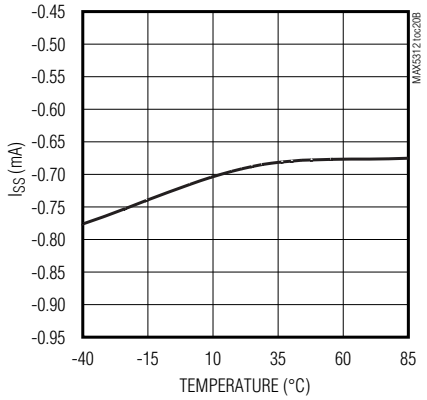
UNIPOLAR SUPPLY CURRENT vs. TEMPERATURE



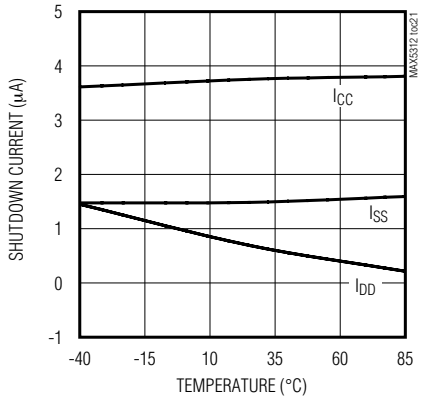
BIPOLAR POSITIVE SUPPLY CURRENT vs. TEMPERATURE



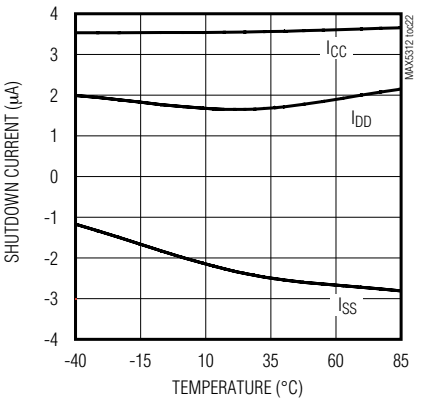
BIPOLAR NEGATIVE SUPPLY CURRENT vs. TEMPERATURE



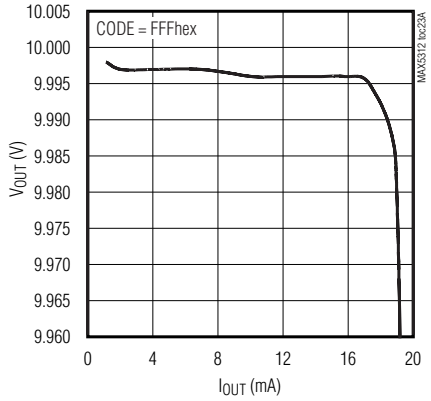
UNIPOLAR SHUTDOWN CURRENT vs. TEMPERATURE



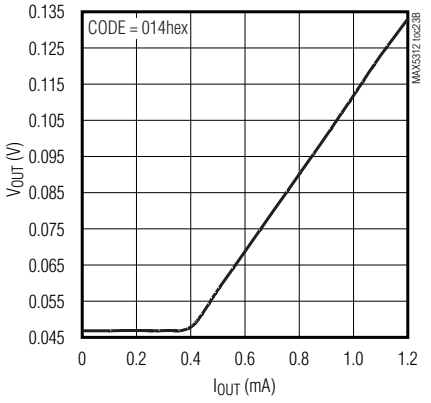
BIPOLAR SHUTDOWN CURRENT vs. TEMPERATURE



UNIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT



UNIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT

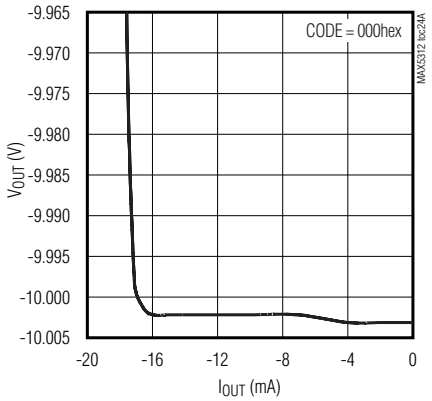


±10V, 12-Bit, Serial, Voltage-Output DAC

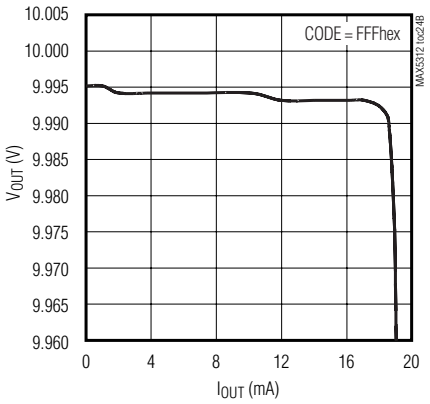
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND = 0, V_{REF} = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

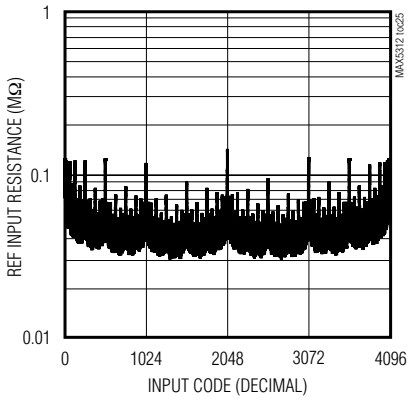
BIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT



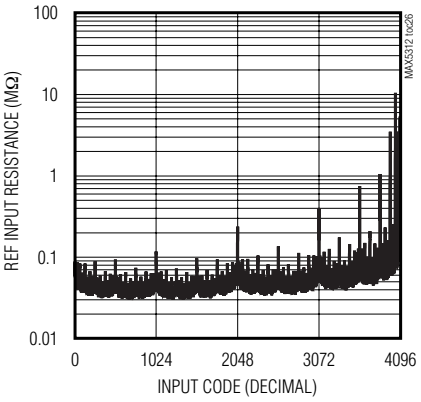
BIPOLAR OUTPUT VOLTAGE vs. OUTPUT CURRENT



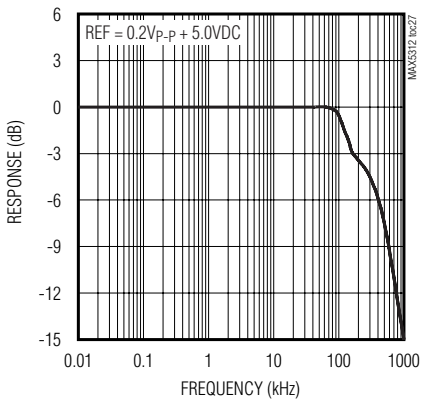
UNIPOLAR REF INPUT RESISTANCE vs. INPUT CODE



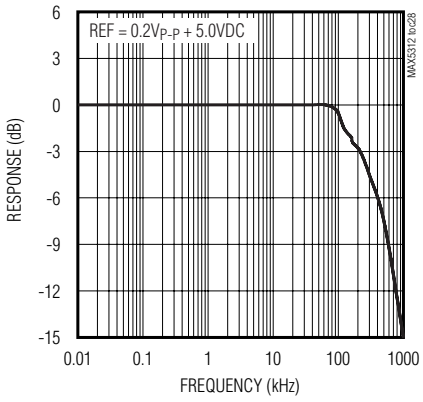
BIPOLAR REF INPUT RESISTANCE vs. INPUT CODE



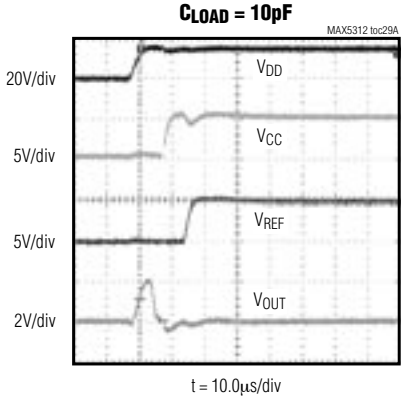
UNIPOLAR REFERENCE INPUT BANDWIDTH



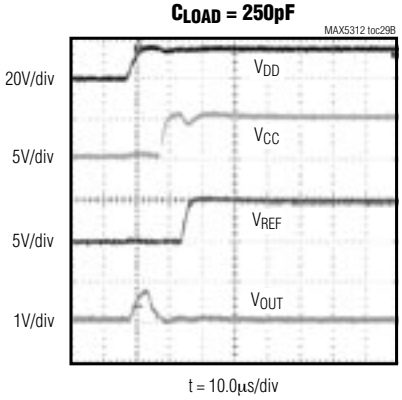
BIPOLAR REFERENCE INPUT BANDWIDTH



UNIPOLAR STARTUP RESPONSE, C_{LOAD} = 10pF



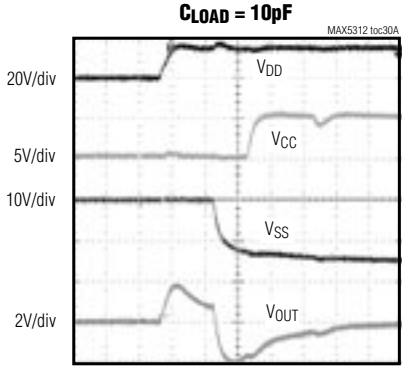
UNIPOLAR STARTUP RESPONSE, C_{LOAD} = 250pF



Typical Operating Characteristics (continued)

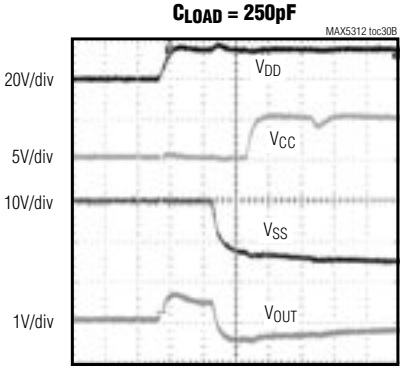
(V_{DD} = +15V, V_{SS} = -15V for bipolar graphs, V_{SS} = 0 for unipolar graphs, V_{CC} = +5V, AGND = DGND = SGND = 0, V_{REF} = +5.0V, output unloaded, T_A = +25°C, all graphs apply to both unipolar and bipolar, unless otherwise noted.)

BIPOLAR STARTUP RESPONSE, C_{LOAD} = 10pF



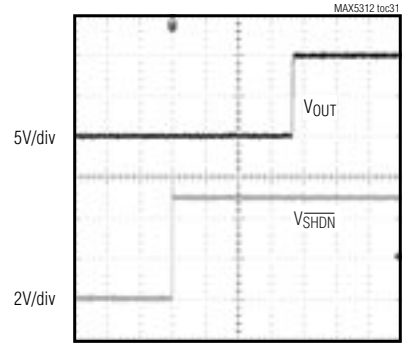
t = 10.0µs/div

BIPOLAR STARTUP RESPONSE, C_{LOAD} = 250pF



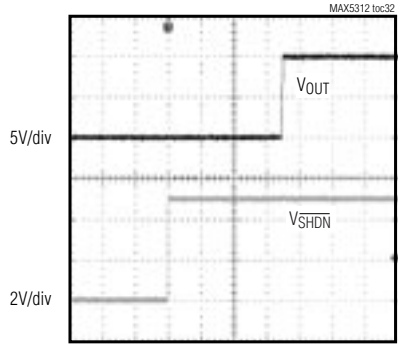
t = 10.0µs/div

UNIPOLAR RELEASE FROM HARDWARE-SHUTDOWN RESPONSE



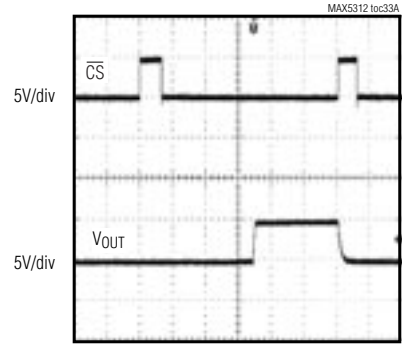
t = 100µs/div

BIPOLAR RELEASE FROM HARDWARE-SHUTDOWN RESPONSE



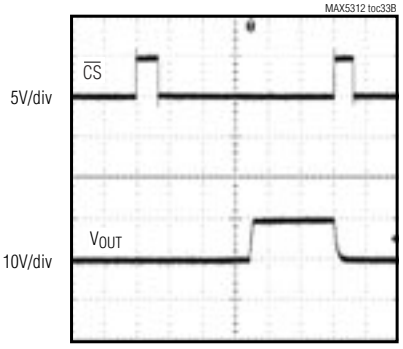
t = 100µs/div

UNIPOLAR SOFTWARE-SHUTDOWN RESPONSE



t = 40.0µs/div

BIPOLAR SOFTWARE-SHUTDOWN RESPONSE



t = 40.0µs/div

±10V, 12-Bit, Serial, Voltage-Output DAC

Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial-Clock Input. Data is shifted from DIN into the internal register on the rising edge of SCLK. Data is clocked out at DOUT on the falling edge of SCLK. SCLK is active only while $\overline{CS}$ is low.
2	DIN	Serial-Data Input. DIN is the data input port for the serial interface. Clock data in on the rising edge of SCLK.
3	$\overline{CS}$	Active-Low Chip-Select Input. $\overline{CS}$ activates the serial interface. Drive $\overline{CS}$ low to initiate serial communication.
4	DOUT	Serial-Data Output. DOUT is the data output port for the serial interface. Data shifted into DIN appears at DOUT 16.5 clock cycles later, valid on the falling edge of SCLK. DOUT is high impedance when $\overline{CS}$ is high.
5	DGND	Digital Ground
6	V_{CC}	Digital Power Input. V_{CC} ranges from +2.7V to +5.5V. Bypass V_{CC} with a 0.1µF and 1.0µF capacitor to
7	$\overline{SHDN}$	Active-Low Shutdown Input. $\overline{SHDN}$ places the device into low-power shutdown mode. When shut down REF and DOUT are high impedance, drive $\overline{SHDN}$ low to place the device into shutdown mode.
8	UNI/$\overline{BIP}$	Unipolar/Bipolar-Select Input. UNI/$\overline{BIP}$ selects unipolar or bipolar output. In unipolar mode, the analog output range is 0 to (+2 x V_{REF}). In bipolar mode, the analog output range is (-2 x V_{REF}) to (+2 x V_{REF}). Drive UNI/$\overline{BIP}$ high for unipolar output. Drive UNI/$\overline{BIP}$ low for bipolar output. Dual supplies are required for bipolar operation.
9	OUT	Analog Output. OUT is the output port for the DAC. Read OUT relative to SGND.
10	SGND	Signal Ground. SGND is the ground-reference node for the output amplifier's internal feedback resistors. Connect SGND directly to AGND. (See Figure 1.)
11	AGND	Analog Ground. AGND is the ground return for V_{DD} and V_{SS}.
12	V_{SS}	Negative Power Input. Bypass V_{SS} with a 0.1µF and 1.0µF capacitor to AGND. If operating with a single supply, connect V_{SS} to AGND.
13	REF	External Reference Input. Apply an external reference voltage of +2V to +5.25V to REF to determine the output voltage range. In unipolar mode, the output range is from 0 to (+2 x V_{REF}). In bipolar mode, the output range is from (-2 x V_{REF}) to (+2 x V_{REF}).
14	V_{DD}	Positive Power Input. Bypass V_{DD} with a 0.1µF and 1.0µF capacitor to AGND.
15	$\overline{CLR}$	Active-Low Clear Input. $\overline{CLR}$ clears input and DAC registers and resets the DAC output to 0V. Drive $\overline{CLR}$ low to assert the clear condition.
16	$\overline{LDAC}$	Active-Low Load Input. Use $\overline{LDAC}$ to update the DAC register. $\overline{LDAC}$ is an asynchronous control input. Drive low to force an update.

Detailed Description

The MAX5312 12-bit DAC operates from either single or dual supplies. Dual ±12V to ±15V power supplies provide a bipolar ±5V to ±10V output, or a unipolar 0 to 10V output. Single 12V to 15V power supplies provide only a unipolar 0 to 10V output. The reference input accepts voltages from 2V to 5.25V. The DAC features INL and DNL less than ±1 LSB (max), a fast 10µs settling time, and a hardware-shutdown mode that reduces current consumption to 3.5µA (max). The device features a 10MHz SPI-/QSPI-/MICROWIRE-compatible serial interface that operates with 3V or 5V logic, an asynchronous load input, and a serial-data output. The device offers a $\overline{CLR}$ that sets the DAC output to 0V. Figure 1 shows the functional diagram of the MAX5312.

Serial Interface

An SPI-/QSPI-/MICROWIRE-compatible serial interface allows complete control of the DAC through a 16-bit control word. The first 4 bits form the control bits that determine register loading and software-shutdown functions. The last 12 bits form the DAC data. The 16-bit word is entered MSB first.

Table 1 shows the serial-data format. Table 2 shows the interface commands.

The MAX5312 can be programmed while in shutdown.

The serial interface contains three registers: a 16-bit shift register, a 12-bit input register, and a 12-bit DAC register (Figure 1). The shift register accepts data from the serial interface. The input register acts as a holding register for data going to the DAC register and isolates the shift register from the DAC register. The DAC register controls the DAC ladder and thus the output voltage. Any update in the DAC register updates the output voltage.

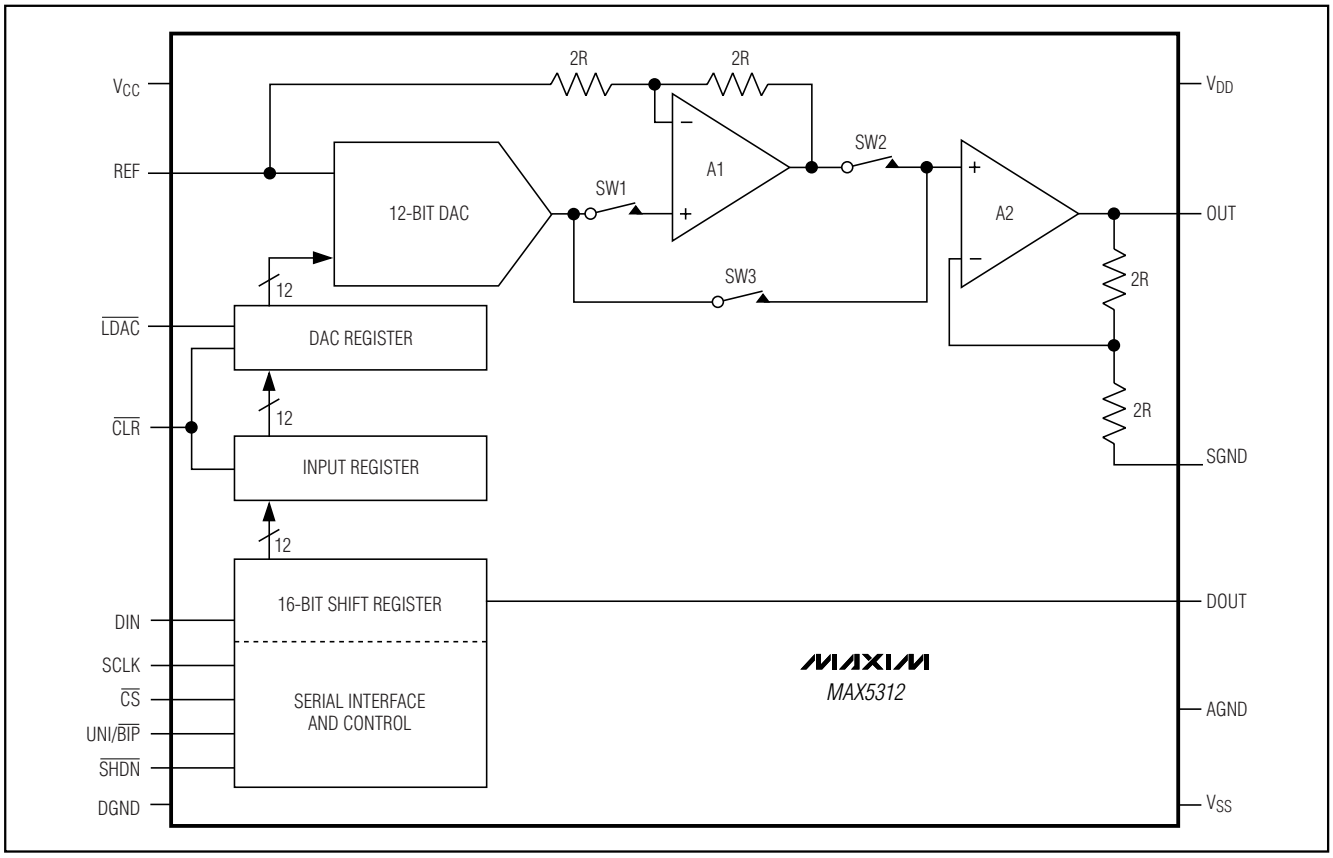


Figure 1. Functional Diagram

±10V, 12-Bit, Serial, Voltage-Output DAC

Data in the shift register is transferred to the input register during the appropriate software command only. Data in the input register is transferred to the DAC register in one of two ways: using the software command, or through external logic control using the asynchronous load input ($\overline{LDAC}$). Table 2 shows the software commands that transfer the data from the shift register to the input and/or DAC registers. The $\overline{CLR}$, an external logic control, asynchronously forces the input and DAC registers to zero code, and the output to 0V, in both unipolar and bipolar modes. The interface timing is shown in Figures 2 and 3.

Wait a minimum of 100ns after $\overline{CS}$ goes high before implementing $\overline{LDAC}$ or $\overline{CLR}$. If either of these logic inputs activates during a data transfer, the incoming data is corrupted and needs to be reloaded. For software control only, connect $\overline{LDAC}$ and $\overline{CLR}$ high.

DAC Architecture

The MAX5312 uses an inverted DAC ladder architecture to convert the digital input into an analog output voltage. The digital input controls weighted-switches that connect the DAC ladder nodes to either REF or GND (Figure 4). The sum of the weights produces the analog equivalent of the digital-input word and is then buffered at the output.

Table 1. Serial-Data Format

CONTROL BITS				DATA BITS											
MSB															LSB
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2. Serial-Interface Programming Commands

CONTROL BITS*				INPUT DATA	FUNCTION
C3	C2	C1	C0	D11–D0	
0	0	0	0	XXXXXXXXXXXX	No operation; command is ignored.
0	0	1	0	12-bit DAC data	Load input register from shift register; DAC output unchanged.
0	1	0	0	12-bit DAC data	Load input and DAC registers from shift register; DAC output updated.
0	1	1	0	XXXXXXXXXXXX	Load DAC register from input register; DAC output updated; input register unchanged.
1	0	0	0	XXXXXXXXXXXX	Enter shutdown; input and DAC registers unchanged.
1	1	0	0	XXXXXXXXXXXX	Exit shutdown; input and DAC registers unchanged.

X = *Don't care.*

**All unlisted commands are reserved commands. Do not use.*

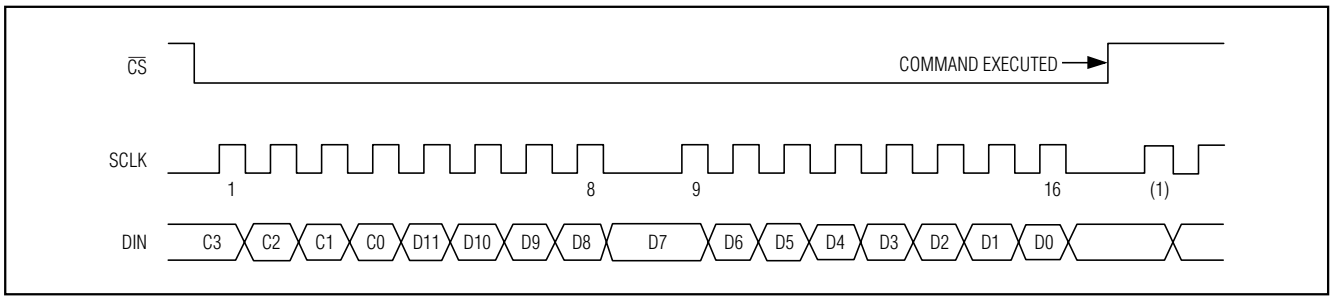


Figure 2. Serial-Interface Signals

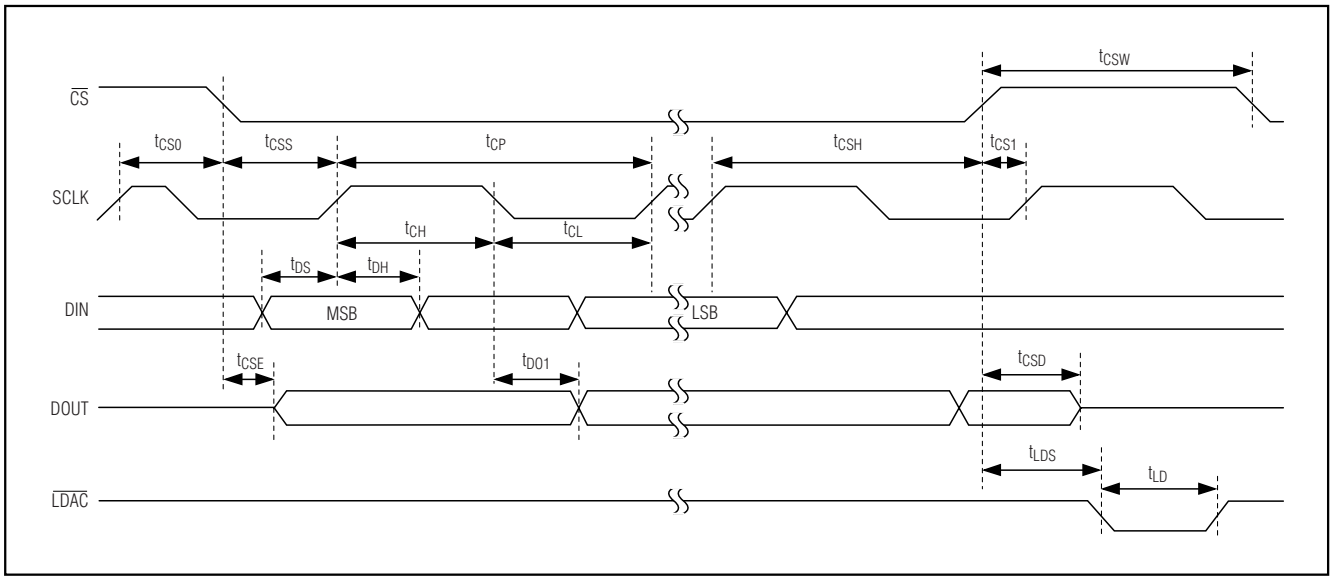


Figure 3. Serial-Interface Timing Diagram

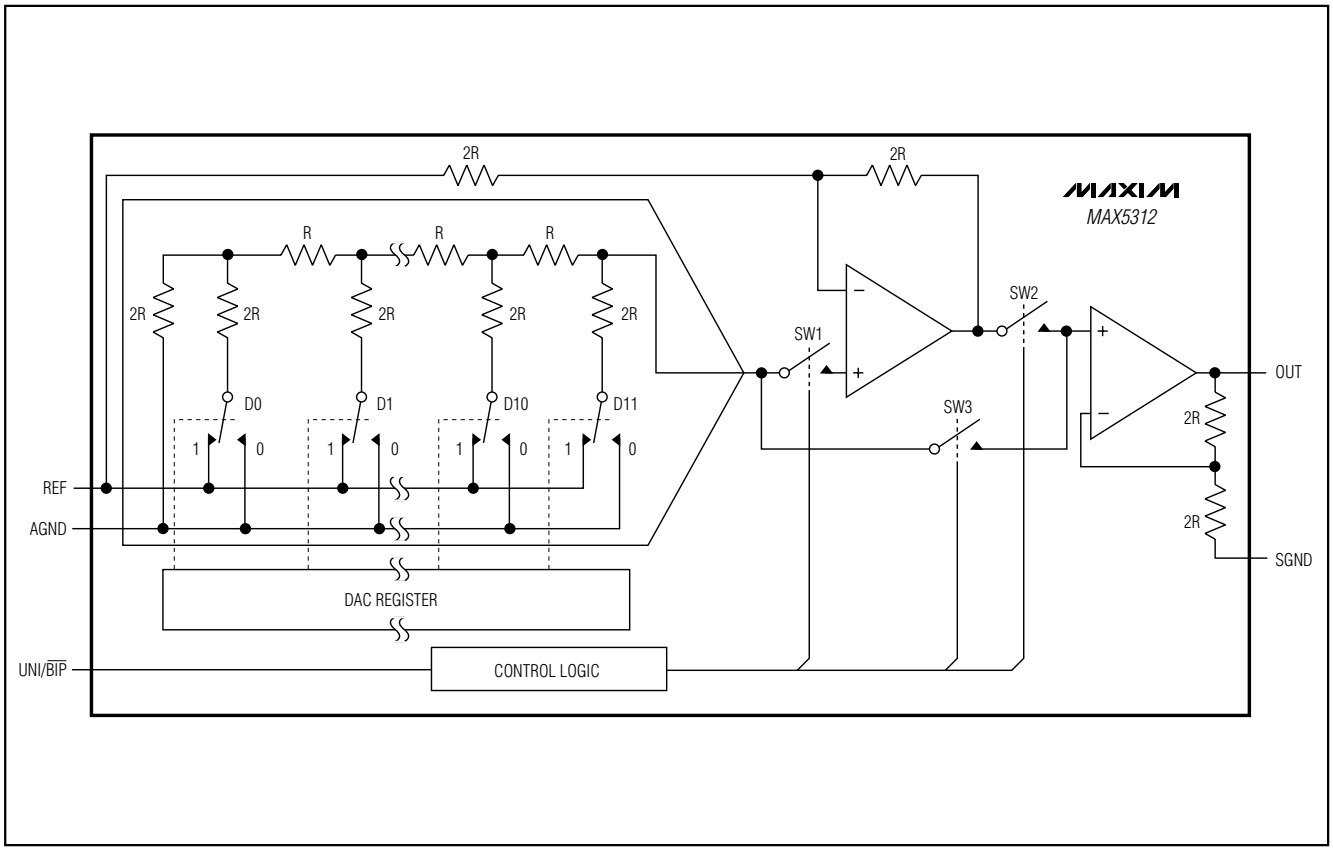


Figure 4. Basic Inverted DAC Ladder

External Reference and Transfer Functions

Connect an external 2V to 5.25V reference to REF (the MAX6350 is recommended). Set the output voltage range with the reference and the input code by using the equations below.

Unipolar Output Voltage:

$$V_{OUT\_UNI} = LSB_{UNI} \times CODE$$

where

$$LSB_{UNI} = \frac{2 \times V_{REF}}{2^{12}}$$

Bipolar Output Voltage:

$$V_{OUT\_BIP} = (LSB_{BIP} \times CODE) - (2 \times V_{REF})$$

where

$$LSB_{BIP} = \frac{4 \times V_{REF}}{2^{12}}$$

where V_{OUT_UNI} is the unipolar output voltage, V_{OUT_BIP} is the bipolar output voltage, LSB_{UNI} is the unipolar LSB step size, LSB_{BIP} is the bipolar LSB step size, V_{REF} is the reference voltage, and CODE is the decimal equivalent of the binary, 12-bit, DAC input code.

In either case, a 000hex input code produces the minimum output (-2 x V_{REF} for bipolar and 0 for unipolar), an 800hex input code produces the midscale output (0 for bipolar and V_{REF} for unipolar), and a FFFhex input code produces the full-scale output (2 x V_{REF} for bipolar and unipolar).

Output Amplifiers

The output-amplifier section can be configured as either unipolar or bipolar by the UNI/$\overline{BIP}$ logic input. With UNI/$\overline{BIP}$ forced low, SW1 and SW2 in Figure 4 are closed, and SW3 is open. This configuration channels the DAC output through two output stages to generate the ±2 x V_{REF} output swing. The first amplifier generates the ±V_{REF} voltage range and the second amplifier increases it by two. When configured for bipolar operation, the MAX5312 must be driven with dual ±12V to ±15V power supplies.

With UNI/$\overline{BIP}$ forced high, switches SW1 and SW2 are open, and SW3 is closed. This configuration channels the DAC output through only a single gain stage to generate a 0 to (2 x V_{REF}) output swing.

Daisy Chaining

SPI-/QSPI-/MICROWIRE-compatible devices can be daisy chained to reduce I/O lines from the host controller (Figure 7). Daisy chain devices by connecting the DOUT of one device to the DIN of the next, and connect the SCLK of all devices to a common clock. Data is shifted out of DOUT 16.5 clock cycles after it is shifted into DIN, and is available on the rising edge of the 17th clock cycle. The SPI-/QSPI-/MICROWIRE-compatible serial interface normally works at up to 10MHz, but must be slowed to 6.0MHz if daisy chaining. DOUT is high impedance when $\overline{CS}$ is high.

Shutdown

Shutdown is controlled by software commands or by the $\overline{SHDN}$ logic input. The $\overline{SHDN}$ logic input can be implemented at any time. The SPI-/QSPI-/MICROWIRE-compatible serial interface remains fully functional, and the device is programmable while shut down. When shut down, the MAX5312 supply current reduces to 3.5µA, DOUT is high impedance, and OUT is pulled to SGND through the internal feedback resistors of the output amplifier (Figure 1). When coming out of shutdown, or during device power-up, allow 350µs for the output to stabilize.

Table 3. Output Voltage as Input Code Examples

BINARY DAC CODE	ANALOG OUTPUT	
MSB LSB	UNIPOLAR (UNI/$\overline{BIP}$_ = HIGH)	BIPOLAR (UNI/$\overline{BIP}$_ = LOW)
1111 1111 1111	+2 x V_{REF} (4095 / 4096)	+2 x V_{REF} (2047 / 2048)
1000 0000 0001	+2 x V_{REF} (2049 / 4096)	+2 x V_{REF} (1 / 2048)
1000 0000 0000	+2 x V_{REF} (2048 / 4096) = V_{REF}	0
0111 1111 1111	+2 x V_{REF} (2047 / 4096)	-2 x V_{REF} (1 / 2048)
0000 0000 0001	+2 x V_{REF} (1 / 4096)	-2 x V_{REF} (2047 / 2048)
0000 0000 0000	0	-2 x V_{REF} (2048 / 2048) = -2 x V_{REF}

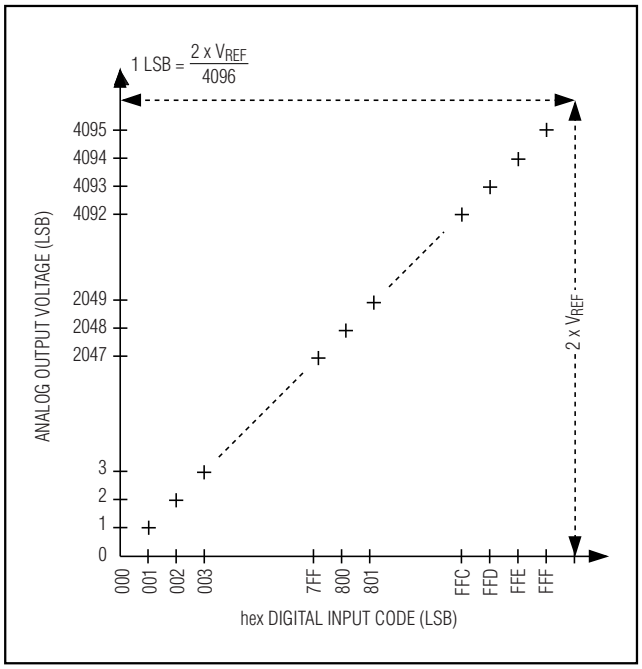


Figure 5. Unipolar Transfer Function

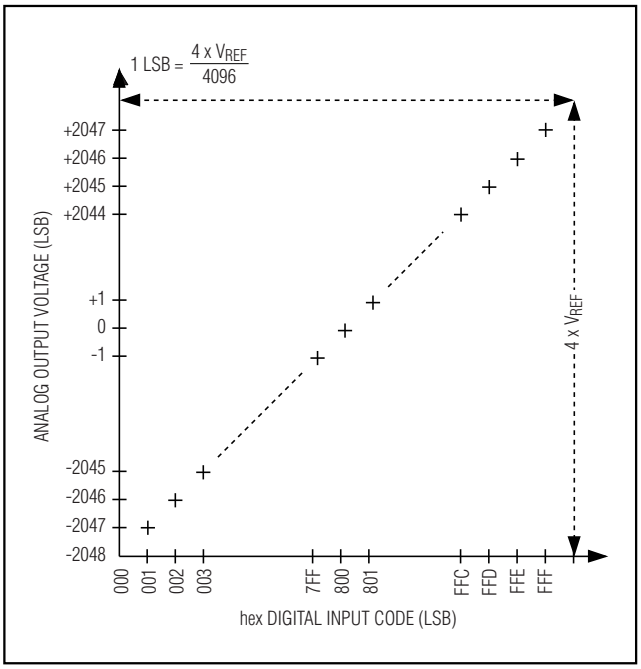


Figure 6. Bipolar Transfer Function

Applications Information

Power Supplies

A single +12V to +15V supply is required to realize a 0 to 10V output swing. A dual ±12V to ±15V supply is required to realize a ±10V output swing, and allows unipolar, 0 to +10V output if UNI/$\overline{BIP}$ is forced high. A +3V to +5V digital power supply and a +2.000V to +5.250V external reference voltage are also required. Always bring up the reference voltage last. The other power supplies do not require sequencing.

Power-Supply Bypassing and Ground Management

Bypass V_{DD} and V_{SS} with 0.1µF and 1.0µF capacitors to AGND, and bypass V_{CC} with 0.1µF and 1.0µF capacitors to DGND. Minimize trace lengths to reduce inductance. Digital and AC transient signals on AGND or DGND can create noise at the output. Connect AGND and DGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane or star connect all ground-return paths back to AGND. Carefully lay out the traces between channels to reduce AC crosscoupling and crosstalk. Wire-wrapped boards, sockets, and breadboards are not recommended.

±10V, 12-Bit, Serial, Voltage-Output DAC

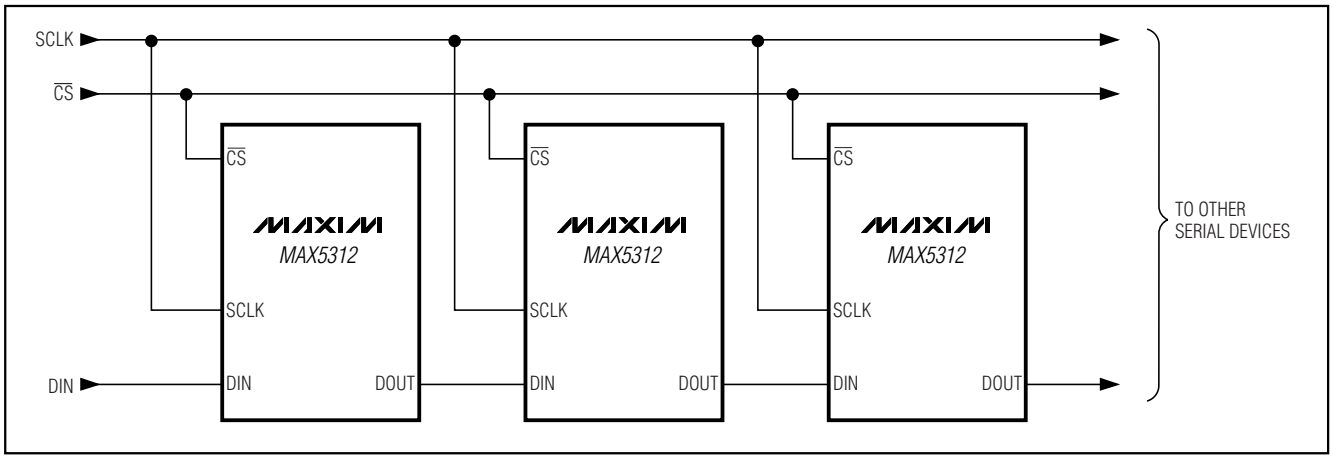


Figure 7. Daisy Chaining Devices

Chip Information

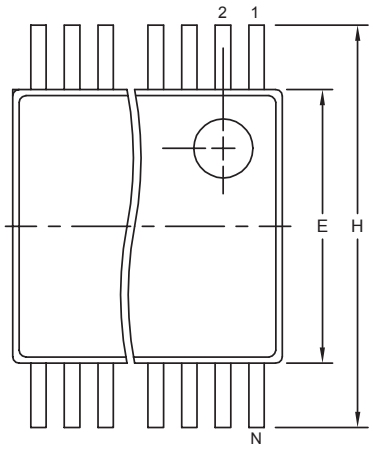
TRANSISTOR COUNT: 3280

TECHNOLOGY: BiCMOS

Package Information

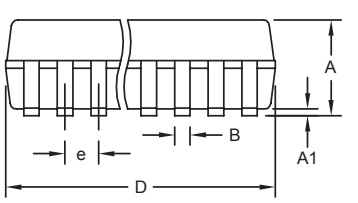
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

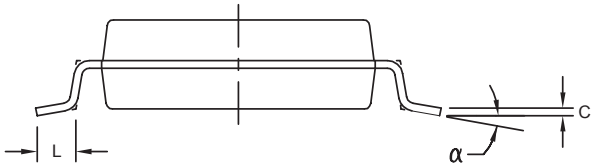
SSOP.EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SSOP, 5.3 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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