19-1469; Rev 0; 7/99

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

General Description

The MAX5165 contains four 1-to-8 multiplexers and 32 sample/hold amplifiers. A single analog input connects to all four internal 1-to-8 multiplexers. The sample/hold amplifiers are organized into four octal sample/holds with independent TTL/CMOS-compatible track/hold enables for each octal set. Additional 3-bit TTL/CMOS-compatible address logic selects the 1-to-8 multiplexer channel. Clamping diodes on each output allow clamping between two external reference voltages. The MAX5165 is available with an output impedance of 50Ω, 500Ω, or 1kΩ, allowing output filtering.

The MAX5165 operates with +10V and -5V supplies and a separate +5V digital logic supply. Manufactured with a proprietary BiCMOS process, it provides high accuracy, fast acquisition time, low droop rate, and a low hold step. The device acquires 8V step input signals to 0.01% accuracy in 2.5µs. Transitions from sample mode to hold mode result in only a 0.5mV error. While in hold mode, the output voltage slowly droops at a rate of 1mV/sec. The MAX5165 is available in a 48-pin TQFP package.

Applications

Automatic Test Equipment (ATE)

Industrial Process Controls

Arbitrary Function Generators

Avionics Equipment

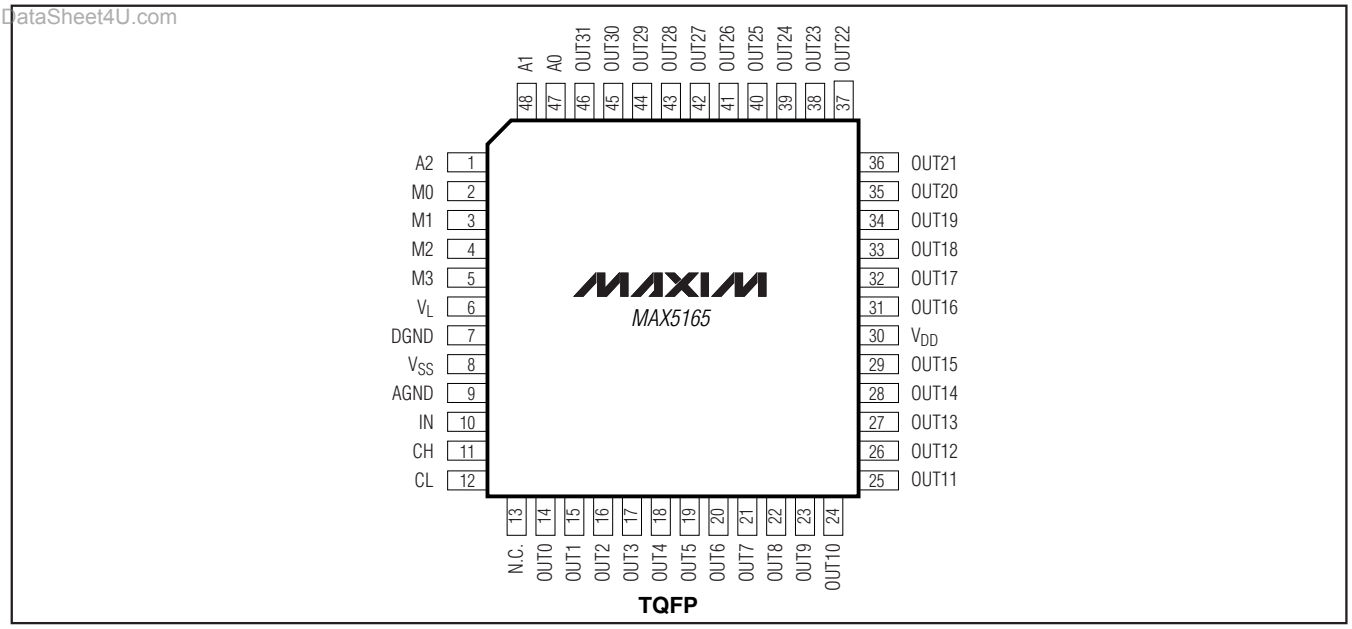
Features

- **32-Channel Sample/Hold**
- **Output Clamping**
- **0.01% Accuracy of Acquired Signal**
- **0.01% Linearity Error**
- **Fast Acquisition Time: 2.5µs**
- **Low Droop Rate: 1mV/sec**
- **Low Hold Step: 0.25mV**
- **Wide Output Voltage Range: +7V to -4V**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	R_{OUT} (Ω)
MAX5165LCCM	0°C to +70°C	48 TQFP	50
MAX5165MCCM	0°C to +70°C	48 TQFP	500
MAX5165NCCM	0°C to +70°C	48 TQFP	1k
MAX5165LECM	-40°C to +85°C	48 TQFP	50
MAX5165MECM	-40°C to +85°C	48 TQFP	500
MAX5165NECM	-40°C to +85°C	48 TQFP	1k

Pin Configuration



TQFP

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +11.0V
V_{SS} to AGND .....-6.0V to +0.3V
V_{DD} to V_{SS} .....+15.75V
VL to DGND .....-0.3V to +6.0V
VL to AGND .....-0.3V to +6.0V
DGND to AGND .....-0.3V to +2.0V
IN to AGND .....V_{SS} to V_{DD}
A_, M_ to DGND .....-0.3V to +6.0V
CH, CL to AGND .....-6.0V to +11.0V
Maximum Current into Output Pin .....±10mA
Maximum Current into A_, M_ .....±20mA
Continuous Power Dissipation (T_A = +70°C)
48-pin TQFP (derate 12.5mW/°C above +70°C).....1000mW
Operating Temperature Ranges
MAX5165_CCM .....0°C to +70°C
MAX5165_ECM.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C
Maximum Current into CH, CL, PIN.....±80mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +10V, V_{SS} = -5V, V_L = +5V ±5%, AGND = DGND, R_L = 5kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SECTION							
Linearity Error		-4V < V_{IN} < +7V, R_L = ∞			0.01	0.08	%
Hold Step	V_{HS}	IN = AGND			0.25	1.00	mV
Droop Rate	$\Delta V_{OUT\_}$	IN = AGND, T_A = +25°C			1	40	mV/sec
Offset Voltage	V_{OS}	IN = AGND, T_A = +25°C		-30	-5	30	mV
		+15°C ≤ T_A ≤ +65°C (Note 1)			20	40	µV/°C
Output Voltage Range	$V_{OUT\_}$	R_L = ∞		V_{SS} + 0.75		V_{DD} - 2.4	V
Analog Crosstalk		8V step with 500ns rising edge (Note 1)	MAX5165L, C_L = 250pF	-72	-76		dB
			MAX5165M, C_L = 10nF	-72	-76		
			MAX5165N, C_L = 10nF	-72	-76		
Input Capacitance	C_{IN}				10	20	pF
DC Output Impedance	$R_{OUT\_}$	R_L = ∞, C_L = 250pF	MAX5165L	35	50	65	Ω
			MAX5165M	350	500	650	
			MAX5165N	700	1000	1300	
Output Source Current	I_{SOURCE}			2			mA
Output Sink Current	I_{SINK}			2			mA
Output Clamp High	V_{CH}			V_{SS}		V_{DD}	V
Output Clamp Low	V_{CL}			V_{SS}		V_{DD}	V
TIMING PERFORMANCE							
Acquisition Time	t_{AQ}	8V step to 0.08%, R_L = ∞, Figure 2 (Note 2)			2.5	4	µs
		T_A = +25°C, 100mV step to ±1mV, R_L = ∞, Figure 2 (Note 2)			1		
Hold-Mode Settling Time	t_H	To ±1mV of final value, Figure 2 (Note 1)			1	2	µs
Aperture Delay	t_{AP}	Figure 2 (Note 1)				200	ns
Inhibit Pulse Width	t_{PW}	Figure 2 (Note 1)		200			ns
Data Hold Time	t_{DH}	Figure 2 (Note 1)		150			ns
Data Setup Time	t_{DS}	Figure 2 (Note 1)		50			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +10V, V_{SS} = -5V, V_L = +5V ±5%, AGND = DGND, R_L = 5kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.8	V
Input Current	I_I	A_ = DGND or V_L, M_ = DGND or V_L	-1		+1	µA
POWER SUPPLIES						
Positive Analog Supply Voltage	V_{DD}	(Note 3)	9.5	10	10.5	V
Negative Analog Supply Voltage	V_{SS}	(Note 3)	-4.75	-5.0	-5.45	V
Digital Logic Supply Voltage	V_L		4.75	5	5.25	V
Positive Analog Supply Current	I_{DD}	R_L = ∞			36	mA
Negative Analog Supply Current	I_{SS}	R_L = ∞			36	mA
Digital Logic Supply Current	I_L	A0–A3 = DGND or V_L; M0, M1, M2 = DGND or V_{CC}			0.5	mA
Digital Logic Supply Current	I_L	A0–A3 = 0.8V or 2V; M0, M1, M2 = 0.8V or 2V			5	mA
Power-Supply Rejection Ratio	PSRR	For both V_{DD} and V_{SS} in sample mode, V_{IN} = 0	-60	-75		dB

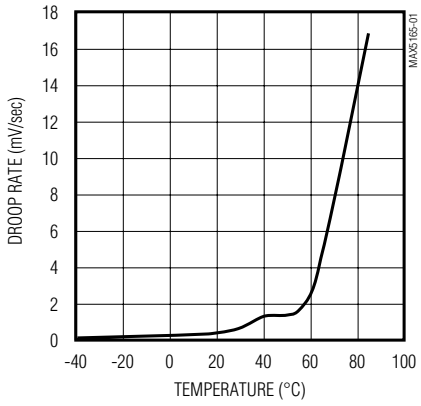
Note 1: Guaranteed by design.
Note 2: Only one M_ input may be asserted low at a time, so only one channel is selected (see *Single vs. Simultaneous Sampling*).
Note 3: Do not exceed the absolute maximum rating for V_{DD} to V_{SS} of +15.75V (see *Absolute Maximum Ratings*).

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

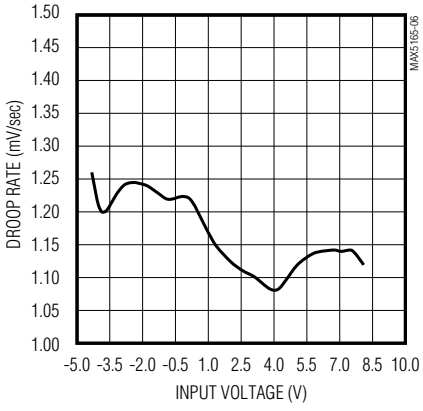
Typical Operating Characteristics

(V_{DD} = +10V, V_{SS} = -5V, V_L = +5V, IN = GND, R_L = ∞, C_L = 0, AGND = DGND, V_{CH} = V_{DD}, V_{CL} = V_{SS}, T_A = +25°C, unless otherwise noted.)

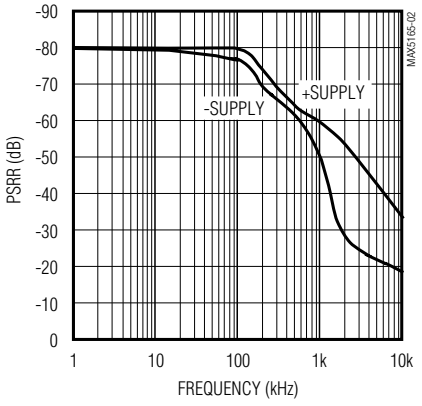
DROOP RATE vs. TEMPERATURE



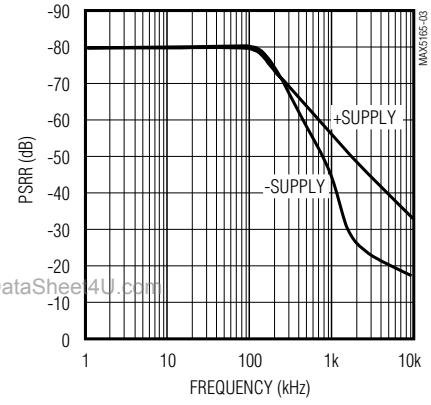
DROOP RATE vs. INPUT VOLTAGE



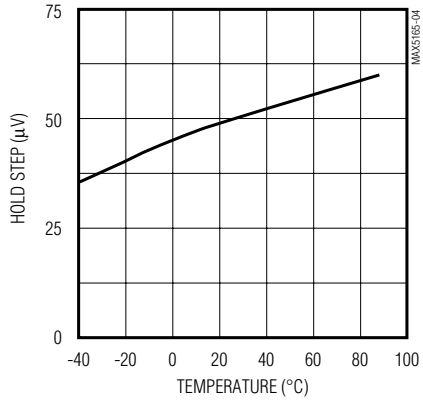
POWER-SUPPLY REJECTION RATIO (HOLD MODE)



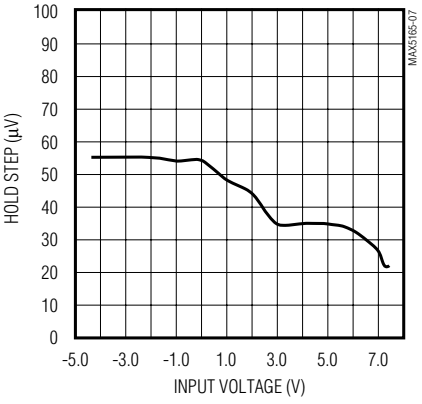
POWER-SUPPLY REJECTION RATIO (SAMPLE MODE)



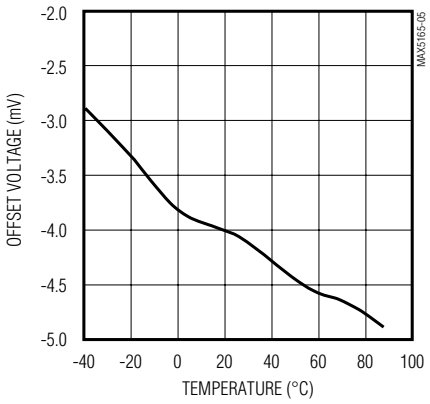
HOLD STEP vs. TEMPERATURE



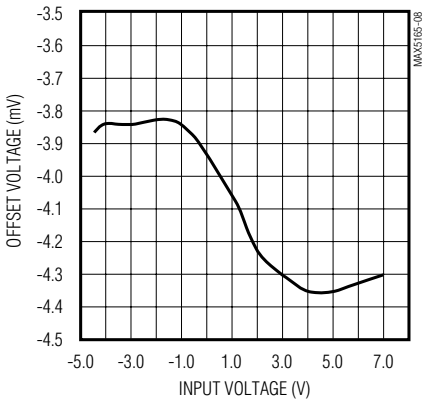
HOLD STEP vs. INPUT VOLTAGE



OFFSET VOLTAGE vs. TEMPERATURE



OFFSET VOLTAGE vs. INPUT VOLTAGE



32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

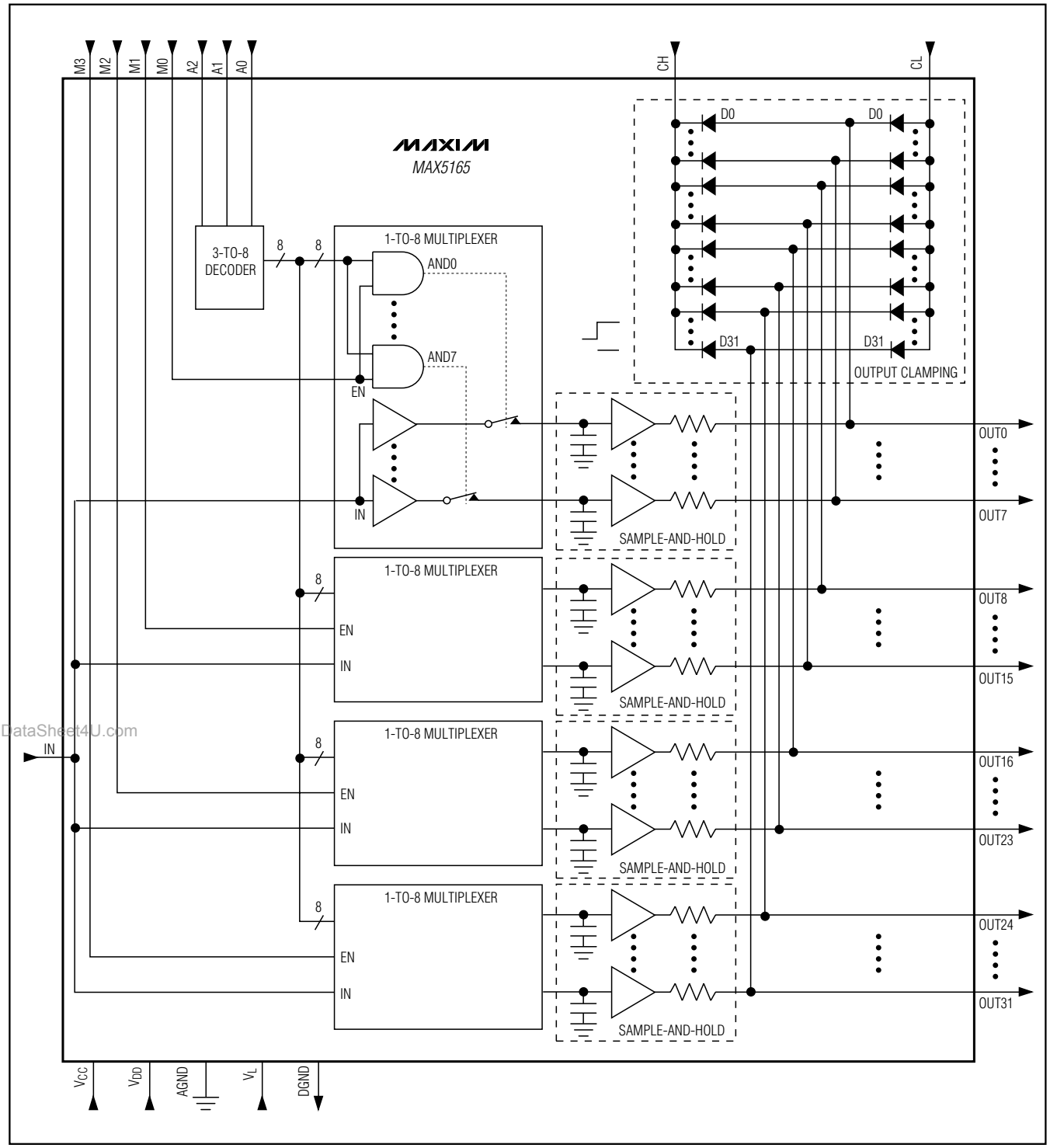


Figure 1. Functional Diagram

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

Pin Description

PIN	NAME	FUNCTION
1, 47, 48	A2, A0, A1	Address Inputs. The input of a 3-to-8 decoder, which controls channel selection for all four 1-to-8 multiplexers simultaneously. Selects which output channels are connected to the input during sample mode (Tables 1, 2).
2–5	M0–M3	Mode-Selection/Multiplexer-Enable Inputs 0 to 3. Independent controls for each of the four 1-to-8 multiplexers. A logic low enables sample mode by connecting the selected channel (via address inputs A2, A1, A0) to IN. A logic high selects hold mode (Tables 1, 2).
6	VL	Positive Digital Logic Power-Supply Input
7	DGND	Digital Ground
8	V_{SS}	Negative Analog Power-Supply Input
9	AGND	Analog Ground
10	IN	Analog Input. Connects to the input of all four internal 1-to-8 multiplexers.
11	CH	Clamp High Input. Clamps V_{OUT} to (V_{CH} + 0.7V).
12	CL	Clamp Low Input. Clamps V_{OUT} to (V_{CL} - 0.7V).
13	N.C.	No Connection. Not internally connected.
14–29	OUT0–OUT15	Sample/Hold Outputs 0 to 15
30	V_{DD}	Positive Analog Power-Supply Input
31–46	OUT16–OUT31	Sample/Hold Outputs 16 to 31

Detailed Description

The MAX5165 connects a single analog input to the inputs of four internal 1-to-8 analog multiplexers. Each multiplexer channel connects to a buffered sample/hold circuit and a series output resistor, creating a single-input device with 32 sample/hold output channels. Three multiplexer channel-address inputs and four mode-select inputs (one for each multiplexer) control channel selection and sample/hold functions (Figure 1 and Tables 1, 2).

Digital Interface

Three address pins and 3-to-8 address decoder logic select the channel for all four internal analog multiplexers. The mode-select inputs (M3–M0) independently control the sample/hold functions for each multiplexer (Tables 1, 2).

Sample/Hold

The MAX5165 contains 32 buffered sample/hold circuits with internal hold capacitors. Internal hold capacitors minimize leakage current, dielectric absorption, feedthrough, and required board space. The value of the hold capacitor affects acquisition time and droop rate. Lower capacitance allows faster acquisition times but increases the droop rate. Higher values increase hold time and acquisition time. The hold capacitor used in the MAX5165 provides fast 2.5µs (typ) acquisition time while maintaining a low 1mV/sec (typ) droop rate, making the sample/hold ideal for high-speed sampling.

Table 1. Output Selection

ADDRESS			OUTPUT SELECTED			
A2	A1	A0	MUX0	MUX1	MUX2	MUX3
0	0	0	OUT0	OUT8	OUT16	OUT24
0	0	1	OUT1	OUT9	OUT17	OUT25
0	1	0	OUT2	OUT10	OUT18	OUT26
0	1	1	OUT3	OUT11	OUT19	OUT27
1	0	0	OUT4	OUT12	OUT20	OUT28
1	0	1	OUT5	OUT13	OUT21	OUT29
1	1	0	OUT6	OUT14	OUT22	OUT30
1	1	1	OUT7	OUT15	OUT23	OUT31

0 = Logic Low, 1 = Logic High

Table 2. Mode Selection

MODE-SELECT INPUTS (M3–M0)	ACTION
0	Sample mode enabled on selected analog multiplexer and channel (Table 1).
1	Hold mode enabled on selected analog multiplexer and channel (Table 1).

0 = Logic Low, 1 = Logic High
** Only one M_ input asserted low; all others must be logic high to meet the timing specification (see Single vs. Simultaneous Sampling section).*

Sample Mode

Driving M3–M0 low (one at a time) selects sample mode (Tables 1, 2). During sample mode, the selected multiplexer channel connects to IN, allowing the hold capacitor to acquire the input signal. To guarantee an accurate sample, maintain sample mode for at least 4µs. The output of the S/H amplifier tracks the input after 4µs. Only the addressed channel on the selected multiplexer samples the input; all other channels remain in hold mode.

Hold Mode

Driving M3–M0 high selects hold mode. Hold mode disables the multiplexer and disconnects all eight channels on the 1-to-8 multiplexer from the input. When a channel is disconnected, the hold capacitor maintains the sampled voltage at the output with a 1mV/sec droop rate (towards V_{DD}).

Hold Step

When switching between sample mode and hold mode, the voltage of the hold capacitor changes due to charge injection from stray capacitance. This voltage change, called hold step, is minimized by limiting the amount of stray capacitance seen by the hold capacitor. The MAX5165 limits the hold step to 0.25mV (typ). An output capacitor to ground can be used to filter out this small hold-step error.

Output

The MAX5165 contains an output buffer for each multiplexer channel (32 total), so the hold capacitor sees a high-impedance input, reducing the droop rate. The capacitor droops at a 1mV/sec (typ) rate while in hold mode. The buffer also provides a low output impedance; however, the device contains output resistors in series with the buffer output (Figure 1) for selected output filtering. To provide greater design flexibility, the MAX5165 is available with an R_O of 50Ω, 500Ω, or 1kΩ.

Note: Output loads increase the analog supply current (I_{DD} and I_{SS}). Excessive loading of the output(s) damages the device by consuming more power than the device will dissipate (see *Absolute Maximum Ratings*). The resistor-divider formed by the output resistor (R_{OUT}) and load impedance (R_L) scales the sampled voltage (V_{SAMP}). Determine the output voltage ($V_{OUT\_}$) as follows:

$$\text{Voltage Gain} = A_V = R_L / (R_L + R_{OUT})$$

$$V_{OUT\_} = V_{SAMP} \cdot A_V$$

The maximum output voltage range depends on the analog supply voltages available, and the scaling factor used:

$$(V_{SS} + 0.75V) \cdot A_V \le V_{OUT\_} \le (V_{DD} - 2.4V) \cdot A_V$$

when $R_L = \infty$, then $A_V = 1$ and this equation becomes:

$$(V_{SS} + 0.75V) \le V_{OUT} \le (V_{DD} - 2.4V)$$

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

Output Clamp

The MAX5165 clamps the output between two externally applied reference voltages. Internal diodes connect all outputs to the clamping voltages, restricting the output voltage to:

$$V_{CH} + 0.7V \le V_{OUT\_} \le V_{CL} - 0.7V$$

When the clamping voltage exceeds the maximum output voltage, the maximum output voltage will be the limiting factor. To disable output clamping, connect CH to V_{DD} and C_L to V_{SS} to set the clamping voltages beyond the maximum output voltage range. The clamping diodes allow the MAX5165 to be used with other devices requiring restricted input voltages.

Timing Definitions

Acquisition time (t_{AQ}) is the amount of time the MAX5165 must remain in sample mode for the hold capacitor to acquire an accurate sample. The hold-mode settling time (t_H) is the amount of time necessary for the output voltage to settle to its final value. Aperture delay (t_{AP}) is the time interval required to disconnect the input from the hold capacitor. The inhibit pulse width (t_{PW}) is the amount of time the MAX5165 must remain in hold mode while the address is changed. The data setup time (t_{DS}) is the amount of time an address must be maintained before the address becomes valid. The data hold time (t_{DH}) is the amount of time that an address must be maintained after mode select has gone from low to high (Figure 2).

Applications Information

Control-Line Reduction

The MAX5165 contains four separate 1-to-8 multiplexers and individual mode selectors for each multiplexer. Configure the device to sample only one channel at a time or up to four channels (with the same address, see Table 1) simultaneously. When sampling one channel at a time, use an external 2-to-4 decoder (with active-low outputs) to reduce the number of digital control lines from seven to five (Figure 3).

Single vs. Simultaneous Sampling

Individually control the four mode/multiplexer-select pins to simultaneously sample on four channels, the same channel for each multiplexer (Figure 4). Each mode-select pin controls sampling on one of the 1-to-8 multiplexers, while the 3-bit address selects one of the eight channels on all the multiplexers (Tables 1, 2). Setting any combination of the mode-select pins low enables sampling on the addressed channels for the selected multiplexers.

Simultaneously sampling two or more channels reduces offset voltage but increases acquisition time. Multiply the single-channel acquisition time by the number of channels sampling.

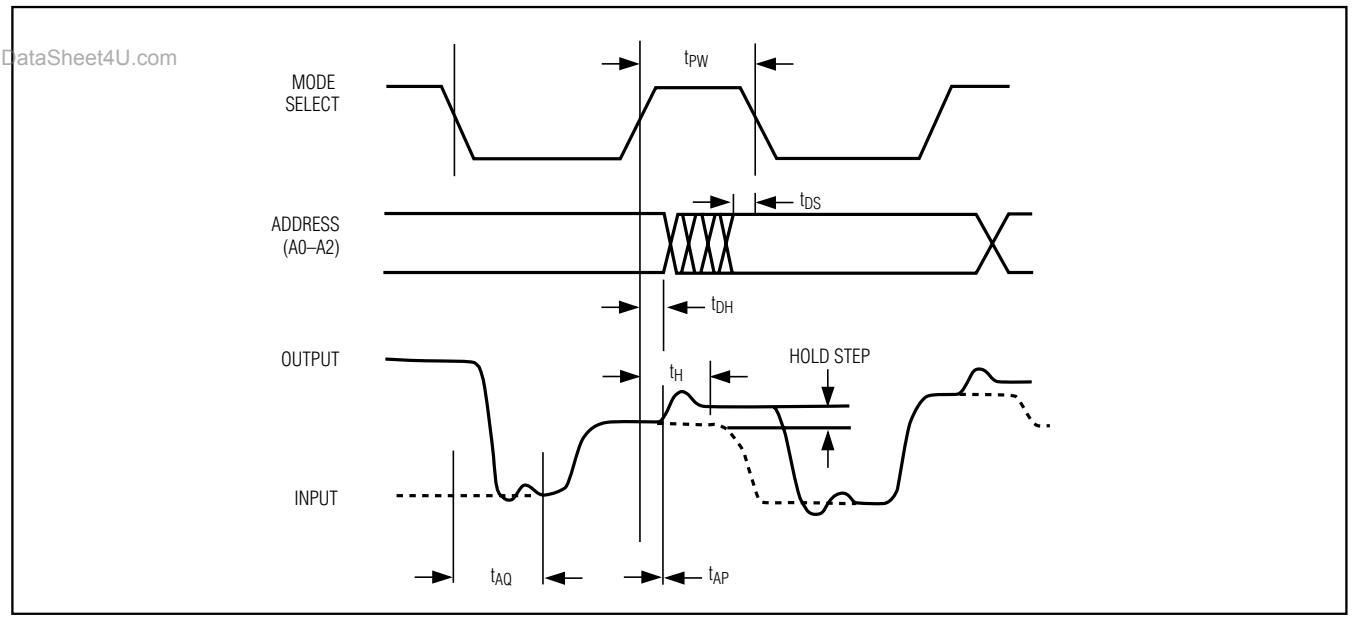


Figure 2. Timing Performance

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

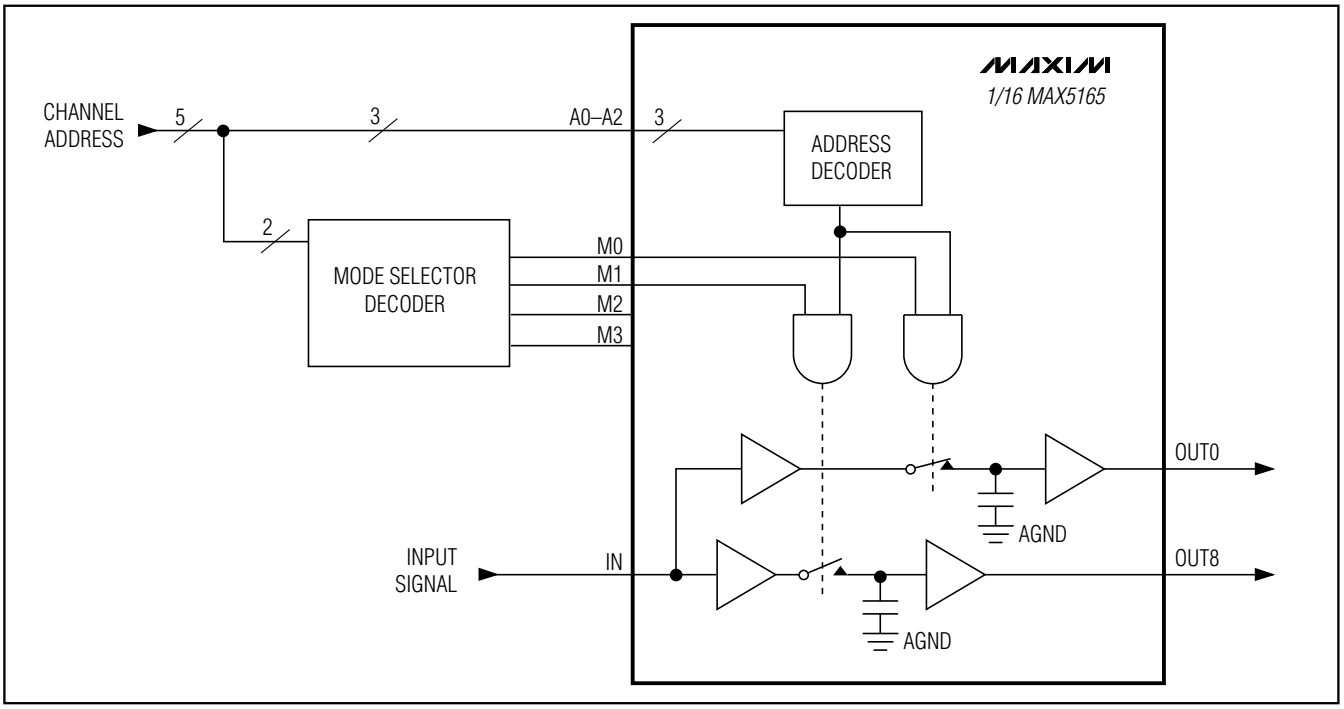


Figure 3. Control-Line Reduction

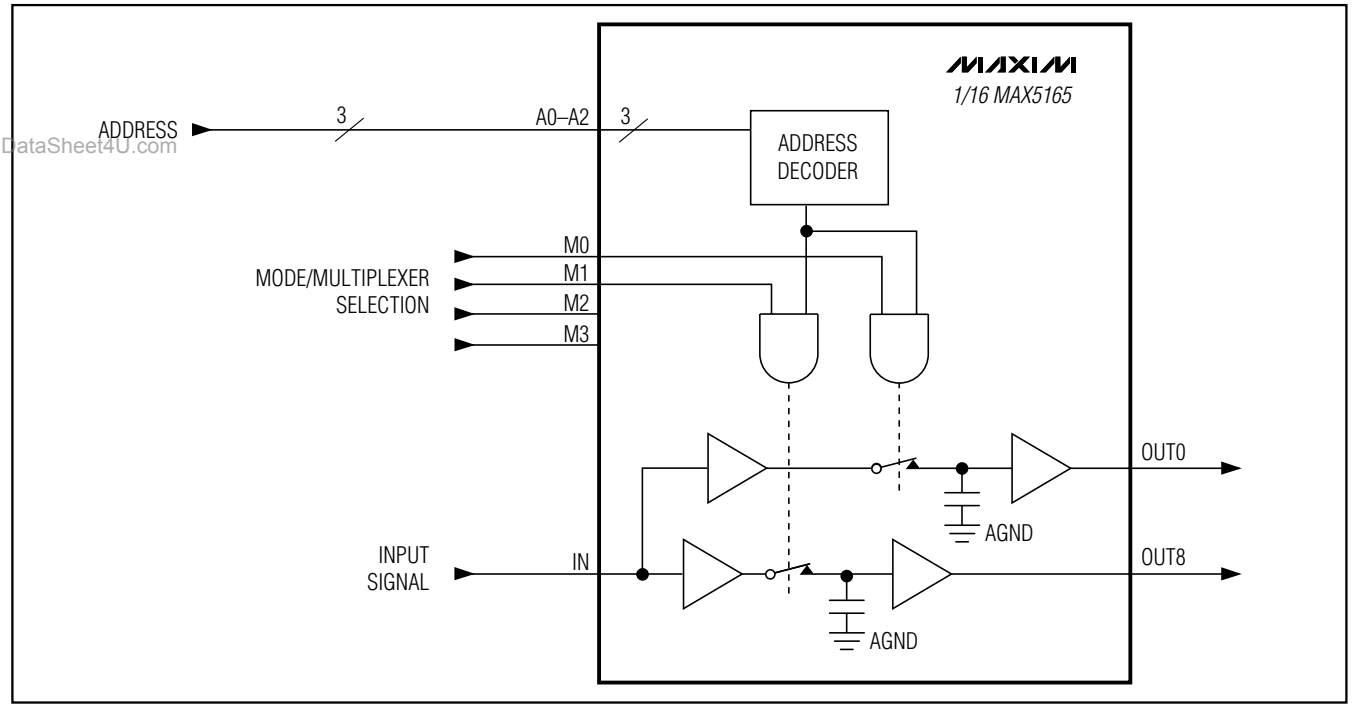


Figure 4. Simultaneous Sampling

32-Channel Sample/Hold Amplifier with a Single Multiplexed Input

Multiplexed DAC

Figure 5 shows a typical demultiplexer application. Different digital codes are converted by the digital-to-analog converter (DAC) and then stored on 32 different channels of the MAX5165. The 100mV/sec (max) droop rate requires refreshing the hold capacitors every 100ms before the voltage drops by 1/2LSB for an 8-bit DAC with a 5V full-scale voltage.

Powering the MAX5165

The MAX5165 does not require a special power-up sequence to avoid latchup. The device requires three separate supply voltages for operation; however, when one or two of the voltages are not available, DC-DC charge-pump (switched-capacitor) converters provide a simple, efficient solution. The MAX860 provides voltage doubling or inversion, ideal for conversions from +5V to +10V or from +5V to -5V. The MAX860 also functions as a voltage divider to provide conversion from +10V to +5V.

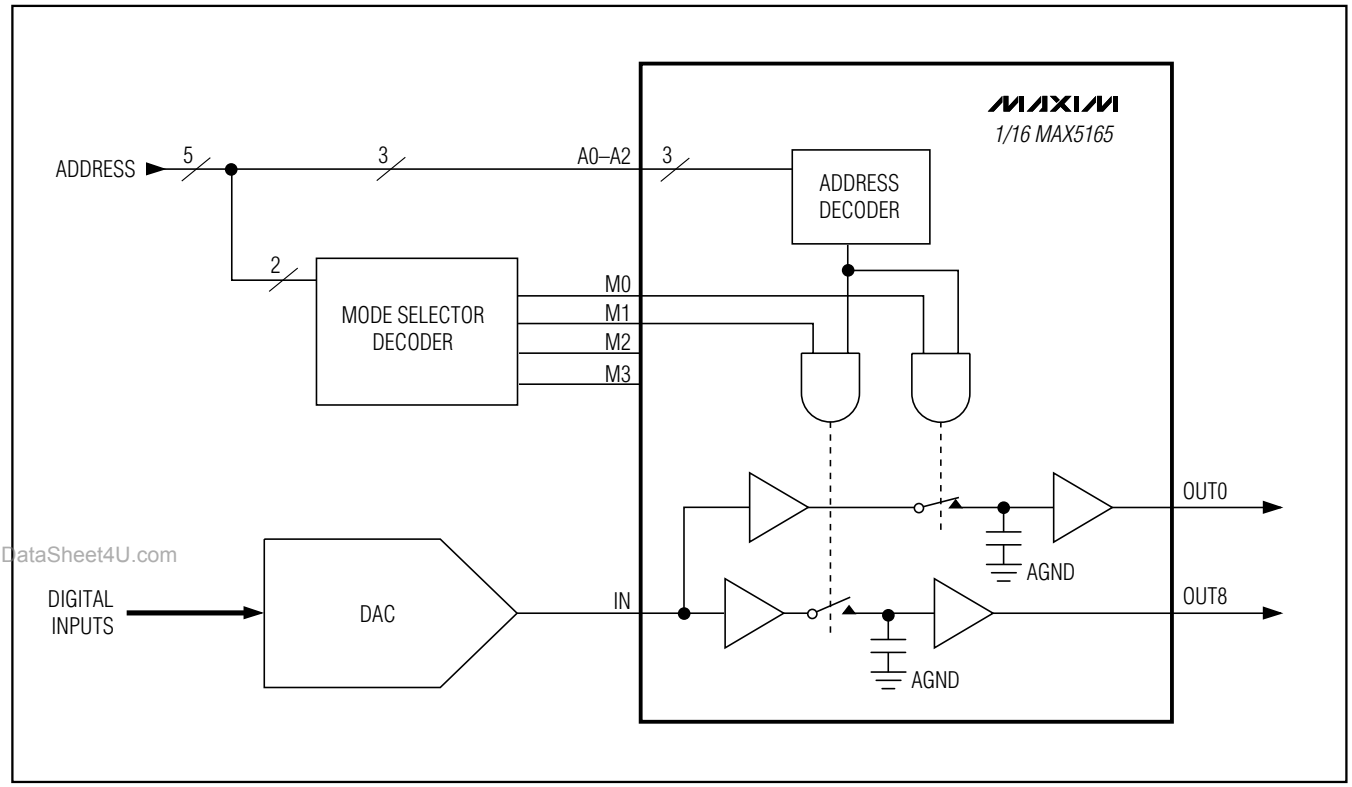


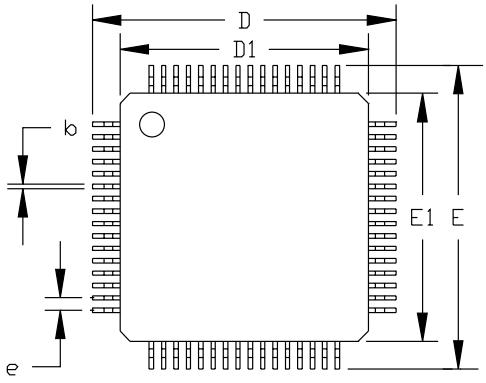
Figure 5. Multiplexing a DAC

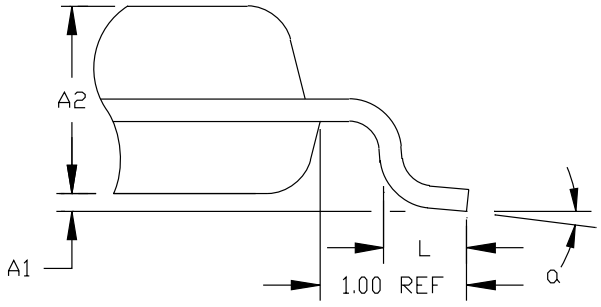
Chip Information

TRANSISTOR COUNT: 5077

Package Information

TQFPPO.EPS





JEDEC VARIATION						
	BC		BE		BJ	
	32 LEAD		48 LEAD		64 LEAD	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00 BSC.	
D_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
E	8.90	9.10	8.90	9.10	12.00 BSC.	
E_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
e	0.8 BSC.		0.5 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC, BE AND BJ.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	C	1/1

NOTES