19-3348; Rev 0; 8/04



# 4A, 20ns, Dual MOSFET Drivers



## General Description

The MAX5054–MAX5057 dual, high-speed MOSFET drivers source and sink up to 4A peak current. These devices feature a fast 20ns propagation delay and 20ns rise and fall times while driving a 5000pF capacitive load. Propagation delay time is minimized and matched between the inverting and noninverting inputs and between channels. High sourcing/sinking peak currents, low propagation delay, and thermally enhanced packages make the MAX5054–MAX5057 ideal for high-frequency and high-power circuits.

The MAX5054–MAX5057 operate from a 4V to 15V single power supply and consume 40µA (typ) of supply current when not switching. These devices have internal logic circuitry that prevents shoot-through during output state changes to minimize the operating current at high switching frequency. The logic inputs are protected against voltage spikes up to +18V, regardless of the $V_{DD}$ voltage. The MAX5054A is the only version that has CMOS input logic levels while the MAX5054B/MAX5055/MAX5056/MAX5057 have TTL input logic levels.

The MAX5055–MAX5057 provide the combination of dual inverting, dual noninverting, and inverting/noninverting input drivers. The MAX5054 feature both inverting and noninverting inputs per driver for greater flexibility. They are available in 8-pin TDFN (3mm x 3mm), standard SO, and thermally enhanced SO packages. These devices operate over the automotive temperature range of -40°C to +125°C.

## Applications

Power MOSFET Switching

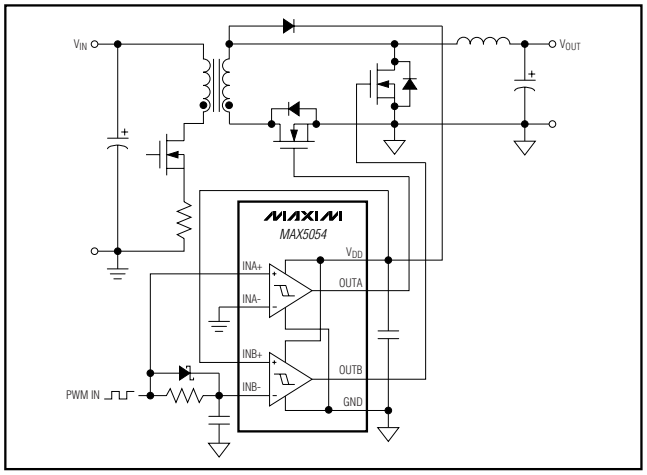
Motor Control

Switch-Mode Power Supplies

Power-Supply Modules

DC-DC Converters

## Typical Operating Circuit




## Features

- **4V to 15V Single Power Supply**
- **4A Peak Source/Sink Drive Current**
- **20ns (typ) Propagation Delay**
- **Matching Delay Between Inverting and Noninverting Inputs**
- **Matching Propagation Delay Between Two Channels**
- **$V_{DD}$ / 2 CMOS Logic Inputs (MAX5054AATA)**
- **TTL Logic Inputs (MAX5054B/MAX5055/MAX5056/MAX5057)**
- **0.1 x $V_{DD}$ (CMOS) and 0.3V (TTL) Logic-Input Hysteresis**
- **Up to +18V Logic Inputs (Regardless of $V_{DD}$ Voltage)**
- **Low Input Capacitance: 2.5pF (typ)**
- **40µA (typ) Quiescent Current**
- **-40°C to +125°C Operating Temperature Range**
- **8-Pin TDFN and SO Packages**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|---|---|---|---|
| **MAX5054**AATA | -40°C to +125°C | 8 TDFN-EP* | AGS |
| MAX5054BATA | -40°C to +125°C | 8 TDFN-EP* | AGR |
| **MAX5055**AASA | -40°C to +125°C | 8 SO-EP* | — |
| MAX5055BASA | -40°C to +125°C | 8 SO | — |
| **MAX5056**AASA | -40°C to +125°C | 8 SO-EP* | — |
| MAX5056BASA | -40°C to +125°C | 8 SO | — |
| **MAX5057**AASA | -40°C to +125°C | 8 SO-EP* | — |
| MAX5057BASA | -40°C to +125°C | 8 SO | — |

*EP = Exposed pad. Package code S8E-14.

***Selector Guide and Pin Configurations appear at end of data sheet.***

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
$V_{DD}$.....-0.3V to +18V
INA+, INA-, INB+, INB- .....-0.3V to +18V
OUTA, OUTB.....-0.3V to ($V_{DD}$ + 0.3V)
OUTA, OUTB Short-Circuit Duration .....10ms
Continuous Source/Sink Current at OUT_ ($P_D < P_{DMAX}$).....200mA
Continuous Power Dissipation ($T_A$ = +70°C)
8-Pin TDFN-EP (derate 24.4mW/°C above +70°C).....1951mW
Junction-to-Case Thermal Resistance ($\theta_{JC}$) .....2°C/W
8-Pin SO-EP (derate 19.2mW/°C above +70°C)… .....1538mW
Junction-to-Case Thermal Resistance ($\theta_{JC}$) .....6°C/W
8-Pin SO (derate 5.9mW/°C above +70°C)… .....471mW
Junction-to-Case Thermal Resistance ($\theta_{JC}$) .....40°C/W
Operating Temperature Range.....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s).....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 4V to 15V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{DD}$ = 15V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| $V_{DD}$ Operating Range | $V_{DD}$ | | | 4 | | 15 | V |
| $V_{DD}$ Undervoltage Lockout | UVLO | $V_{DD}$ rising | | 3.00 | 3.50 | 3.85 | V |
| $V_{DD}$ Undervoltage Lockout Hysteresis | | | | | 200 | | mV |
| $V_{DD}$ Undervoltage Lockout to Output Delay | | $V_{DD}$ rising | | | 12 | | µs |
| $V_{DD}$ Supply Current | $I_{DD}$ | INA- = INB- = $V_{DD}$, INA+ = INB+ = 0V (not switching) | $V_{DD}$ = 4V | | 28 | 55 | µA |
| | | | $V_{DD}$ = 15V | | 40 | 75 | |
| | $I_{DD-SW}$ | INA- = 0V, INB+ = $V_{DD}$ = 15V, INA+ = INB- both channels switching at 250kHz, $C_L$ = 0 | | 1 | 2.4 | 4 | mA |
| **DRIVER OUTPUT (SINK)** | | | | | | | |
| Driver Output Resistance Pulling Down | $R_{ON-N}$ | $V_{DD}$ = 15V, $I_{OUT\_}$ = -100mA | $T_A$ = +25°C | | 1.1 | 1.8 | Ω |
| | | | $T_A$ = +125°C | | 1.5 | 2.4 | |
| | | $V_{DD}$ = 4.5V, $I_{OUT\_}$ = -100mA | $T_A$ = +25°C | | 2.2 | 3.3 | |
| | | | $T_A$ = +125°C | | 3.0 | 4.5 | |
| Peak Output Current (Sinking) | $I_{PK-N}$ | $V_{DD}$ = 15V, $C_L$ = 10,000pF | | | 4 | | A |
| Output-Voltage Low | | $I_{OUT\_}$ = -100mA | $V_{DD}$ = 4.5V | | | 0.45 | V |
| | | | $V_{DD}$ = 15V | | | 0.24 | |
| Latchup Protection | $I_{LUP}$ | Reverse current $I_{OUT\_}$ (Note 2) | | 400 | | | mA |
| **DRIVER OUTPUT (SOURCE)** | | | | | | | |
| Driver Output Resistance Pulling Up | $R_{ON-P}$ | $V_{DD}$ = 15V, $I_{OUT\_}$ = 100mA | $T_A$ = +25°C | | 1.5 | 2.1 | Ω |
| | | | $T_A$ = +125°C | | 1.9 | 2.75 | |
| | | $V_{DD}$ = 4.5V, $I_{OUT\_}$ = 100mA | $T_A$ = +25°C | | 2.75 | 4 | |
| | | | $T_A$ = +125°C | | 3.75 | 5.5 | |
| Peak Output Current (Sourcing) | $I_{PK-P}$ | $V_{DD}$ = 15V, $C_L$ = 10,000pF | | | 4 | | A |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 4V to 15V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{DD}$ = 15V and $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output-Voltage High | | $I_{OUT\_}$ = 100mA | $V_{DD}$ = 4.5V | $V_{DD}$ - 0.55 | | | V |
| | | | $V_{DD}$ = 15V | $V_{DD}$ - 0.275 | | | |
| **LOGIC INPUT** (Note 3) | | | | | | | |
| Logic 1 Input Voltage | $V_{IH}$ | MAX5054A | | 0.7 x $V_{DD}$ | | | V |
| | | MAX5054B/MAX5055/MAX5056/MAX5057 (Note 4) | | 2.1 | | | |
| Logic 0 Input Voltage | $V_{IL}$ | MAX5054A | | | | 0.3 x $V_{DD}$ | V |
| | | MAX5054B/MAX5055/MAX5056/MAX5057 | | | | 0.8 | |
| Logic-Input Hysteresis | $V_{HYS}$ | MAX5054A | | | 0.1 x $V_{DD}$ | | V |
| | | MAX5054B/MAX5055/MAX5056/MAX5057 | | | 0.3 | | |
| Logic-Input-Current Leakage | | INA+, INB+, INA-, INB- = 0V or $V_{DD}$ | | -1 | +0.1 | +1 | µA |
| Input Capacitance | $C_{IN}$ | | | | 2.5 | | pF |
| **SWITCHING CHARACTERISTICS FOR $V_{DD}$ = 15V** (Figure 1) | | | | | | | |
| OUT_ Rise Time | $t_R$ | $C_L$ = 1000pF | | | 4 | | ns |
| | | $C_L$ = 5000pF | | | 18 | | |
| | | $C_L$ = 10,000pF | | | 32 | | |
| OUT_ Fall Time | $t_F$ | $C_L$ = 1000pF | | | 4 | | ns |
| | | $C_L$ = 5000pF | | | 15 | | |
| | | $C_L$ = 10,000pF | | | 26 | | |
| Turn-On Delay Time | $t_{D-ON}$ | $C_L$ = 10,000pF (Note 2) | | 10 | 20 | 34 | ns |
| Turn-Off Delay Time | $t_{D-OFF}$ | $C_L$ = 10,000pF (Note 2) | | 10 | 20 | 34 | ns |
| **SWITCHING CHARACTERISTICS FOR $V_{DD}$ = 4.5V** (Figure 1) | | | | | | | |
| OUT_ Rise Time | $t_R$ | $C_L$ = 1000pF | | | 7 | | ns |
| | | $C_L$ = 5000pF | | | 37 | | |
| | | $C_L$ = 10,000pF | | | 85 | | |
| OUT_ Fall Time | $t_F$ | $C_L$ = 1000pF | | | 7 | | ns |
| | | $C_L$ = 5000pF | | | 30 | | |
| | | $C_L$ = 10,000pF | | | 75 | | |
| Turn-On Delay Time | $t_{D-ON}$ | $C_L$ = 10,000pF (Note 2) | | 18 | 35 | 70 | ns |
| Turn-Off Delay Time | $t_{D-OFF}$ | $C_L$ = 10,000pF (Note 2) | | 18 | 35 | 70 | ns |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 4V to 15V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $V_{DD}$ = 15V and $T_A$ = +25°C.) (Note 1)

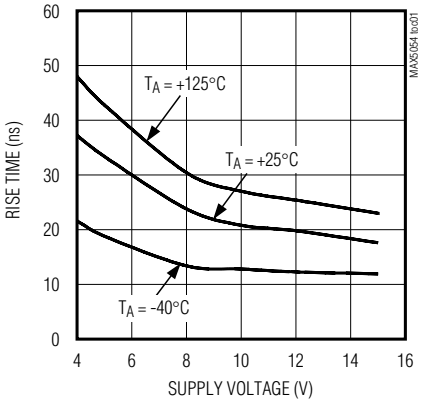
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **MATCHING CHARACTERISTICS** | | | | | | |
| Mismatch Propagation Delays from Inverting and Noninverting Inputs to Output | $\Delta t_{ON-OFF}$ | $V_{DD}$ = 15V, $C_L$ = 10,000pF | | 2 | | ns |
| | | $V_{DD}$ = 4.5V, $C_L$ = 10,000pF | | 4 | | |
| Mismatch Propagation Delays Between Channel A and Channel B | $\Delta t_{A-B}$ | $V_{DD}$ = 15V, $C_L$ = 10,000pF | | 1 | | ns |
| | | $V_{DD}$ = 4.5V, $C_L$ = 10,000pF | | 2 | | |

**Note 1:** All devices are 100% tested at $T_A$ = +25°C. Specifications over -40°C to +125°C are guaranteed by design.
**Note 2:** Limits are guaranteed by design, not production tested.
**Note 3:** The logic-input thresholds are tested at $V_{DD}$ = 4V and $V_{DD}$ = 15V.
**Note 4:** TTL compatible with reduced noise immunity.

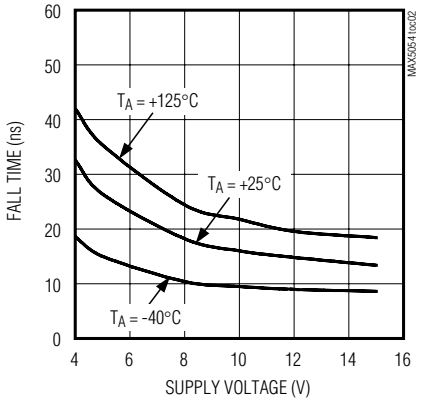
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

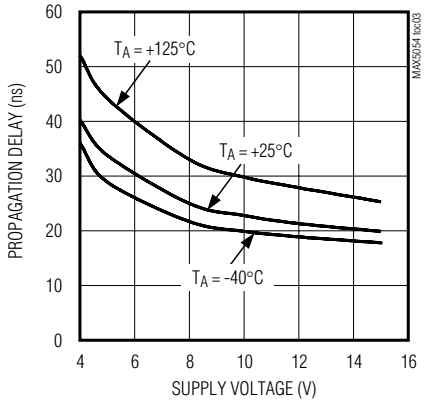
**RISE TIME vs. SUPPLY VOLTAGE ($C_L$ = 5000pF)**



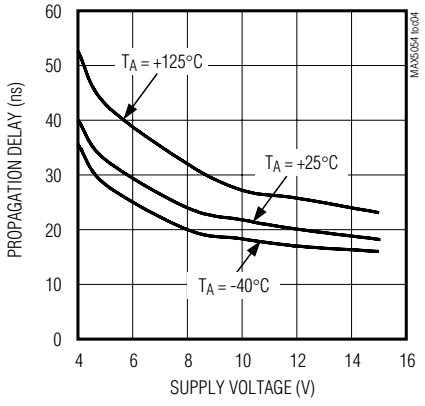

**FALL TIME vs. SUPPLY VOLTAGE ($C_L$ = 5000pF)**



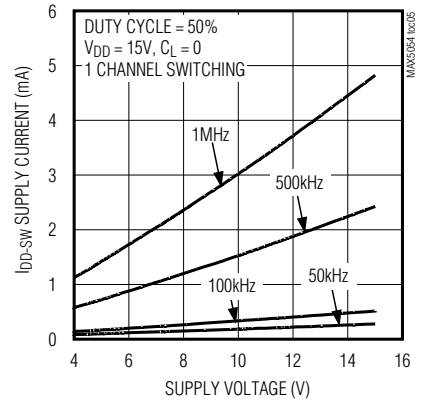

**PROPAGATION DELAY TIME, LOW-TO-HIGH vs. SUPPLY VOLTAGE ($C_L$ = 5000pF)**



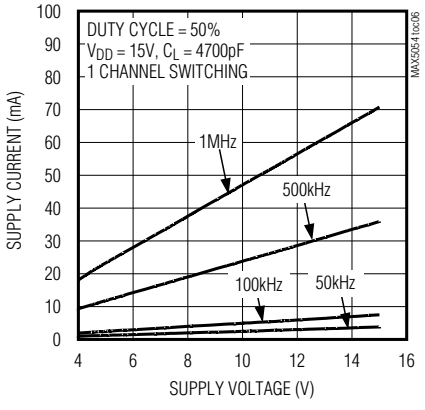

**PROPAGATION DELAY TIME, HIGH-TO-LOW vs. SUPPLY VOLTAGE ($C_L$ = 5000pF)**




**$I_{DD-SW}$ SUPPLY CURRENT vs. SUPPLY VOLTAGE**



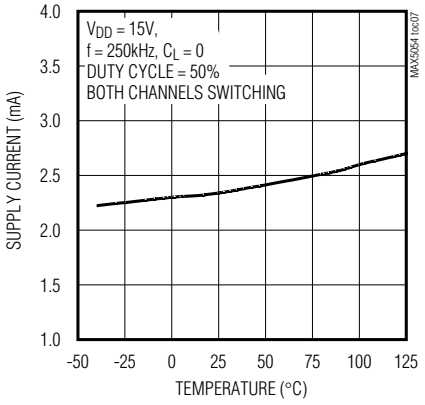

**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



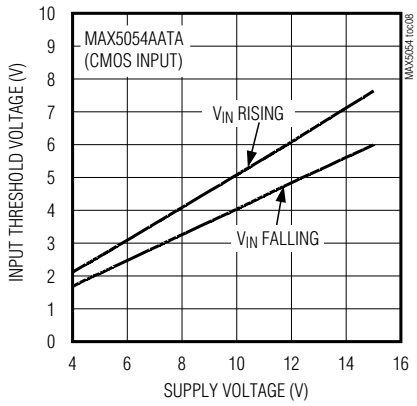
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

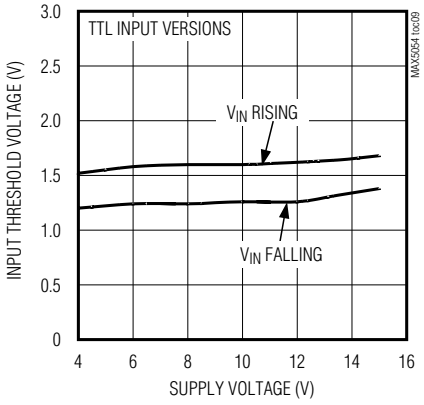
**$I_{DD-SW}$ SUPPLY CURRENT vs. TEMPERATURE**



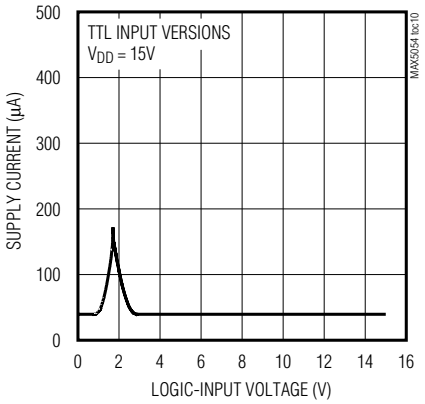

**INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE**



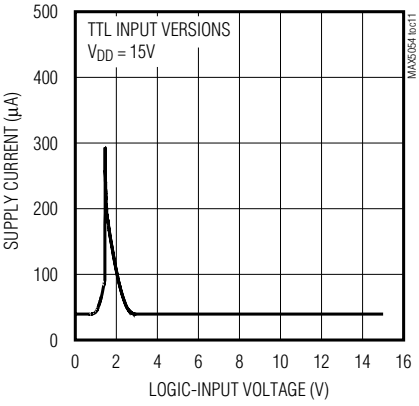

**INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE**



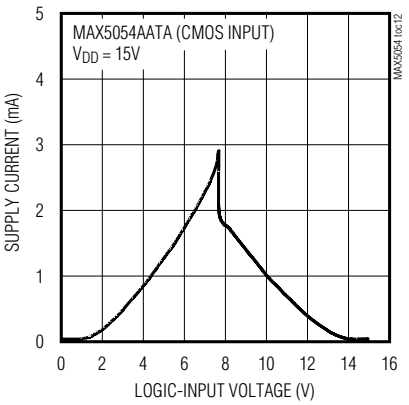

**SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT LOW-TO-HIGH)**



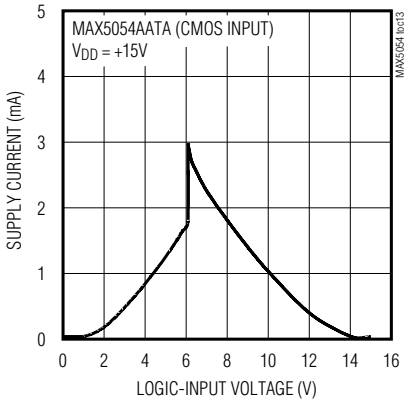

**SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT HIGH-TO-LOW)**



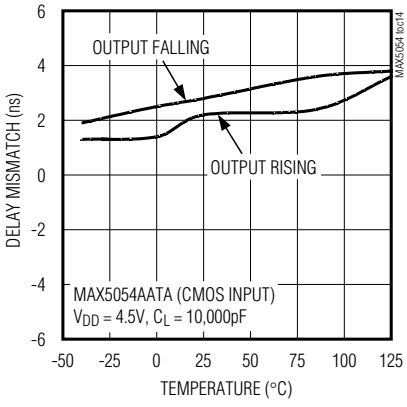

**SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT LOW-TO-HIGH)**



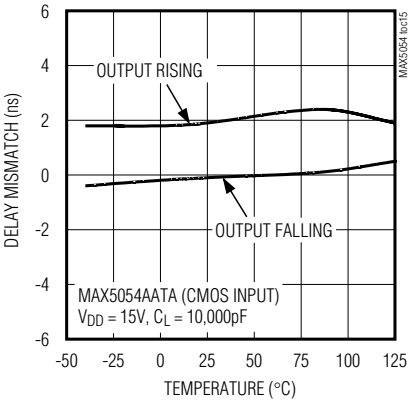

**SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT HIGH-TO-LOW)**




**DELAY MISMATCH BETWEEN IN_+ AND IN_- TO OUT_ vs. TEMPERATURE**



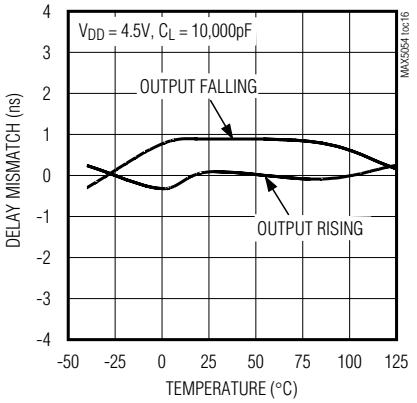

**DELAY MISMATCH BETWEEN IN_+ AND IN_- TO OUT_ vs. TEMPERATURE**



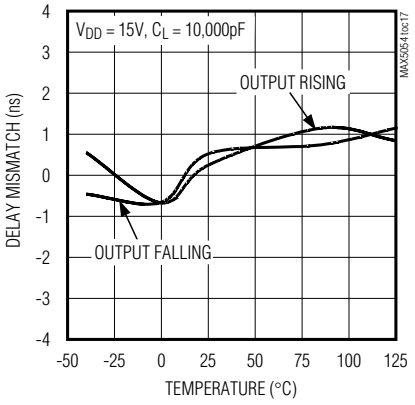
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

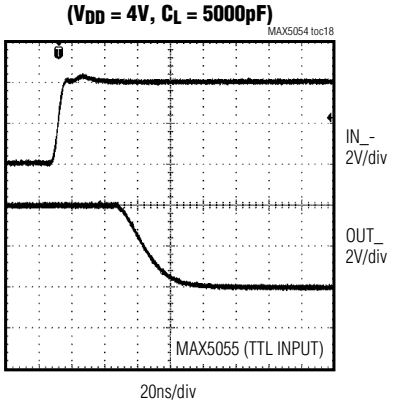
**DELAY MISMATCH BETWEEN 2 CHANNELS vs. TEMPERATURE**



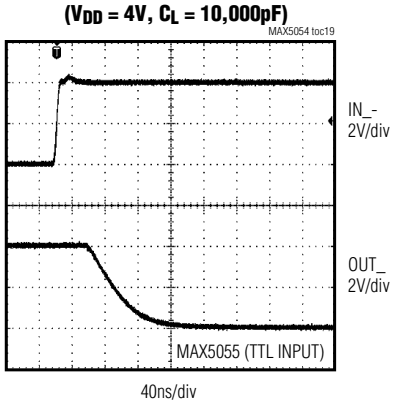

**DELAY MISMATCH BETWEEN 2 CHANNELS vs. TEMPERATURE**



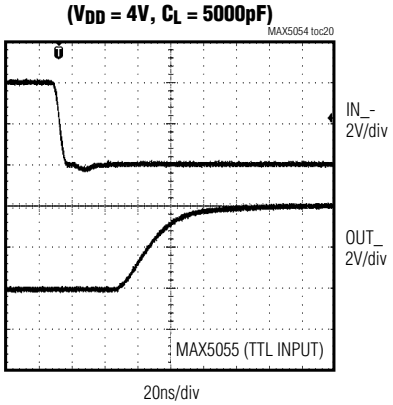

**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 4V, $C_L$ = 5000pF)**



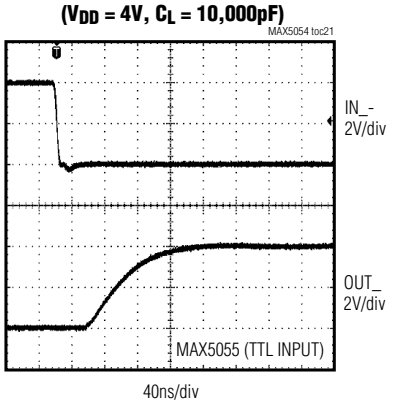

**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 4V, $C_L$ = 10,000pF)**




**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 4V, $C_L$ = 5000pF)**



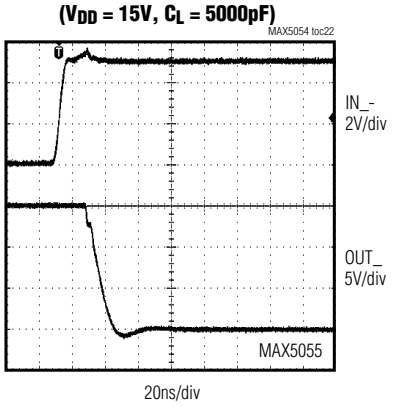

**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 4V, $C_L$ = 10,000pF)**



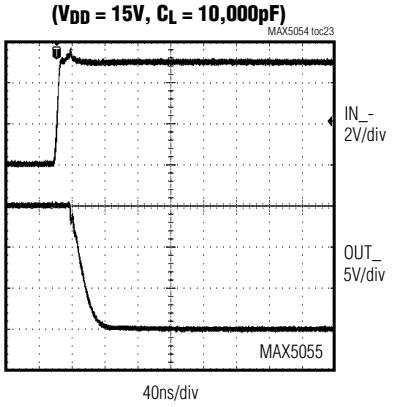
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

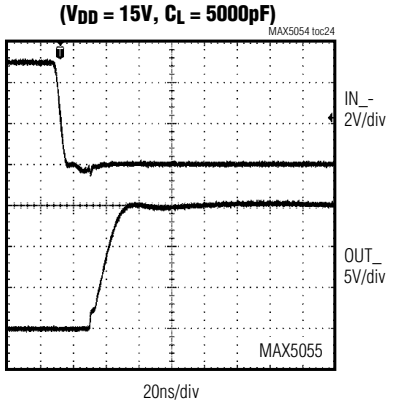
**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 15V, $C_L$ = 5000pF)**



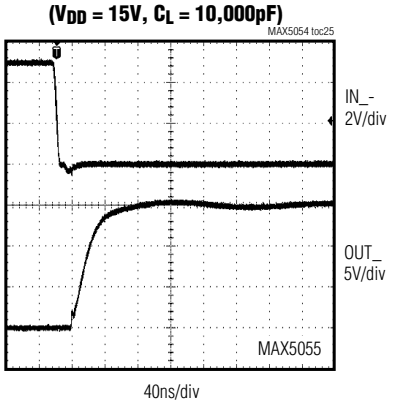

**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 15V, $C_L$ = 10,000pF)**



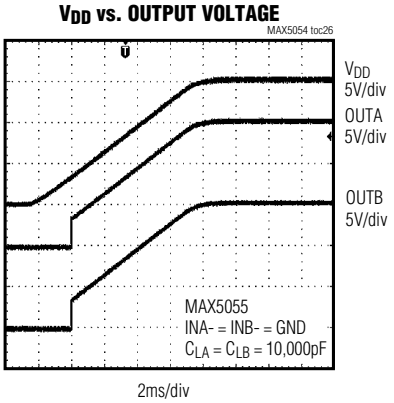

**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 15V, $C_L$ = 5000pF)**



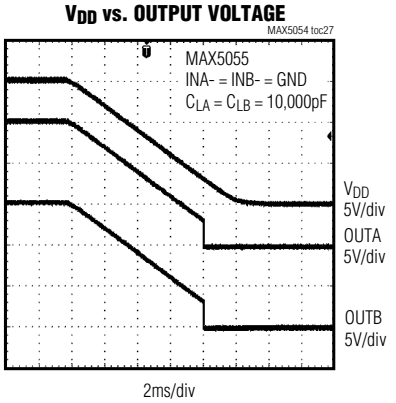

**LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V_{DD}$ = 15V, $C_L$ = 10,000pF)**




**$V_{DD}$ vs. OUTPUT VOLTAGE**




**$V_{DD}$ vs. OUTPUT VOLTAGE**



## Pin Descriptions

### MAX5054

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | INA- | Inverting Logic-Input Terminal for Driver A. Connect to GND when not used. |
| 2 | INB- | Inverting Logic-Input Terminal for Driver B. Connect to GND when not used. |
| 3 | GND | Ground |
| 4 | OUTB | Driver B Output. Sources or sinks current for channel B to turn the external MOSFET on or off. |
| 5 | $V_{DD}$ | Power Supply. Bypass to GND with one or more 0.1µF ceramic capacitors. |
| 6 | OUTA | Driver A Output. Sources or sinks current for channel A to turn the external MOSFET on or off. |
| 7 | INB+ | Noninverting Logic-Input Terminal for Driver B. Connect to $V_{DD}$ when not used. |
| 8 | INA+ | Noninverting Logic-Input Terminal for Driver A. Connect to $V_{DD}$ when not used. |
| — | EP | Exposed Pad. Internally connected to GND. Do not use the exposed pad as the only electrical ground connection. |

### MAX5055/MAX5056/MAX5057

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX5055 | MAX5056 | MAX5057 | | |
| 1, 8 | 1, 8 | 1, 8 | N.C. | No Connection. Not internally connected. |
| 2 | — | 2 | INA- | Inverting Logic-Input Terminal for Driver A. Connect to GND if not used. |
| 3 | 3 | 3 | GND | Ground |
| 4 | — | — | INB- | Inverting Logic-Input Terminal for Driver B. Connect to GND if not used. |
| 5 | 5 | 5 | OUTB | Driver B Output. Sources or sinks current for channel B to turn the external MOSFET on or off. |
| 6 | 6 | 6 | $V_{DD}$ | Power Supply. Bypass to GND with one or more 0.1µF ceramic capacitors. |
| 7 | 7 | 7 | OUTA | Driver A Output. Sources or sinks current for channel A to turn the external MOSFET on or off. |
| — | 4 | 4 | INB+ | Noninverting Logic-Input Terminal for Driver B. Connect to $V_{DD}$ if not used. |
| — | 2 | — | INA+ | Noninverting Logic-Input Terminal for Driver A. Connect to $V_{DD}$ if not used. |
| — | — | — | EP | Exposed Pad. Internally connected to GND. Do not use the exposed pad as the only electrical ground connection. |

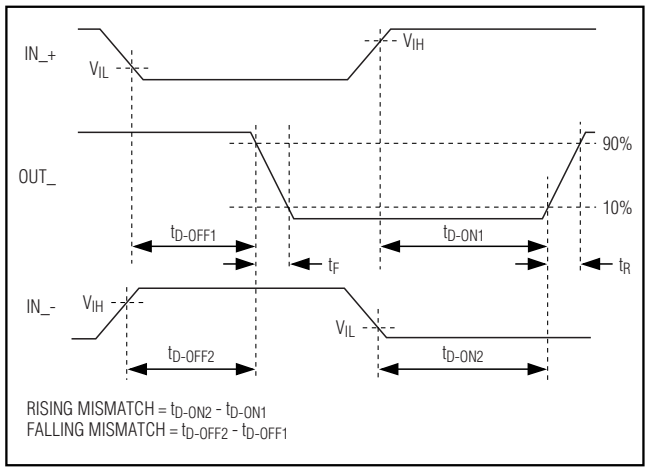



*Figure 1. Timing Diagram*

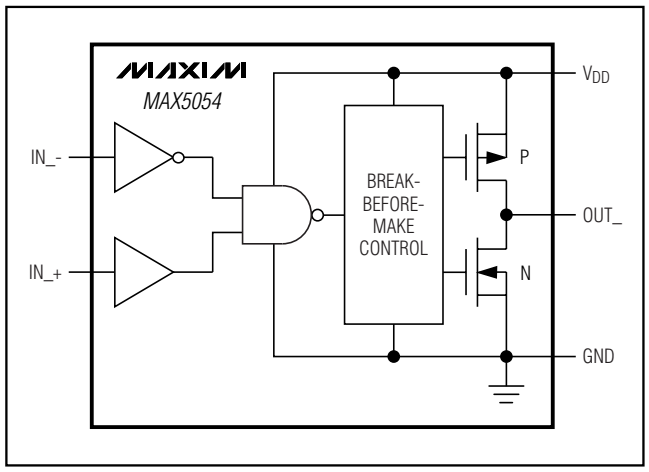



*Figure 2. MAX5054 Block Diagram (1 Driver)*

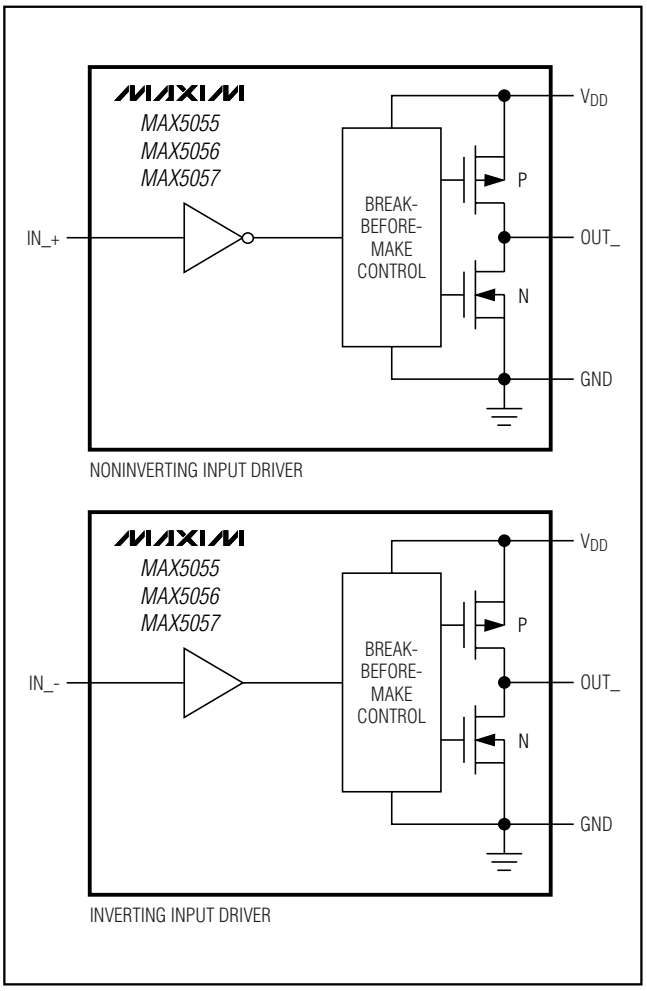



*Figure 3. MAX5055/MAX5056/MAX5057 Functional Diagrams (1 Driver)*

## Detailed Description

### VDD Undervoltage Lockout (UVLO)

The MAX5054–MAX5057 have internal undervoltage lockout for $V_{DD}$. When $V_{DD}$ is below the UVLO threshold, OUT_ is low, independent of the state of the inputs. The undervoltage lockout is typically 3.5V with 200mV typical hysteresis to avoid chattering. When $V_{DD}$ rises above the UVLO threshold, the outputs go high or low depending upon the logic-input levels. Bypass $V_{DD}$ using low-ESR ceramic capacitors for proper operation (see the *Applications Information* section).

### Logic Inputs

The MAX5054B–MAX5057 have TTL-compatible logic inputs, while the MAX5054A is a CMOS logic-input driver. The logic-input signals can be independent of the $V_{DD}$ voltage. For example, the device can be powered by a 5V supply while the logic inputs are provided from CMOS logic. Also, the logic inputs are protected against the voltage spikes up to 18V, regardless of the $V_{DD}$ voltage. The TTL and CMOS logic inputs have 300mV and 0.1 x $V_{DD}$ hysteresis, respectively, to avoid possible double pulsing during transition. The low 2.5pF input capacitance reduces loading and increases switching speed.

### Table 1. MAX5054 Truth Table

| INA+/INB+ | INA-/INB- | OUTA/OUTB |
|---|---|---|
| Low | Low | Low |
| Low | High | Low |
| High | Low | High |
| High | High | Low |

### Table 2. MAX5055/MAX5056/MAX5057 Truth Table

| NONINVERTING | |
|---|---|
| **IN_+** | **OUT_** |
| Low | Low |
| High | High |
| **INVERTING** | |
| **IN_-** | **OUT_** |
| Low | High |
| High | Low |

The logic inputs are high impedance and must not be left floating. If the inputs are left open, OUT_ can go to an undefined state as soon as $V_{DD}$ rises above the UVLO threshold. Therefore, the PWM output from the controller must assume proper state when powering up the device.

The MAX5054 has two logic inputs per driver providing greater flexibility in controlling the MOSFET. Use IN_+ for noninverting logic and IN_- for inverting logic operation. Connect IN_+ to $V_{DD}$ and IN_- to GND if not used. Alternatively, the unused input can be used as an ON/OFF function. Use IN_+ for active-low shutdown logic and IN_- for active-high shutdown logic (see Figure 4). See Table 1 for all possible input combinations.

#### Driver Output

The MAX5054–MAX5057 have low $R_{DS(ON)}$ p-channel and n-channel devices (totem pole) in the output stage for the fast turn-on and turn-off high gate-charge switching MOSFETs. The peak source or sink current is typically 4A. The OUT_ voltage is approximately equal to $V_{DD}$ when in high state and is ground when in low state. The driver $R_{DS(ON)}$ is lower at higher $V_{DD}$, thus higher source-/sink-current capability and faster switching speeds. The propagation delays from the noninverting and inverting logic inputs to outputs are matched to 2ns. The break-before-make logic avoids any cross-conduction between the internal p- and n-channel devices, and eliminates shoot-through currents reducing the quiescent supply current.

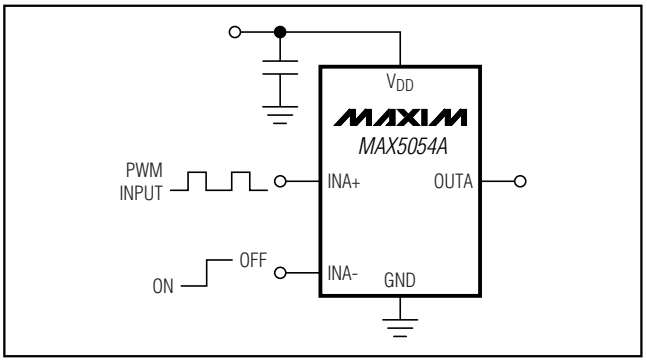



*Figure 4. Unused Input as an ON/OFF Function (1/2 MAX5054A)*

## Applications Information

#### RLC Series Circuit

The driver's $R_{DS(ON)}$ ($R_{ON}$), internal bond and lead inductance ($L_P$), trace inductance ($L_S$), gate inductance ($L_G$), and gate capacitance ($C_G$) form a series RLC circuit with a second-order characteristic equation. The series RLC circuit has an undamped natural frequency ($\varpi_0$) and a damping ratio ($\zeta$) where:

$$\varpi_0 = \frac{1}{\sqrt{(L_P + L_S + L_G) \times C_G}}$$

$$\xi = \frac{R_{ON}}{2 \times \sqrt{\frac{(L_P + L_S + L_G)}{C_G}}}$$

The damping ratio needs to be greater than 0.5 (ideally 1) to avoid ringing. Add a small resistor ($R_{GATE}$) in series with the gate when driving a very low gate-charge MOSFET, or when the driver is placed away from the MOSFET. Use the following equation to calculate the series resistor:

$$R_{GATE} \geq \sqrt{\frac{(L_P + L_S + L_G)}{C_G}} - R_{ON}$$

$L_P$ can be approximated as 3nH and 2nH for SO and TDFN packages, respectively. $L_S$ is on the order of 20nH/in. Verify $L_G$ with the MOSFET vendor.

### Supply Bypassing and Grounding

Pay extra attention to bypassing and grounding the MAX5054–MAX5057. Peak supply and output currents may exceed 8A when both drivers drive large external capacitive loads in phase. Supply voltage drops and ground shifts create forms of negative feedback for inverters and may degrade the delay and transition times. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same AC ground return path. Any series inductance in the $V_{DD}$, OUT_, and/or GND paths can cause oscillations due to the very high di/dt when switching the MAX5054–MAX5057 with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel as close to the device as possible to bypass $V_{DD}$ to GND. Use a ground plane to minimize ground return resistance and series inductance. Place the external MOSFET as close as possible to the MAX5054–MAX5057 to further minimize board inductance and AC path impedance.

### Power Dissipation

Power dissipation of the MAX5054–MAX5057 consists of three components: caused by the quiescent current, capacitive charge/discharge of internal nodes, and the output current (either capacitive or resistive load). Maintain the sum of these components below the maximum power dissipation limit.

The current required to charge and discharge the internal nodes is frequency dependent (see the Supply Current vs. Supply Voltage graph in the *Typical Operating Characteristics*). The power dissipation ($P_Q$) due to the quiescent switching supply current ($I_{DD-SW}$) per driver can be calculated as:

$$P_Q = V_{DD} \times I_{DD-SW}$$

For capacitive loads, use the following equation to estimate the power dissipation per driver:

$$P_{CLOAD} = C_{LOAD} \times (V_{DD})^2 \times f_{SW}$$

where $C_{LOAD}$ is the capacitive load, $V_{DD}$ is the supply voltage, and $f_{SW}$ is the switching frequency.

Calculate the total power dissipation ($P_T$) per driver as follows:

$$P_T = P_Q + P_{CLOAD}$$

Use the following equation to estimate the MAX5054–MAX5057 total power dissipation per driver when driving a ground-referenced resistive load:

$$P_T = P_Q + P_{RLOAD}$$

$$P_{RLOAD} = D \times R_{ON(MAX)} \times I_{LOAD}^2$$

where D (duty cycle) is the fraction of the period the MAX5054–MAX5057's output pulls high duty cycle, $R_{ON(MAX)}$ is the maximum on-resistance of the device with the output high, and $I_{LOAD}$ is the output load current of the MAX5054–MAX5057.

### Layout Information

The MAX5054–MAX5057 MOSFET drivers source and sink large currents to create very fast rising and falling edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PC board layout guidelines when designing with the MAX5054–MAX5057:

- Place one or more 0.1µF decoupling ceramic capacitors from $V_{DD}$ to GND as close to the device as possible. Connect $V_{DD}$ and GND to large copper areas. Place one bulk capacitor of 10µF (min) on the PC board with a low resistance path to the $V_{DD}$ input and GND of the MAX5054–MAX5057.
- Two AC current loops form between the device and the gate of the driven MOSFET. The MOSFET looks like a large capacitance from gate to source when the gate pulls low. The active current loop is from the MOSFET gate to OUT_ of the MAX5054–MAX5057, to GND of the MAX5054–MAX5057, and to the source of the MOSFET. When the gate of the MOSFET pulls high, the active current is from the $V_{DD}$ terminal of the decoupling capacitor, to $V_{DD}$ of the MAX5054–MAX5057, to OUT_ of the MAX5054–MAX5057, to the MOSFET gate, to the MOSFET source, and to the negative terminal of the decoupling capacitor. Both charging current and discharging current loops are important. Minimize the physical distance and the impedance in these AC current paths.
- Keep the device as close to the MOSFET as possible.
- In a multilayer PC board, the inner layers should consist of a GND plane containing the discharging and charging current loops.
- Pay extra attention to the ground loop and use a low-impedance source when using a TTL logic-input device. Fast fall time at OUT_ may corrupt the input during transition.

### Exposed Pad

Both the SO-EP and TDFN-EP packages have an exposed pad on the bottom of their package. These pads are internally connected to GND. For the best thermal conductivity, solder the exposed pad to the ground plane to dissipate 1.5W and 1.9W in SO-EP and TDFN-EP packages, respectively. Do not use the ground-connected pads as the only electrical ground connection or ground return. Use GND (pin 3) as the primary electrical ground connection.

## Additional Application Circuits

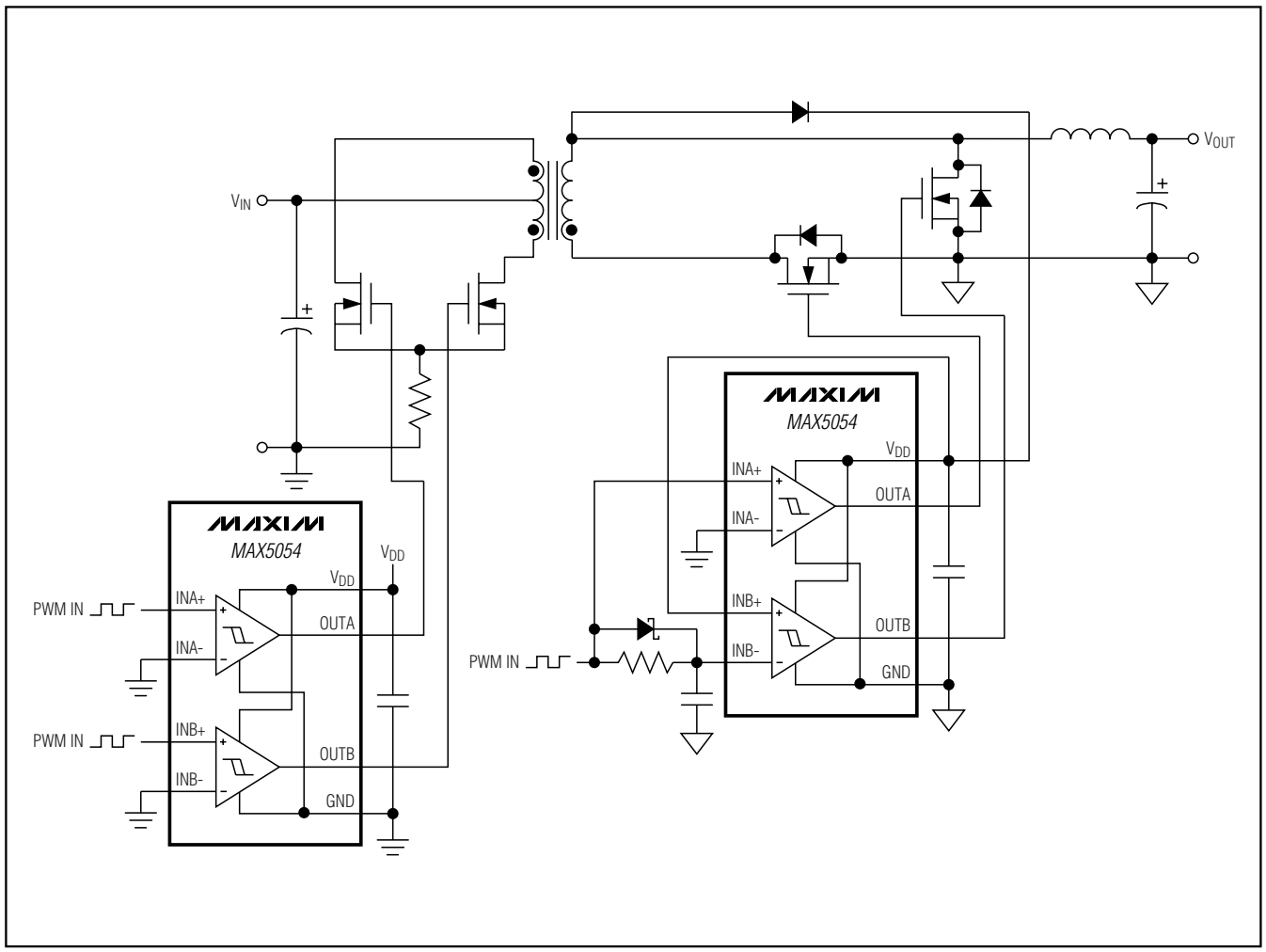



*Figure 5. Push-Pull Converter with Synchronous Rectification Drive Using MAX5054*

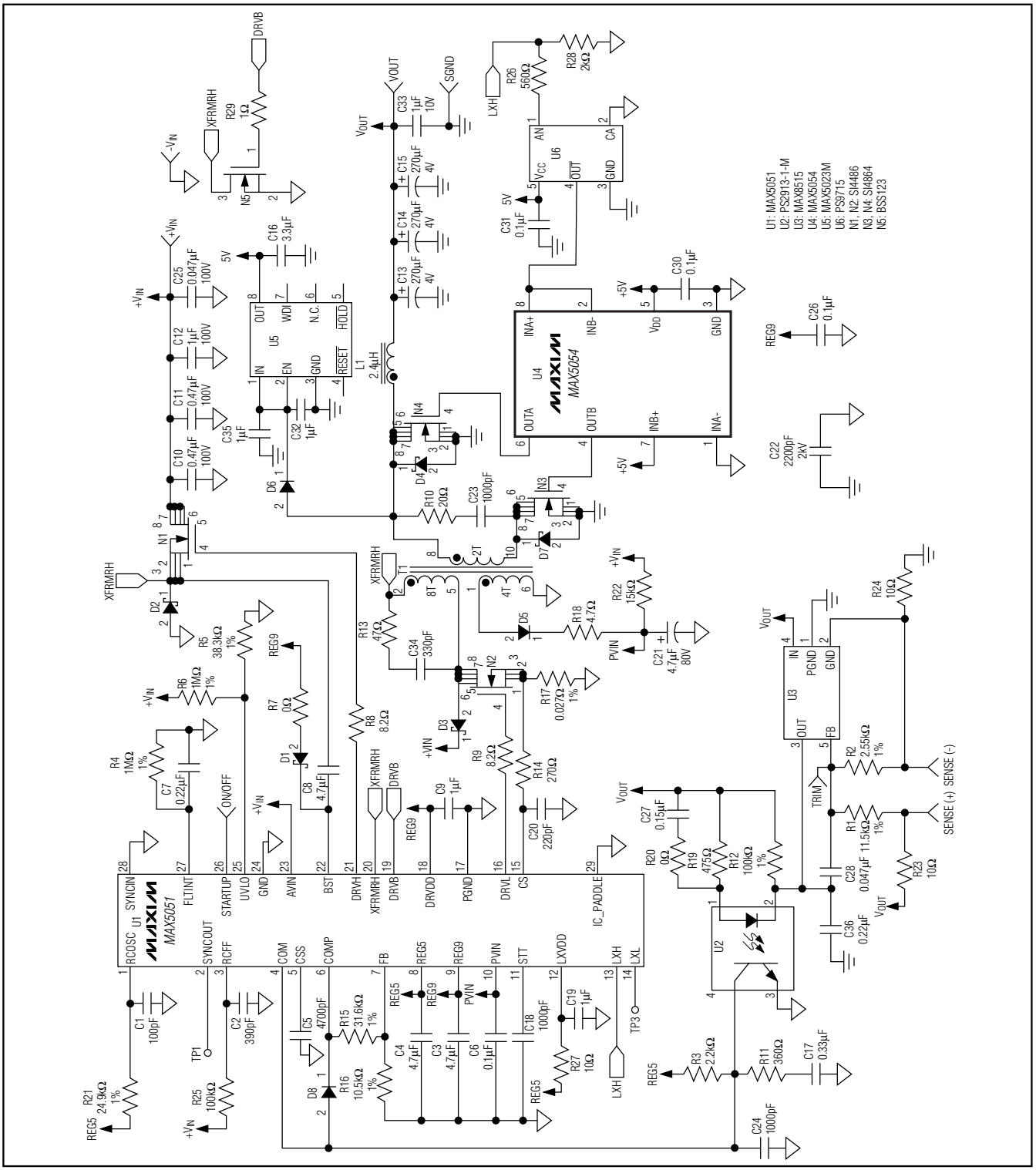
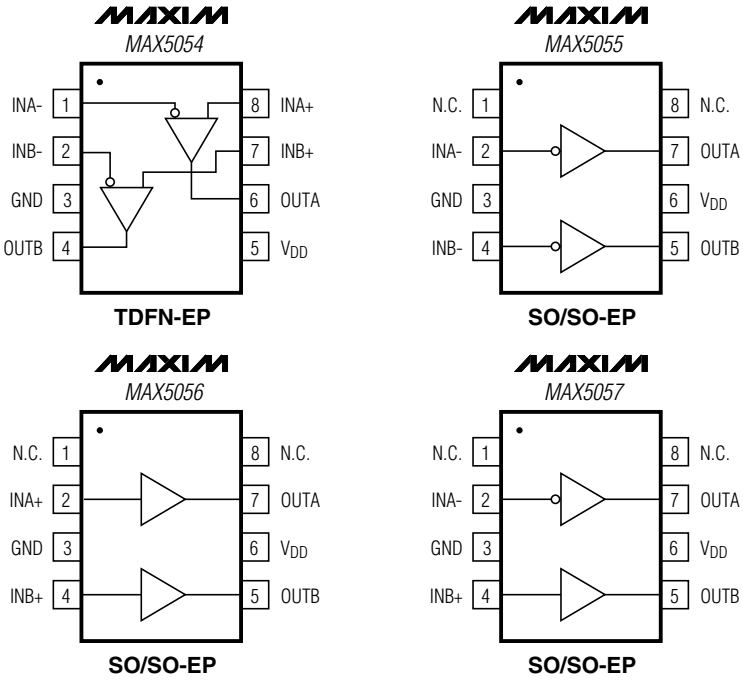



*Figure 6. Schematic of a 48V Input, 3.3V at 15A Output Synchronously Rectified, Isolated Power Supply*

# 4A, 20ns, Dual MOSFET Drivers

## Pin Configurations

TOP VIEW




## Selector Guide

| PART | PIN-PACKAGE | LOGIC INPUT |
|---|---|---|
| MAX5054AATA | 8 TDFN-EP* | $V_{DD}$ / 2 CMOS Dual Inverting and Dual Noninverting Inputs |
| MAX5054BATA | 8 TDFN-EP* | TTL Dual Inverting and Dual Noninverting Inputs |
| MAX5055AASA | 8 SO-EP* | TTL Dual Inverting Inputs |
| MAX5055BASA | 8 SO | TTL Dual Inverting Inputs |
| MAX5056AASA | 8 SO-EP* | TTL Dual Noninverting Inputs |
| MAX5056BASA | 8 SO | TTL Dual Noninverting Inputs |
| MAX5057AASA | 8 SO-EP* | TTL Inverting and Noninverting Inputs |
| MAX5057BASA | 8 SO | TTL Inverting and Noninverting Inputs |

**EP = Exposed pad.*

## Chip Information

TRANSISTOR COUNT: 258

PROCESS: CMOS

## Package Information

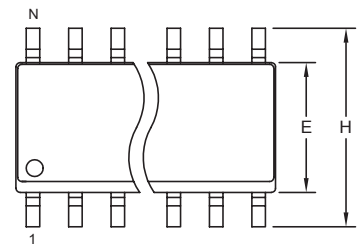
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

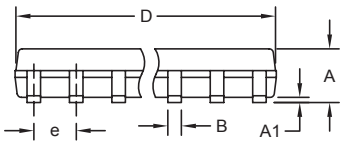
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

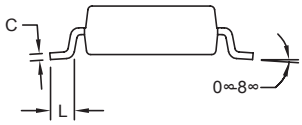
| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |




TOP VIEW




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, .150" SOIC

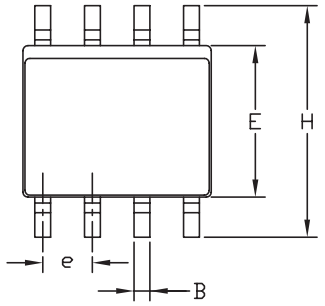
| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |

# 4A, 20ns, Dual MOSFET Drivers

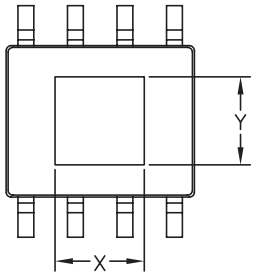
## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

8L, SOIC EXP. PAD.EPS



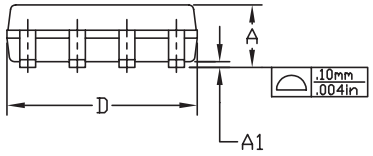

TOP VIEW

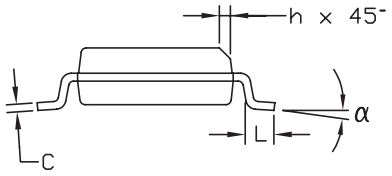



BOTTOM VIEW

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.056 | 0.066 | 1.43 | 1.68 |
| A1 | 0.000 | 0.004 | 0.00 | 0.10 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| D | 0.189 | 0.196 | 4.80 | 4.98 |
| e | 0.050 | BSC | 1.27 | BSC |
| E | 0.150 | 0.157 | 3.81 | 3.99 |
| H | 0.230 | 0.244 | 5.81 | 6.20 |
| h | 0.010 | 0.016 | 0.25 | 0.41 |
| L | 0.016 | 0.035 | 0.41 | 0.89 |
| α | 0° | 8° | 0° | 8° |

| PKG. | X (mm) MIN | X (mm) MAX | Y (mm) MIN | Y (mm) MAX |
|---|---|---|---|---|
| S8E-12 | 2.184 | 2.388 | 2.184 | 2.388 |
| S8E-14 | 2.311 | 2.515 | 2.997 | 3.200 |




NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 EXCEPT DIMENSION A1.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

DALLAS SEMICONDUCTOR MAXIM

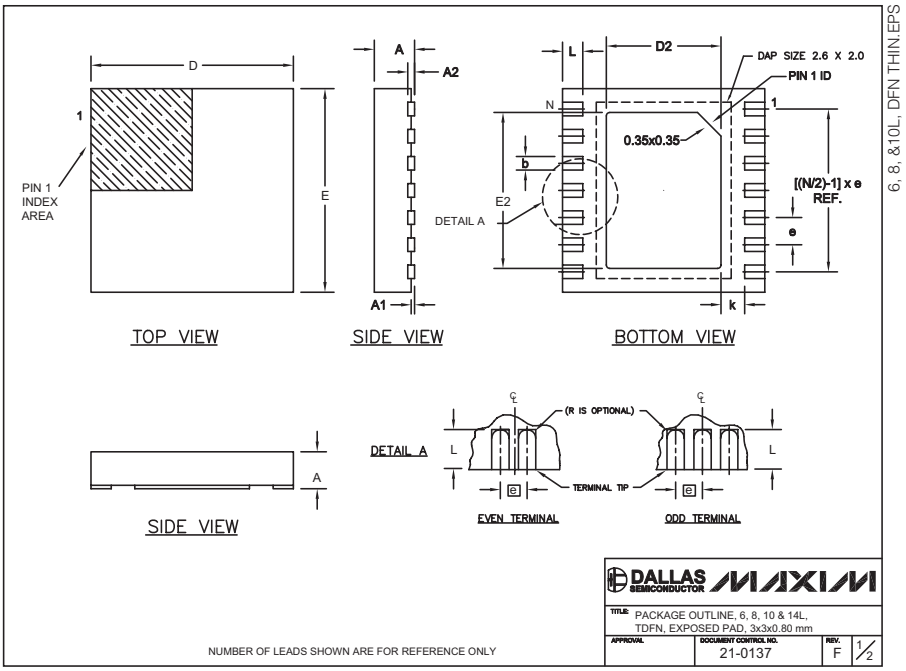
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
8L SOIC, .150" EXPOSED PAD

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0111 | B | 1/1 |

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)




| COMMON DIMENSIONS | | |
|---|---|---|
| SYMBOL | MIN. | MAX. |
| A | 0.70 | 0.80 |
| D | 2.90 | 3.10 |
| E | 2.90 | 3.10 |
| A1 | 0.00 | 0.05 |
| L | 0.20 | 0.40 |
| k | 0.25 MIN. | |
| A2 | 0.20 REF. | |

| PACKAGE VARIATIONS | | | | | | | |
|---|---|---|---|---|---|---|---|
| PKG. CODE | N | D2 | E2 | e | JEDEC SPEC | b | [(N/2)-1] x e |
| T633-1 | 6 | 1.50±0.10 | 2.30±0.10 | 0.95 BSC | MO229 / WEEA | 0.40±0.05 | 1.90 REF |
| T833-1 | 8 | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WEEC | 0.30±0.05 | 1.95 REF |
| T1033-1 | 10 | 1.50±0.10 | 2.30±0.10 | 0.50 BSC | MO229 / WEED-3 | 0.25±0.05 | 2.00 REF |
| T1433-1 | 14 | 1.70±0.10 | 2.30±0.10 | 0.40 BSC | ---- | 0.20±0.03 | 2.40 REF |
| T1433-2 | 14 | 1.70±0.10 | 2.30±0.10 | 0.40 BSC | ---- | 0.20±0.03 | 2.40 REF |

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 6, 8, 10 & 14L,
TDFN, EXPOSED PAD, 3x3x0.80 mm
21-0137
F
2/2