19-4178; Rev 0; 6/08

SATA I/SATA II Bidirectional Re-Driver

General Description

The MAX4951 dual-channel buffer is designed to re-drive serial-ATA (SATA) I and SATA II signals and is functional up to 6.0Gbps for next-generation data rates. The MAX4951 can be placed near an eSATA connector to overcome board losses and produce an eSATA-compatible signal level.

The MAX4951 preserves signal integrity at the receiver by reestablishing full output levels, and can reduce the total system jitter (T_J) by squaring up the signal. This device features channel-independent digital boost controls to drive SATA outputs over longer trace lengths, or to meet eSATA specifications. SATA Out-Of-Band (OOB) signaling is supported using high-speed amplitude detection on the inputs, and squelch on the corresponding outputs. Inputs and outputs are all internally 50Ω terminated and must be AC-coupled to the SATA controller IC and SATA device.

The MAX4951 operates from a single +3.3V (typ) supply and is available in a small, 4mm x 4mm, TQFN package with flow-through traces for ease of layout. This device is specified over the 0°C to +70°C operating temperature range.

Applications

Servers

Desktop Computers

Notebook Computers

Docking Stations

Data Storage/Workstations

Features

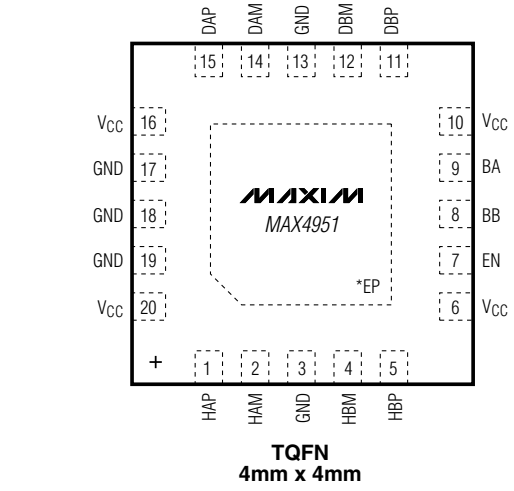
- **Single +3.3V (typ) Supply Operation**
- **Supports SATA I (1.5Gbps) and SATA II (3.0Gbps)**
- **Supports up to 6.0Gbps for Next-Generation Applications**
- **Meets SATA I, SATA II Input-/Output-Return Loss Mask**
- **Supports eSATA Levels**
- **Supports SATA Out-of-Band (OOB) Signaling**
- **Internal Input/Output 50Ω Termination Resistors**
- **In-Line Signal Traces for Flow-Through Layout**
- **Space-Saving, 4mm x 4mm, TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4951CTP+	0°C to +70°C	20 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



TQFN
4mm x 4mm

*CONNECT EXPOSED PAD (EP) TO GND.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} .....-0.3V to +4.0V
HAP, HAM, DBP, DBM, EN, BA, BB
(Note 1).....-0.3V to (V_{CC} + 0.3V)
Short-Circuit Output Current
(HBP, HBM, DAP, DAM) 90mA
Continuous Current at Inputs
(HAP, HAM, DBP, DBM).....±30mA
Continuous Current
(EN, BA, BB).....±5mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 25.6mW/°C above +70°C) 2051mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
20-Pin TQFN.....6°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
20-Pin TQFN.....39°C/W
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: All I/O pins are clamped by internal diodes.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_L = 10nF, R_L = 50Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Power-Supply Range	V_{CC}		3.0		3.6	V
Operating Supply Current	I_{CC}	BA = BB = V_{CC}		90	125	mA
		BA = BB = GND		70	100	
Standby Supply Current	I_{STBY}	EN = GND		7	10	mA
Single-Ended Input Resistance	$Z_{RX-SE-DC}$		40			Ω
Differential Input Resistance	$Z_{RX-DIFF-DC}$		85	100	115	Ω
Single-Ended Output Resistance	$Z_{TX-SE-DC}$		40			Ω
Differential Output Resistance	$Z_{TX-DIFF-DC}$		85	100	115	Ω
AC PERFORMANCE						
Differential Input Return Loss (Note 4)	$RL_{RX-DIFF}$	f = 150MHz to 300MHz		-29	-18	dB
		f = 300MHz to 600MHz		-26	-14	
		f = 600MHz to 1200MHz		-22	-10	
		f = 1.2GHz to 2.4GHz		-18	-8	
		f = 2.4GHz to 3.0GHz		-15	-3	
		f = 3.0GHz to 5.0GHz		-14	-1	
Common-Mode Input Return Loss (Note 4)	RL_{RX-CM}	f = 150MHz to 300MHz			-5	dB
		f = 300MHz to 600MHz			-5	
		f = 600MHz to 1200MHz			-2	
		f = 1.2GHz to 2.4GHz			-2	
		f = 2.4GHz to 3.0GHz			-2	
		f = 3.0GHz to 5.0GHz			-1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_L = 10nF, R_L = 50Ω, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Output Return Loss (Note 4)	$RL_{TX-DIFF}$	f = 150MHz to 300MHz			-32	-14	dB
		f = 300MHz to 600MHz			-26	-8	
		f = 600MHz to 1200MHz			-21	-6	
		f = 1.2GHz to 2.4GHz			-16	-6	
		f = 2.4GHz to 3.0GHz			-15	-3	
		f = 3.0GHz to 5.0GHz			-13	-1	
Common-Mode Output Return Loss (Note 4)	RL_{TX-CM}	f = 150MHz to 300MHz				-8	dB
		f = 300MHz to 600MHz				-5	
		f = 600MHz to 1200MHz				-2	
		f = 1.2GHz to 2.4GHz				-2	
		f = 2.4GHz to 3.0GHz				-2	
		f = 3.0GHz to 5.0GHz				-1	
Differential Input Signal Range	$V_{RX-DFF-PP}$	SATA 1.5Gbps/3.0Gbps		220		1600	mV_{P-P}
Differential Output Swing	$V_{TX-DFF-PP}$	f = 750MHz	BA = BB = GND	450	525	650	mV_{P-P}
			BA = BB = V_{CC}	770	930	1144	
Propagation Delay	t_{PD}				240		ps
Output Rise/Fall Time	t_R	(Notes 4, 5)			60		ps
Deterministic Jitter	$T_{TX-DJ-DFF}$	Up to 6.0Gbps (Notes 4, 6)				15	ps_{P-P}
Random Jitter	$T_{TX-RJ-DFF}$	Up to 6.0Gbps (Notes 4, 6)				1.8	ps_{RMS}
OOB Detector Threshold	V_{TH-OOB}	SATA OOB		50		150	mV_{P-P}
OOB Output Startup/Shutdown Time	t_{OOB}	(Note 7)			2	5	ns
Crosstalk	CTK	f ≤ 1.5GHz	BA = BB = GND		-35		dB
			BA = BB = V_{CC}		-30		
LOGIC INPUT							
Input Logic-High	V_{IH}			1.4			V
Input Logic-Low	V_{IL}					0.6	V
Input Logic Hysteresis	V_{HYST}				0.1		V

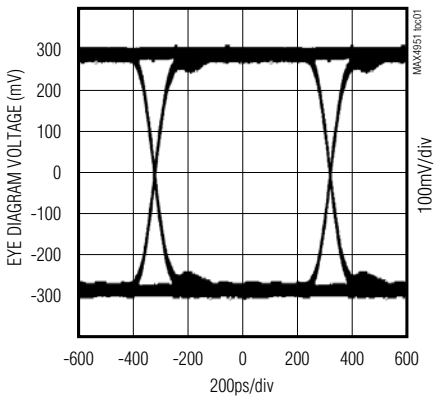
Note 3: All devices are 100% production tested at T_A = +70°C. All temperature limits are guaranteed by design.
Note 4: Guaranteed by design.
Note 5: Rise and fall times are measured using 20% and 80% levels.
Note 6: DJ measured using K28.5 pattern; RJ measured using K28.7 pattern.
Note 7: Total time for OOB detection circuit to enable/squelch the output.

SATA I/SATA II Bidirectional Re-Driver

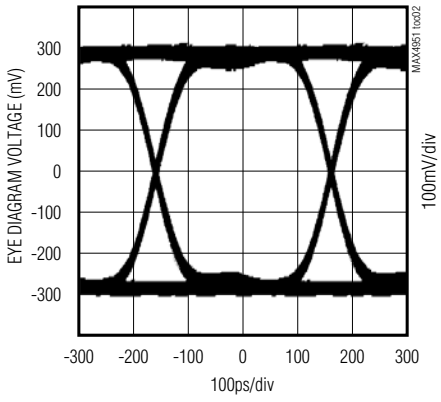
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, all eye diagrams measured using K28.5 pattern.)

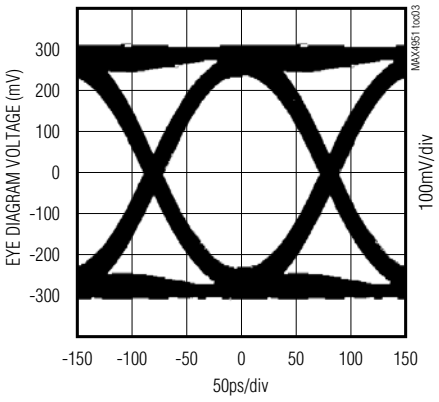
BA = BB = GND EYE DIAGRAM ($V_{RX-DFF-PP}$ = 220mV$_{P-P}$, 1.5Gbps)



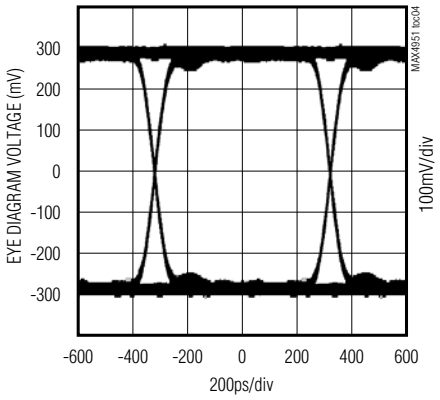
BA = BB = GND EYE DIAGRAM ($V_{RX-DFF-PP}$ = 220mV$_{P-P}$, 3.0Gbps)



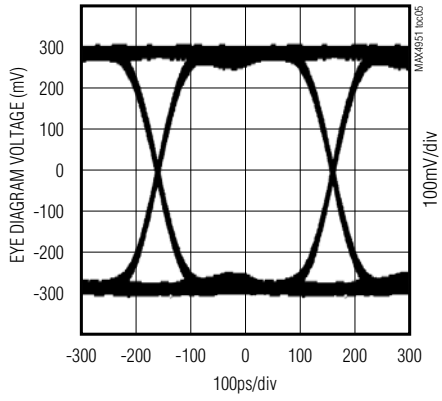
BA = BB = GND EYE DIAGRAM ($V_{RX-DFF-PP}$ = 220mV$_{P-P}$, 6.0Gbps)



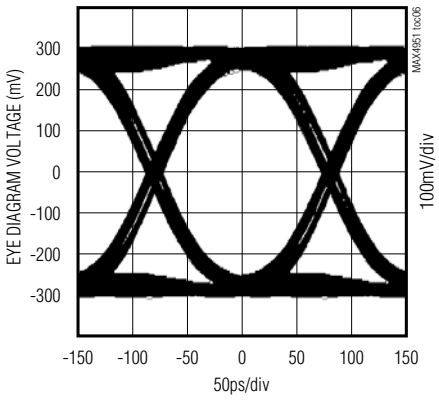
BA = BB = GND EYE DIAGRAM ($V_{RX-DFF-PP}$ = 1600mV$_{P-P}$, 1.5Gbps)



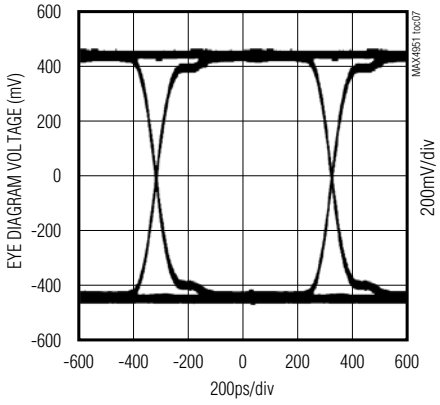
BA = BB = GND EYE DIAGRAM ($V_{RX-DFF-PP}$ = 1600mV$_{P-P}$, 3.0Gbps)



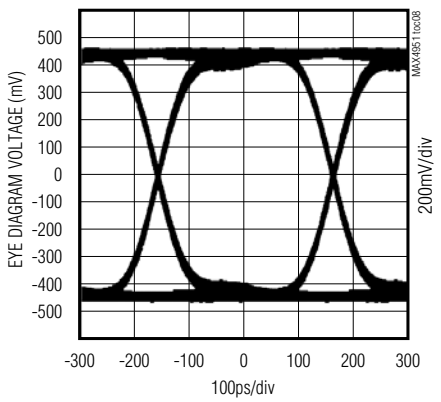
BA = BB = GND EYE DIAGRAM ($V_{RX-DFF-PP}$ = 1600mV$_{P-P}$, 6.0Gbps)



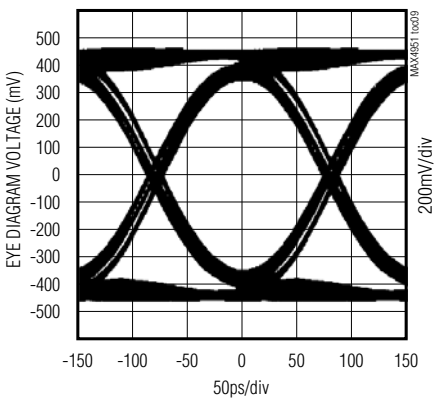
BA = BB = V_{CC} EYE DIAGRAM ($V_{RX-DFF-PP}$ = 220mV$_{P-P}$, 1.5Gbps)



BA = BB = V_{CC} EYE DIAGRAM ($V_{RX-DFF-PP}$ = 220mV$_{P-P}$, 3.0Gbps)



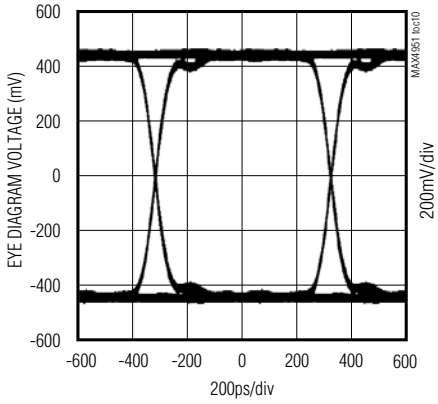
BA = BB = V_{CC} EYE DIAGRAM ($V_{RX-DFF-PP}$ = 220mV$_{P-P}$, 6.0Gbps)



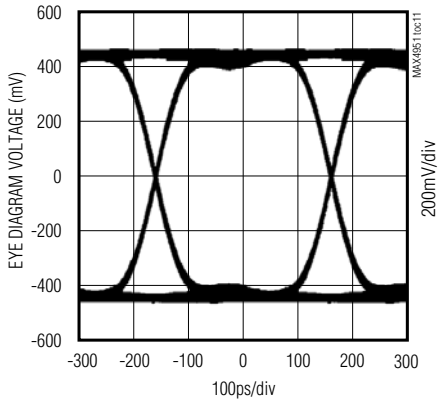
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, all eye diagrams measured using K28.5 pattern.)

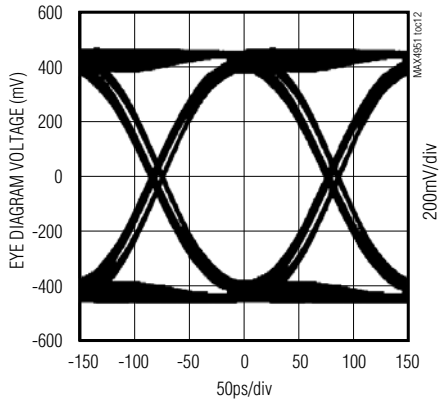
BA = BB = V_{CC} EYE DIAGRAM ($V_{RX-DFF-PP}$ = 1600mV_{P-P}, 1.5Gbps)



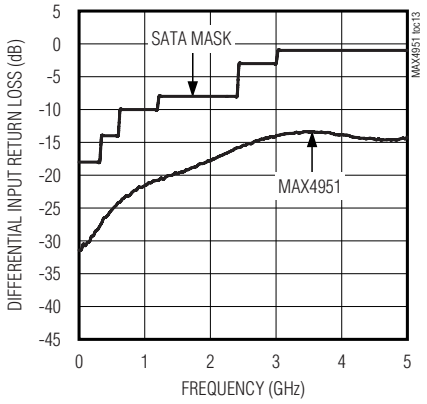
BA = BB = V_{CC} EYE DIAGRAM ($V_{RX-DFF-PP}$ = 1600mV_{P-P}, 3.0Gbps)



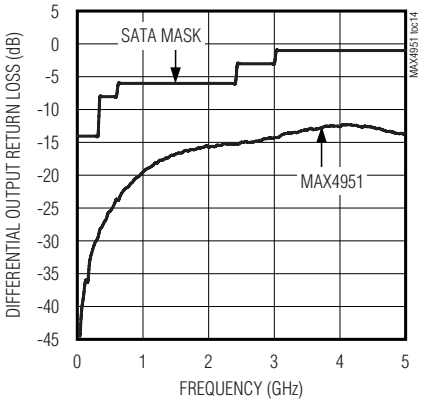
BA = BB = V_{CC} EYE DIAGRAM ($V_{RX-DFF-PP}$ = 1600mV_{P-P}, 6.0Gbps)



DIFFERENTIAL INPUT RETURN LOSS vs. FREQUENCY



DIFFERENTIAL OUTPUT RETURN LOSS vs. FREQUENCY



SATA I/SATA II Bidirectional Re-Driver

Pin Description

PIN	NAME	FUNCTION
1	HAP	Noninverting Input from Host Channel A
2	HAM	Inverting Input from Host Channel A
3, 13, 17, 18, 19	GND	Ground
4	HBM	Inverting Output to Host Channel B
5	HBP	Noninverting Output to Host Channel B
6, 10, 16, 20	V_{CC}	Positive Supply Voltage Input. Bypass V_{CC} to GND with 0.1µF and 0.001µF capacitors in parallel and as close to the device as possible.
7	EN	Active-High Enable Input. Drive EN low to put device in standby mode. Drive EN high for normal operation. EN is internally pulled down.
8	BB	Channel-B Boost Enable Input. Drive BB high to enable channel-B output boost. Drive BB low for standard SATA output level. BB is internally pulled down.
9	BA	Channel-A Boost Enable Input. Drive BA high to enable channel-A output boost. Drive BA low for standard SATA output level. BA is internally pulled down.
11	DBP	Noninverting Input from Device Channel B
12	DBM	Inverting Input from Device Channel B
14	DAM	Inverting Output to Device Channel A
15	DAP	Noninverting Output to Device Channel A
—	EP	Exposed Pad. Internally connected to GND. EP must be electrically connected to a ground plane for proper thermal and electrical operation.

Detailed Description

The MAX4951 consists of two identical buffers that take SATA input signals and return them to full output levels. This device functions up to 6.0Gbps for next-generation SATA applications.

Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to V_{CC} (see the *Functional Diagram/Truth Table*) and must be AC-coupled to the SATA controller IC and SATA device for proper operation.

Out-Of-Band Logic

The MAX4951 provides full Out-Of-Band (OOB) signal support through high-speed amplitude detection circuitry. SATA OOB differential input signals of $50mV_{P-P}$ or less are detected as OFF and not passed to the output. This prevents the system from responding to unwanted noise. SATA OOB differential input signals of $150mV_{P-P}$ or more are detected as ON and passed to the output. This allows OOB signals to transmit through the MAX4951. The time for the amplitude detection circuit to detect an inactive SATA OOB input and squelch the associated output, or detect an active SATA OOB input and enable the output, is less than 5ns.

Enable Input

The MAX4951 features an active-high enable input (EN). EN has an internal pulldown resistor of 70kΩ (typ). When EN is driven low or left unconnected, the MAX4951 enters low-power standby mode and the buffers are disabled. Drive EN high for normal operation.

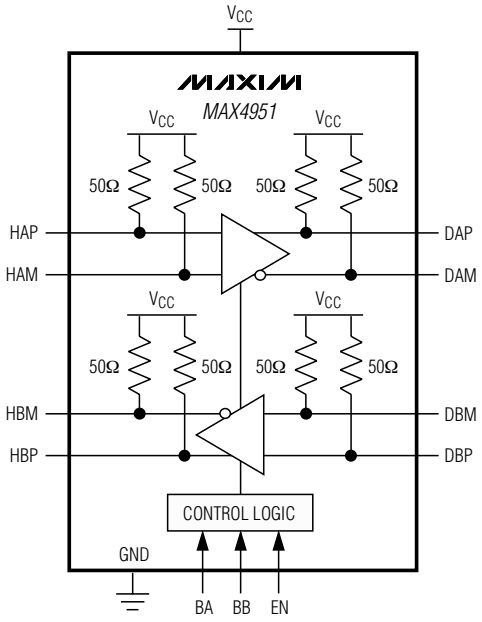
Output Boost Selection Inputs

The MAX4951 has two digital control logic inputs, BA and BB. BA and BB have internal pulldown resistors of 70kΩ (typ). BA and BB control the boost level of their corresponding buffers (see the *Functional Diagram/Truth Table*). Drive BA or BB low or leave unconnected for standard SATA output levels. Drive BA or BB high to boost the output. The boosted output level compensates for attenuation from longer trace-length cables or to meet eSATA specifications.

Applications Information

Figure 1 shows a typical application circuit with the MAX4951 used to drive an eSATA output. The diagram assumes that the MAX4951 is close to the SATA host controller. BB is set low to drive standard SATA levels to the host, and BA is set high to drive eSATA levels to the device. If the MAX4951 is further from the controller, set BB high to compensate for attenuation.

Functional Diagram/Truth Table



MAX4951				
EN	**BA**	**BB**	**CHANNEL A**	**CHANNEL B**
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

X = Don't Care

Exposed-Pad Package

The exposed-pad, 20-pin, TQFN package incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The exposed pad on the MAX4951 must be soldered to GND for proper thermal and electrical performance. For more information on exposed-pad packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Layout

Use controlled-impedance transmission lines to interface with the MAX4951 high-speed inputs and outputs. Place power-supply decoupling capacitors as close as possible to V_{CC}.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply V_{CC} before applying signals, especially if the signal is not current limited.

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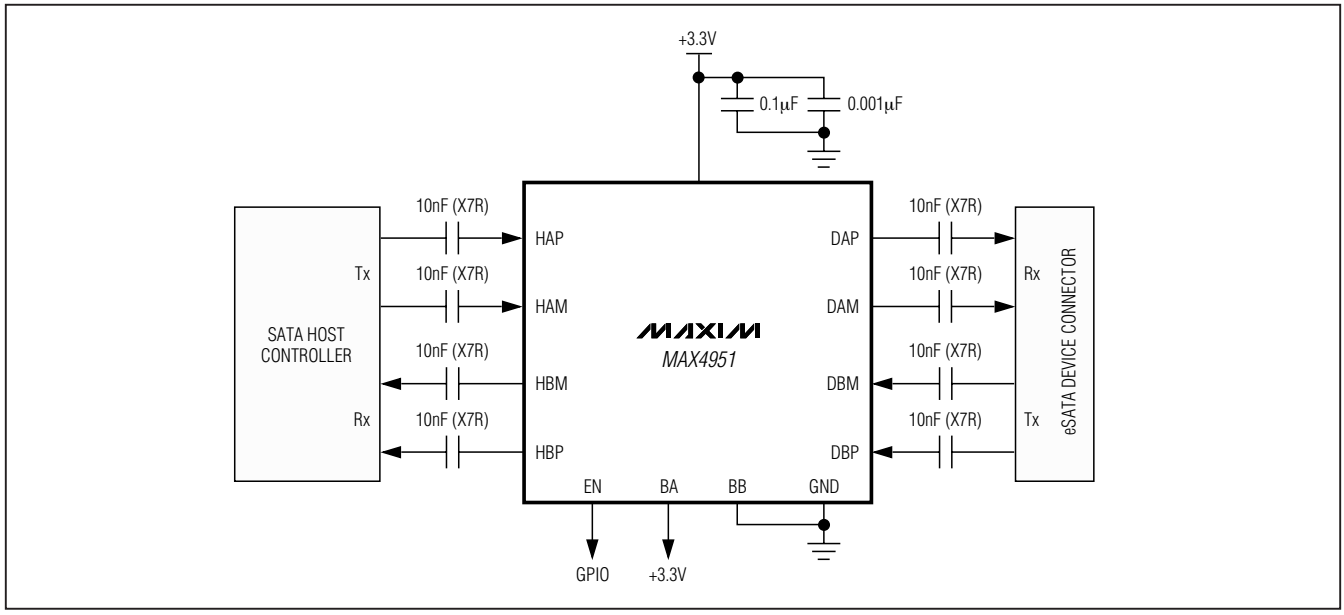

Figure 1. Typical Application Circuit

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN-EP	T2044-2	**21-0139**