WM8593

24-bit 192kHz 2Vrms Multi-Channel CODEC

DESCRIPTION

The WM8593 is a high performance multi-channel audio CODEC with flexible input/output selection and digital and analogue volume control. Features include a 24-bit stereo ADC with digital gain control, two 24-bit DACs with independent volume control and clocking, and a range of input/output channel selection options for flexible routing within current and future audio systems.

The WM8593 has an eight stereo input selector which accepts input levels up to 2Vrms. One stereo input can be routed to the ADC. All inputs can be routed to an output selector.

The output selector inputs two DAC channels and all analogue bypass inputs, and outputs three independent stereo channels at 2Vrms line level. The DAC channels include independent digital volume control, and all three output channels include analogue volume control.

The WM8593 is ideal for audio applications requiring high performance and flexible routing options, including flat panel digital TV and DVD recorder.

The WM8593 supports up to 2Vrms analogue inputs, 2Vrms outputs, with sample rates from 32kHz to 192kHz on the DACs, and 32kHz to 96kHz on the ADC.

The device is controlled via a serial interface with support for 2-wire and 3-wire control with readback. Control of mute, powerdown and reset can also be achieved by pin selection.

The WM8593 is available in a 64-lead TQFP package.

FEATURES

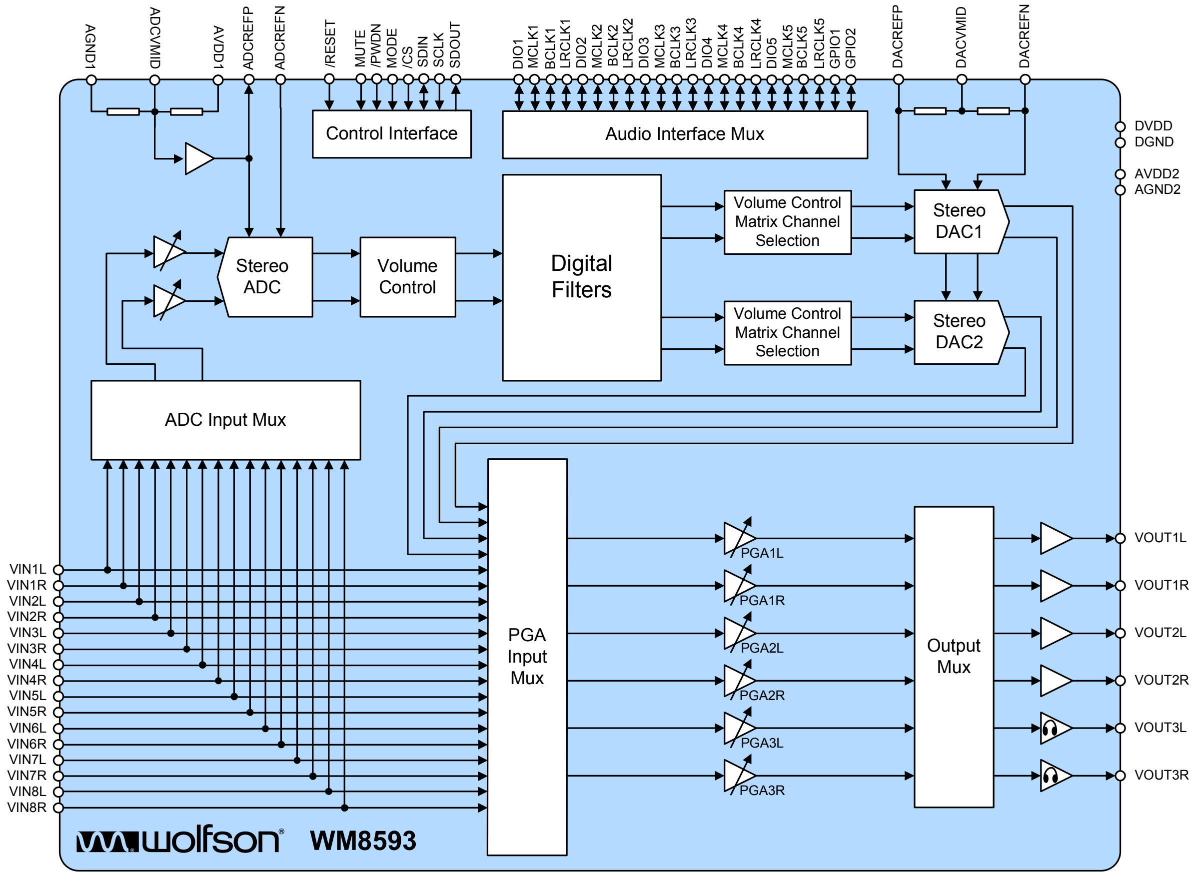
- Multi-channel CODEC with 8 stereo input selector and 3 stereo output selector
- 4-channel DAC, 2-channel ADC
- 8x2Vrms stereo input selector with 8x2 channel analogue bypass to output selector
- 3x2Vrms stereo output selector
- Audio performance
  - DAC: 100dB SNR typical (‘A’ weighted @ 48kHz)
  - DAC: -90dB THD typical
  - ADC: 100dB SNR typical (‘A’ weighted @ 48kHz)
  - ADC: -90dB THD typical
- Independent sampling rate for ADC and DACs
- Independent sampling rate for DAC1 and DAC2
- DACs sampling frequency 32kHz – 192kHz
- ADC sampling frequency 32kHz – 96kHz
- DAC digital volume control +12dB to -100dB in 0.5dB steps
- ADC analogue volume control from +30dB to -97dB in 0.5dB steps
- Output analogue volume control +6dB to -74dB in 0.5dB steps with zero cross or soft ramp to prevent pops and clicks
- Headphone drive capability on one stereo output with jack detect
- Digital multiplexer to interface to multiple digital sources – DSP, HDMI, memory card
- 2-wire and 3-wire serial control interface with readback and hardware reset, mute and powerdown pins
- Independent master or slave clocking modes
- Programmable format audio data interface modes
  - I2S, LJ, RJ, DSP
- 3.3V / 9V Analogue, 3.3V Digital Supply Operation
- 64-lead TQFP package

APPLICATIONS

- Digital Flat Panel TV
- DVD-RW
- Set Top Boxes

WOLFSON MICROELECTRONICS plc Product Preview, January 2007, Rev 1.0

BLOCK DIAGRAM



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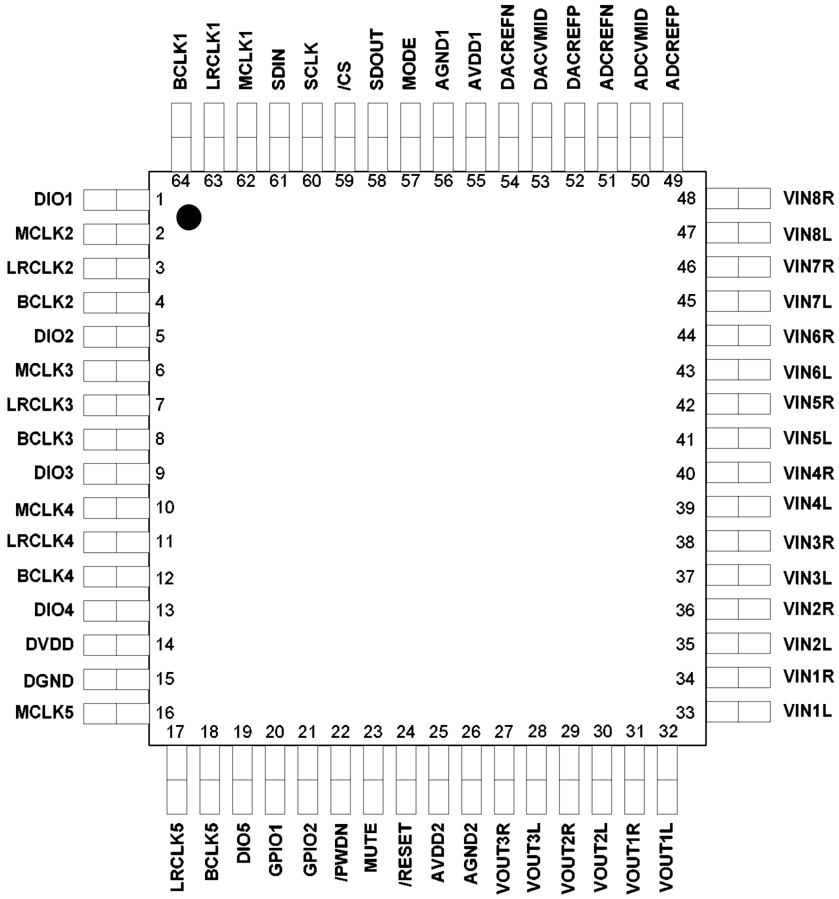
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PACKAGE BODY TEMPERATURE
WM8593SEFT/V	-25°C to +85°C	64-lead TQFP (Pb-free)	MSL3	260°C

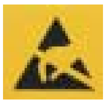
PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DIO1	Digital Input/Output	Audio interface port 1 data input/output
2	MCLK2	Digital Input/Output	Audio interface port 2 master clock input/output
3	LRCLK2	Digital Input/Output	Audio interface port 2 left/right clock input/output
4	BCLK2	Digital Input/Output	Audio interface port 2 bit clock input/output
5	DIO2	Digital Input/Output	Audio interface port 2 data input/output
6	MCLK3	Digital Input/Output	Audio interface port 3 master clock input/output
7	LRCLK3	Digital Input/Output	Audio interface port 3 left/right clock input/output
8	BCLK3	Digital Input/Output	Audio interface port 3 bit clock input/output
9	DIO3	Digital Input/Output	Audio interface port 3 data input/output
10	MCLK4	Digital Input/Output	Audio interface port 4 master clock input/output
11	LRCLK4	Digital Input/Output	Audio interface port 4 left/right clock input/output
12	BCLK4	Digital Input/Output	Audio interface port 4 bit clock input/output
13	DIO4	Digital Input/Output	Audio interface port 4 data input/output
14	DVDD	Supply	Digital supply
15	DGND	Supply	Digital ground
16	MCLK5	Digital Input/Output	Audio interface port 5 master clock input/output
17	LRCLK5	Digital Input/Output	Audio interface port 5 left/right clock input/output
18	BCLK5	Digital Input/Output	Audio interface port 5 bit clock input/output
19	DIO5	Digital Input/Output	Audio interface port 5 data input/output
20	GPIO1	Digital Input/Output	General purpose input/output 1
21	GPIO2	Digital Input/Output	General purpose input/output 2
22	/PWDN	Digital Input	Hardware standby mode
23	MUTE	Digital Input	Hardware DAC mute
24	/RESET	Digital Input	Hardware reset
25	AVDD2	Supply	Analogue 9V supply
26	AGND2	Supply	Analogue ground
27	VOUT3R	Analogue Output	Output selector channel 3 right output
28	VOUT3L	Analogue Output	Output selector channel 3 left output
29	VOUT2R	Analogue Output	Output selector channel 2 right output
30	VOUT2L	Analogue Output	Output selector channel 2 left output
31	VOUT1R	Analogue Output	Output selector channel 1 right output
32	VOUT1L	Analogue Output	Output selector channel 1 left output
33	VIN1L	Analogue Input	Input selector channel 1 left input
34	VIN1R	Analogue Input	Input selector channel 1 right input
35	VIN2L	Analogue Input	Input selector channel 2 left input
36	VIN2R	Analogue Input	Input selector channel 2 right input
37	VIN3L	Analogue Input	Input selector channel 3 left input
38	VIN3R	Analogue Input	Input selector channel 3 right input
39	VIN4L	Analogue Input	Input selector channel 4 left input
40	VIN4R	Analogue Input	Input selector channel 4 right input
41	VIN5L	Analogue Input	Input selector channel 5 left input
42	VIN5R	Analogue Input	Input selector channel 5 right input
43	VIN6L	Analogue Input	Input selector channel 6 left input
44	VIN6R	Analogue Input	Input selector channel 6 right input
45	VIN7L	Analogue Input	Input selector channel 7 left input
46	VIN7R	Analogue Input	Input selector channel 7 right input
47	VIN8L	Analogue Input	Input selector channel 8 left input
48	VIN8R	Analogue Input	Input selector channel 8 right input

PIN	NAME	TYPE	DESCRIPTION
49	ADCREFP	Analogue Output	Positive reference for ADC
50	ADCVMID	Analogue Output	Midrail divider decoupling pin for ADC
51	ADCREFN	Analogue Input	Ground reference for ADC
52	DACREFP	Analogue Input	Positive reference for DACs
53	DACVMID	Analogue Output	Midrail divider decoupling pin for DACs
54	DACREFN	Analogue Input	Ground reference for DACs
55	AVDD1	Supply	Analogue 3.3V supply
56	AGND1	Supply	Analogue ground
57	MODE	Digital Input	2-wire/3-wire mode select
58	SDOUT	Digital Output	Serial Data output for 3-wire readback
59	/CS	Digital Input	3-wire serial control interface latch
60	SCLK	Digital Input	Software mode: serial control interface clock signal
61	SDIN	Digital Input	Software mode: serial control interface data signal
62	MCLK1	Digital Input/Output	Audio interface port 1 master clock input/output
63	LRCLK1	Digital Input/Output	Audio interface port 1 left/right clock input/output
64	BCLK1	Digital Input/Output	Audio interface port 1 bit clock input/output

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage, DVDD	-0.3V	+4.5V
Analogue supply voltage, AVDD1	-0.3V	+7V
Analogue supply voltage, AVDD2	-0.3V	+15V
Voltage range digital inputs	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	TBD	AVDD1 + 2.4V
Master Clock Frequency		38.462MHz
Ambient temperature (supplies applied)	-55°C	+125°C
Storage temperature	-65°C	+150°C
Pb free package body temperature (reflow 10 seconds)		+260°C
Package body temperature (soldering 2 minutes)		+183°C

Note:

1. Analogue and digital grounds must always be within 0.3V of each other.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal resistance – junction to ambient	$R_{\theta JA}$			TBD See note 1		°C/W

Notes:

1. Figure given for package mounted on 4-layer FR4 according to JESD51-7. (No forced air flow is assumed).
2. Thermal performance figures are estimated.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital power supply	DVDD		2.97	3.3	3.6	V
Analogue power supply	AVDD1		2.97	3.3	3.6	V
Analogue power supply	AVDD2		8.1	9	9.9	V
Ground	DGND/AGND1/ AGND2			0		V
Operating temperature range	T_A		-25		+85	°C

Notes:

1. Digital supply (DVDD) must never be more than 0.3V greater than AVDD1 in normal operation.
2. Digital ground (DGND) and analogue grounds (AGND1, AGND2) must never be more than 0.3V apart.

SUPPLY CURRENT CONSUMPTION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply current	I_{DVDD}			TBD		mA
Analogue supply current	I_{AVDD1}			TBD		mA
Analogue supply current	I_{AVDD2}			TBD		mA
Standby current				TBD		µA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, T_A=+25˚C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital logic levels						
Input low level	V_{IL}				0.3xDVDD	V
Input high level	V_{IH}		0.7xDVDD			V
Output low level	V_{OL}				0.1 x DVDD	V
Output high level	V_{OH}		0.9 x DVDD			V
Digital input leakage current				TBD		µA
Digital input capacitance				TBD		pF
Analogue Reference Levels						
ADC Midrail Voltage	ADCVMID			AVDD1/2		V
ADC Buffered Positive Reference Voltage	ADCREFP			ADCVMID		V
DAC Midrail Voltage	DACVMID			DACREFP/2		V
Potential divider resistance		AVDD1 to ADCVMID ADCVMID to AGND1		100		kΩ
		DACVREFP to DACVMID DACVMID to DACVREFN VMID_SEL[1:0] = 01		50 (Note 2)		kΩ
Analogue Line Outputs						
Output signal level (0dB)			TBD	2.0x AVDD2 / 9	TBD	Vrms
Maximum capacitance load					11	nF
Minimum resistance load			1			kΩ
Analogue Headphone Outputs						
Output signal level (0dB)		R_L = 32Ω	TBD	0.8x AVDD2 / 9	TBD	Vrms
Minimum resistance load			16			Ω
Analogue Inputs						

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, T_A=+25˚C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input signal level (0dB)				2.0 x AVDD1/3.3	TBD	Vrms
Input impedance			10	11	12	kΩ
Extended input impedance (Note 3)		External resistor = 10kΩ		21		kΩ
Input capacitance				TBD		pF
DAC Performance						
Signal to Noise Ratio[1,5]	SNR	A-weighted @ fs = 48kHz	TBD	100		dB
		A-weighted @ fs = 96kHz		100		dB
		A-weighted @ fs = 192kHz		100		dB
Dynamic Range[2,5]	DNR	A-weighted, -60dB full scale input	TBD	100		dB
Total Harmonic Distortion[3,5]	THD	1kHz, 0dBFS @ fs = 48kHz		-90	TBD	dB
		1kHz, 0dBFS @ fs = 96kHz		-90		dB
		1kHz, 0dBFS @ fs = 192kHz		-90		dB
Channel Separation[4,5]				100		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Power supply rejection ratio	PSRR	1kHz, 100mVpp	TBD	50		dB
		20Hz to 20kHz, 100mVpp		TBD		dB
ADC Performance						
Signal to Noise Ratio[1,5]	SNR	A-weighted, 0dB gain @ fs = 48kHz	TBD	100		dB
		A-weighted, 0dB gain @ fs = 96kHz		97		dB
Dynamic Range[2,5]	DNR	A-weighted, -60dB full scale input	TBD	100		dB
Total Harmonic Distortion[3,5]	THD	1kHz, -1dBFS @ fs = 48kHz		-90	TBD	dB
		1kHz, -1dBFS @ fs = 96kHz		-87		dB
Channel Separation[4,5]				100		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Power Supply Rejection Ratio	PSRR		TBD	50		dB
				TBD		dB
Analogue Bypass Paths						
Signal to Noise Ratio[1,5]	SNR	A-weighted		100		dB
Dynamic Range[2,5]	DNR	A-weighted		100		dB
Total Harmonic Distortion[3,5]	THD			90		dB
Channel Separation[4,5]				100		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, T_A=+25˚C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Amplifier						
Output signal level (0dB)				0.8		Vrms
Signal to Noise Ratio[1,5]	SNR	A-weighted		TBD		dB
Total Harmonic Distortion	THD	P_O=20mW, R_L=16Ω		TBD		dB
		P_O=20mW, R_L=32Ω		TBD		dB
Channel Separation[4,5]				TBD		dB
Power Supply Rejection Ratio	PSRR			TBD		dB
Digital Volume Control						
ADC minimum digital volume				-97		dB
ADC maximum digital volume				+30		dB
ADC volume step size				0.5		dB
DAC minimum digital volume				-100		dB
DAC maximum digital volume				+12		dB
DAC volume step size				0.5		dB
Analogue Volume Control						
Minimum gain				-73.5		dB
Maximum gain				+6		dB
Step size				0.5		dB
Mute attenuation				TBD		dB
Crosstalk						
DAC to ADC		1kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
		20kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
ADC to DAC		1kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
		20kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB

TERMINOLOGY

1. Signal-to-noise ratio (dBFS) – SNR is the difference in level between a reference full scale output signal and the device output with no signal applied. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dBFS) – DNR is a measure of the difference in level between the highest and lowest components of a signal. Normally a THD measurement at -60dBFS. The measured signal is then corrected by adding 60dB to the result, e.g. THD @ -60dBFS = -30dB, DNR = 90dB.
3. Total Harmonic Distortion (dBFS) – THD is the difference in level between a reference full scale output signal and the first seven odd harmonics of the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the next seven odd harmonics is calculated.
4. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
5. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

Notes:

1. All minimum and maximum values are subject to change.
2. This resistance is selectable using VMID_SEL[1:0] – see Figure 51 for full details.
3. See p95 for details of extended input impedance configuration.

MASTER CLOCK TIMING

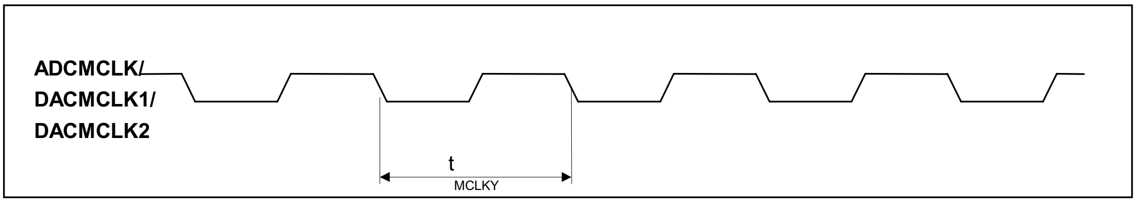


Figure 1 MCLK Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25^{O}C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Master Clock Timing Information					
MCLK System clock cycle time	t_{MCLKY}	27		120	ns
MCLK Duty cycle		40:60		60:40	%
MCLK Period Jitter				200	ps
MCLK Rise/Fall times				10	ns

Table 1 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE TIMING – SLAVE MODE

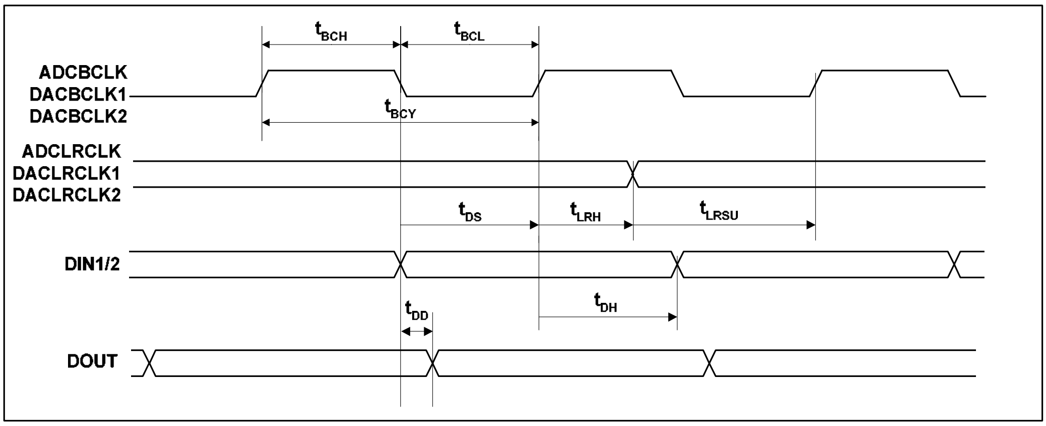


Figure 2 Slave Mode Digital Audio Data Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25˚C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCBCLK / DACBCLK1 / DACBCLK2 cycle time	t_{BCY}	80			ns
ADCBCLK / DACBCLK1 / DACBCLK2 pulse width high	t_{BCH}	30			ns
ADCBCLK / DACBCLK1 / DACBCLK2 pulse width low	t_{BCL}	30			ns
ADCBCLK / DACBCLK1 / DACBCLK2 rise/fall times				5	ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 set-up time to ADCBCLK / DACBCLK1 / DACLRCLK2 rising edge	t_{LRSU}	22			ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 hold time from ADCBCLK / DACBCLK1 / DACBCLK2 rising edge	t_{LRH}	25			ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 rise/fall times				5	ns
DIN1/2 hold time from DACBCLK1 / DACBCLK2 rising edge	t_{DH}	25			ns
DOUT propagation delay from ADCBCLK falling edge	t_{DD}	4		16	ns

Table 2 Slave Mode Audio Interface Timing

DIGITAL AUDIO INTERFACE TIMING – MASTER MODE

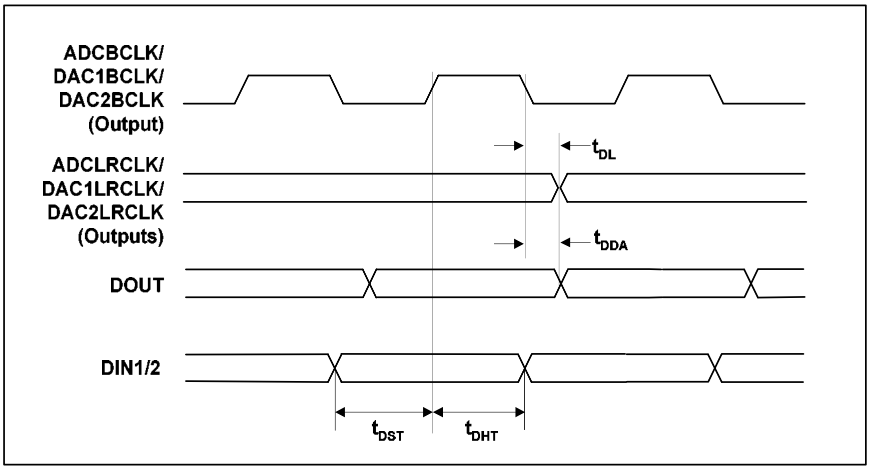


Figure 3 Master Mode Digital Audio Data Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25˚C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCLRCLK / DACLRCLK1 / DACLRCLK2 propagation delay from ADCBCLK / DACBCLK1 / DACLRCLK2 falling edge	t_{DL}	4		16	ns
DOUT propagation delay from ADCBCLK falling edge	t_{DDA}	4		16	ns
DIN1 / DIN2 setup time to DACBCLK1 / DACBCLK2 rising edge	t_{DST}	22			ns
DIN1 / DIN2 hold time to DACBCLK1 / DACBCLK2 rising edge	t_{DHT}	25			ns

Table 3 Master Mode Audio Interface Timing

CONTROL INTERFACE TIMING – 2-WIRE MODE

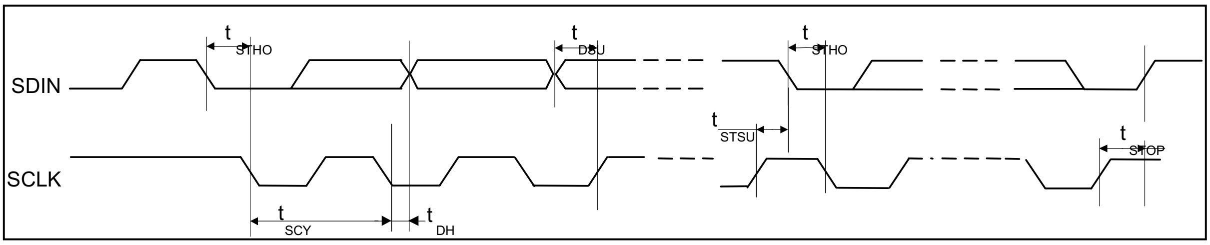


Figure 4 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25˚C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK pulse cycle time	t_{SCY}	2500			ns
SCLK duty cycle		40/60		60/40	%
SCLK frequency				400	kHz
Hold Time (Start Condition)	t_{STHO}	600			ns
Setup Time (Start Condition)	t_{STSU}	600			ns
Data Setup Time	t_{DSU}	100			ns
SDIN, SCLK Rise Time				300	ns
SDIN, SCLK Fall Time				300	ns
Setup Time (Stop Condition)	t_{STOP}	600			ns
Data Hold Time	t_{DHO}			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 4 Control Interface Timing – 2-Wire Serial Control Mode

CONTROL INTERFACE TIMING – 3-WIRE MODE

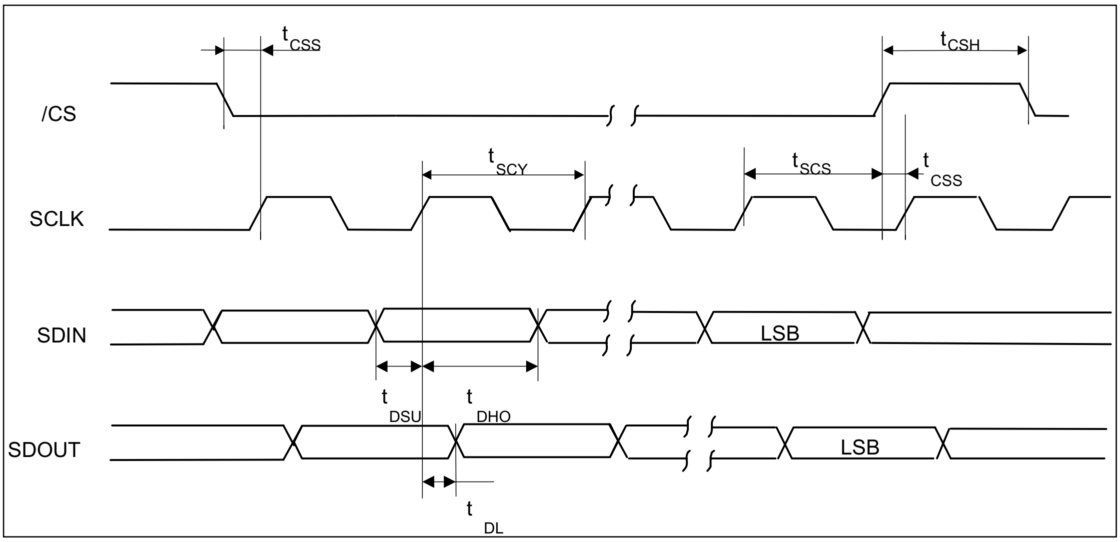


Figure 5 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25˚C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	160			ns
SCLK duty cycle		40/60		60/40	%
SDIN to SCLK set-up time	t_{DSU}	20			ns
SDIN hold time from SCLK rising edge	t_{DHO}	40			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			5	ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising/falling to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 5 Control Interface Timing – 3-Wire Serial Control Mode

POWER ON RESET (POR)

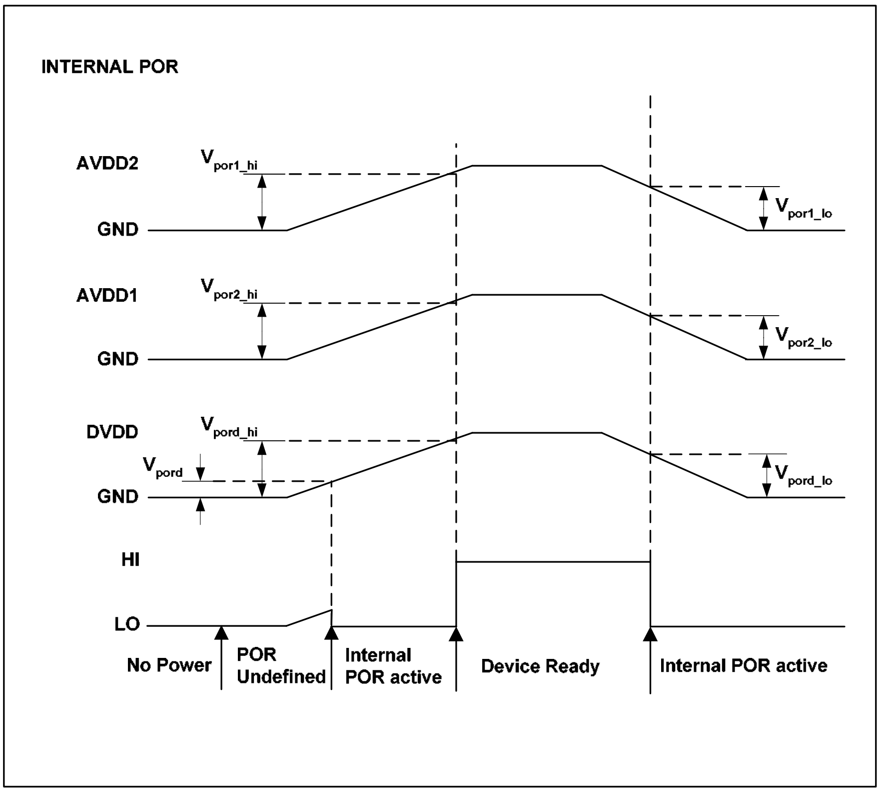


Figure 1 Power Supply Timing Requirements

Test Conditions

DVDD = 3.3V, AVDD1 = 3.3V, AVDD2 = 9V DGND = AGND1 = AGND2 = 0V, T_A = +25°C, T_{A_max} = +125°C, T_{A_min} = -25°C

$AVDD1_{max}$ = $DVDD_{max}$ = 3.63V, $AVDD1_{min}$ = $DVDD_{mim}$= 2.97V

$AVDD2_{max}$ = 9.9V, $AVDD2_{min}$ = 8.1V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (DVDD rising)	V_{pord}	Measured from DGND	0.27	0.36	0.60	V
VDD level to POR rising edge (DVDD rising)	V_{pord_hi}	Measured from DGND	1.34	1.88	2.32	V
VDD level to POR falling edge (DVDD falling)	V_{pord_lo}	Measured from DGND	1.32	1.86	2.30	V
VDD level to POR rising edge (AVDD1 rising)	V_{por1_hi}	Measured from DGND	1.65	1.68	1.85	V
VDD level to POR falling edge (AVDD1 falling)	V_{por1_lo}	Measured from DGND	1.63	1.65	1.83	V
VDD level to POR rising edge (AVDD2 rising)	V_{por2_hi}	Measured from DGND	1.80	1.86	2.04	V
VDD level to POR falling edge (AVDD2 falling)	V_{por2_lo}	Measured from DGND	1.76	1.8	2.02	V

Table 6 Power on Reset

DEVICE DESCRIPTION

INTRODUCTION

The WM8593 is a high performance multi-channel audio CODEC with 2Vrms line level inputs and outputs and flexible analogue and digital input / output switching. The device comprises a 24-bit stereo ADC, two 24-bit stereo DACs with independent sampling rates and digital volume control, a flexible analogue input and output multiplexer and a flexible analogue input and output multiplexer. Analogue inputs and outputs are all at 2Vrms line level, minimising external component count.

The DACs can operate from independent left/right clocks, bit clocks and master clocks with independent data inputs. Alternatively, the DACs can be synchronised to use the same clocks with independent data inputs. Each of the DAC audio interfaces can be configured to operate in ether master or slave clocking modes. In master mode, left/right clocks and bit clocks are all outputs. In slave mode, left/right clocks and bit clocks are all inputs.

The ADC uses a separate left/right clock, bit clock and master clock, allowing independent recording and playback in audio applications. The ADC audio interface can be configured to operate in either master or slave clocking mode. In master mode, left/right clocks and bit clocks are all outputs. In slave mode, left/right clocks and bit clocks are all inputs.

The ADC includes digital gain control, allowing signals to be gained and attenuated between +30dB and -97dB in 0.5dB steps.

The DACs include independent digital volume control, which is adjustable between +12dB and -100 dB in 0.5dB steps. The DACs can be configured to output stereo audio data and a range of mono audio options.

The input analogue multiplexer accepts eight stereo line level inputs at up to 2Vrms. One stereo input can be routed to the ADC, and all eight stereo inputs can be routed to the output multiplexer.

The output analogue multiplexer includes analogue volume control with zero cross, adjustable between +6dB and -73.5dB in 0.5dB steps, and configurable soft ramp rate. Analogue audio is output at 2Vrms line level.

The digital audio interface multiplexer allows flexible routing of the digital signals internal to the device between the independent ADC, DAC1 and DAC2 audio interfaces from any of the five digital audio ports. By integrating this functionality into the WM8593, the external component count and board space normally required to switch between various digital audio sources can be significantly reduced.

Additionally, a jack detect function is included that allows various paths within the device to be muted when a set of headphones is detected.

Control of the internal functionality of the device is by 2-wire or 3-wire serial control interface with readback. The interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally. In addition, control of mute, power-down and reset may also be achieved by pin control.

Operation using system clocks of 128fs, 192fs, 256fs, 384fs, 512fs, 768fs or 1152fs is provided. ADC and DACs may be clocked independently. Sampling rates from 32kHz to 192kHz are supported for both DACs provided the appropriate master clocks are input. Sampling rates from 32kHz to 96kHz are supported for the ADC provided the appropriate master clock is input.

The audio data interface supports right justified, left justified, and I^2S interface formats along with a highly flexible DSP serial port interface format.

CONTROL INTERFACE

Control of the WM8593 is achieved by a 2-wire SM-bus-compliant or 3-wire SPI compliant serial interface with readback. Software interface mode is selected using the MODE pin as shown in Table 7 below:

MODE	INTERFACE FORMAT
Low	2 wire
High	3 wire

Table 7 Control Interface Mode Selection

2-WIRE (SM-BUS COMPATIBLE) SERIAL CONTROL INTERFACE MODE

Many devices can be controlled by the same bus, and each device has a unique 7-bit address.

REGISTER WRITE

The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address and read/write bit, MSB first). If the device address received matches the address of the WM8593, the WM8593 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised, the WM8593 returns to the idle condition and waits for a new start condition with valid address.

When the WM8593 has acknowledged a correct address, the controller sends the first byte of control data (B23 to B16, i.e. the WM8593 register address). The WM8593 then acknowledges the first data byte by pulling SDIN low for one SCLK pulse. The controller then sends a second byte of control data (B15 to B8, i.e. the first 8 bits of register data), and the WM8593 acknowledges again by pulling SDIN low for one SCLK pulse. Finally, the controller sends a third byte of control data (B7 to B0, i.e. the final 8 bits of register data), and the WM8593 acknowledges again by pulling SDIN low for one SCLK pulse.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8593 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the WM8593 reverts to the idle condition.

The WM8593 device address is 34h (0110100) or 36h (0110110), selectable by control of /CS.

/CS (PIN 45)	2-WIRE BUS ADDRESS
0	34h (0110100)
1	36h (0110110)

Table 8 2-Wire Control Interface Bus Address Selection

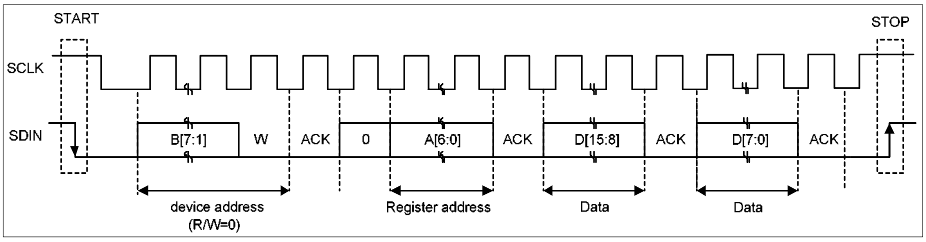


Figure 6 2-Wire Write Protocol

AUTO-INCREMENT REGISTER WRITE

It is possible to write to multiple consecutive registers using the auto-increment feature. When AUTO_INC is set, the register write protocol follows the method shown in Figure 7. As with normal register writes, the controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high, and all devices on the bus receive the device address.

When the WM8593 has acknowledged a correct address, the controller sends the first byte of control data (A6 to A0, i.e. the WM8593 initial register address). The WM8593 then acknowledges the first control data byte by pulling SDIN low for one SCLK pulse. The controller then sends a byte of register data. The WM8593 acknowledges the first byte of register data, auto-increments the register address to be written to, and waits for the next byte of register data. Subsequent bytes of register data can be written to consecutive registers of the WM8593 without setting up the device and register address.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high.

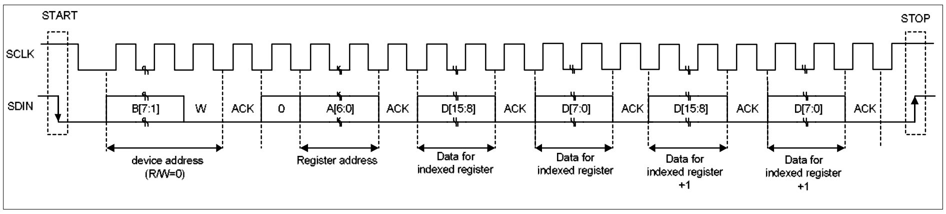


Figure 7 2-Wire Auto-Increment Register Write

REGISTER READBACK

The WM8593 allows readback of all registers with data output on the bidirectional SDIN pin. The protocol is similar to that used to write to the device. The controller will issue the device address followed by a write bit, and the register index will then be passed to the WM8593.

At this point the controller will issue a repeated start condition and resend the device address along with a read bit. The WM8593 will acknowledge this and the WM8593 will become a slave transmitter.

The WM8593 will place the data from the indexed register onto SDIN MSB first. When the controller receives the first byte of data, it acknowledges it. When the controller receives the second and final byte of data it will not acknowledge receipt of the data indicating that it will resume master transmitter control of SDIN. The controller will then issue a stop command completing the read cycle.

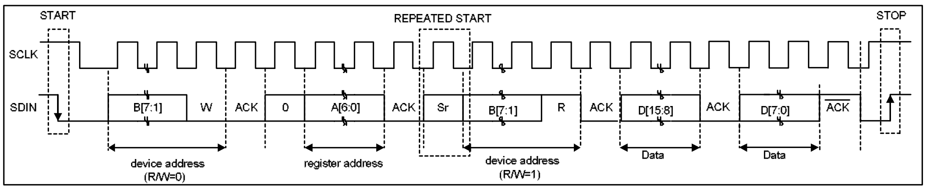


Figure 8 2-wire Read Protocol

AUTO-INCREMENT REGISTER READBACK

It is possible to read from multiple consecutive registers in continuous readback mode. Continuous readback mode is selected by setting AUTO_INC.

In continuous readback mode, the WM8593 will return the indexed register first, followed by consecutive registers in increasing index order until the controller issues a stop sequence.

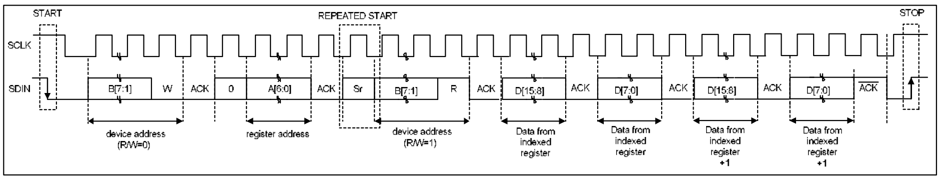


Figure 9 2-Wire Auto-Increment Register Readback

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL INTERFACE MODE

REGISTER WRITE

SDIN is used for the program data, SCLK is used to clock in the program data and /CS is use to latch in the program data. SDIN is sampled on the rising edge of SCLK. The 3-wire interface write protocol is shown in Figure 10.

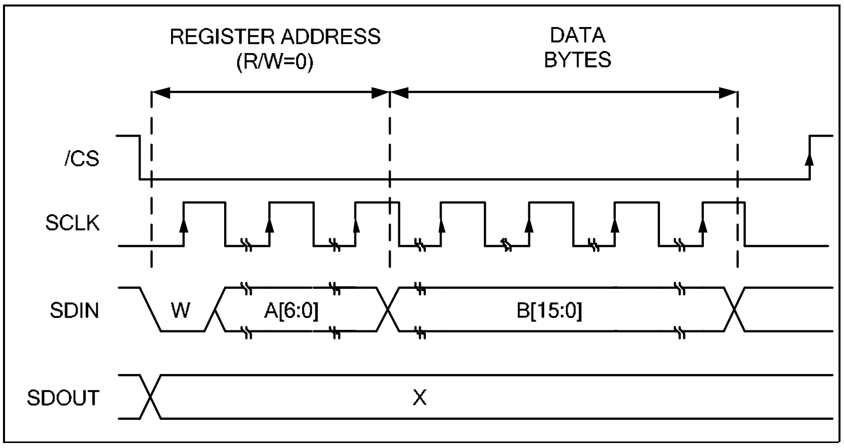


Figure 10 3-Wire Serial Interface Write Protocol

- W indicates write operation.
- A[6:0] is the register index.
- B[15:0] is the data to be written to the register indexed.
- /CS is edge sensitive – the data is latched on the rising edge of /CS.

REGISTER READ-BACK

The read-only status registers can be read back via the SDOUT pin. Read Back is enabled when the R/W bit is high. The data can then be read by writing to the appropriate register address, to which the device will respond with data.

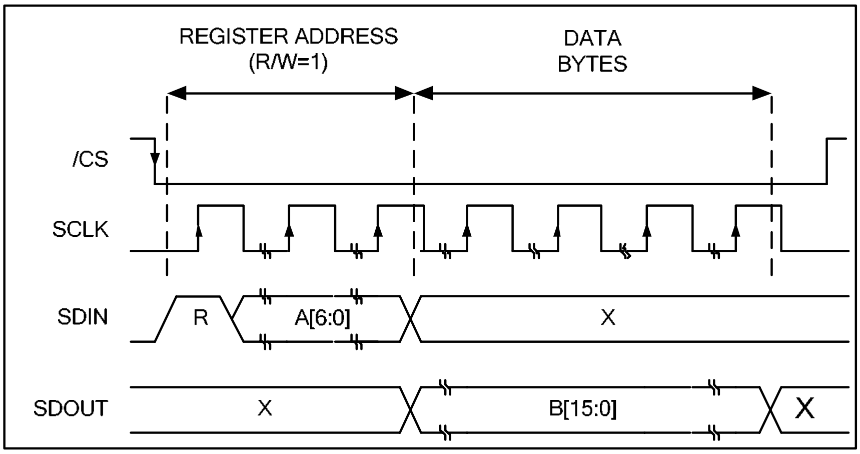


Figure 11 3-Wire Serial Interface Readback Protocol

REGISTER RESET

Any write to register R0 (00h) will reset the WM8593. All register bits are reset to their default values.

DEVICE ID AND REVISION

Reading from register R0 returns the device ID. Reading from register R1 returns the device revision number.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 DEVICE_ID 00h	15:0	DEVICE_ID [15:0]	10000101 10010011	**Device ID** A read of this register will return the device ID, 0x8593.
R1 REVISION 01h	7:0	REVNUM [7:0]	N/A	**Device Revision** A read of this register will return the device revision number. This number is sequentially incremented if the device design is updated.

Table 9 Device ID and Revision Number

GLOBAL ENABLE CONTROL

The WM8593 includes a number of enable and disable mechanisms to allow the device to be powered on and off in a pop-free manner. A global enable control bit enables the ADC, DAC and analogue paths.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 ENABLE 0Ch	0	GLOBAL_ EN	0	**Device Global Enable** 0 = ADC, DAC and PGA ramp control circuitry disabled 1 = ADC, DAC and PGA ramp control circuitry enabled

Table 10 Global Enable Control

DIGITAL AUDIO INTERFACE

Digital audio data is transferred to and from the WM8593 via the digital audio interface. The DACs have independent data inputs and master clocks, bit clocks and left/right frame clocks, and operate in both master or slave mode The ADC has independent master clock, bit clock and left/right frame clock in addition to its data output, and can operate in both master and slave modes.

MASTER MODE

The ADC audio interface requires both a left/right frame clock (ADCLRCLK) and a bit clock (ADCBCLK). These can be supplied externally (slave mode) or they can be generated internally (master mode). Selection of master and slave mode is achieved by setting ADC_MSTR in ADC Control Register 3.

The frequency of ADCLRCLK in master mode is dependent upon the ADC master clock frequency and the ADC_SR[2:0] bits.

The frequency of ADCBCLK in master mode can be selected by ADC_BCLKDIV[1:0].

The DAC audio interfaces require both left/right frame clocks (DACLRCLK1, DACLRCLK2) and bit clocks (DACBCLK1, DACBCLK2). These can be supplied externally (slave mode) or they can be generated internally (master mode). Selection of master and slave mode is achieved by setting DAC1_MSTR in DAC1 Control Register 3 and DAC2_MSTR in DAC2 Control Register 3.

The frequency of DACLRCLK1 in master mode is dependent upon the DAC1 master clock frequency and the DAC1_SR[2:0] bits. Similarly the frequency of DACLRCLK2 in master mode is dependent upon the DAC2 master clock frequency and the DAC2_SR[2:0] bits.

The frequency of DACBCLK1 and DACBCLK2 in master mode can be selected by DAC1_BCLKDIV[1:0] and DAC2_BCLKDIV[1:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 DAC1_CTRL2 03h	2:0	DAC1_ SR[2:0]	000	**DAC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
	5:3	DAC1_ BCLKDIV [2:0]	000	**DAC1 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC1_BCLKDIV[2:0] are reserved
R4 DAC1_CTRL3 04h	0	DAC1_ MSTR	0	**DAC1 Master Mode Select** 0 = Slave mode, DACBCLK1 and DACLRCLK1 are inputs to WM8593 1 = Master mode, DACBCLK1 and DACLRCLK1 are outputs from WM8593
R8 DAC1_CTRL2 08h	2:0	DAC2_ SR[2:0]	000	**DAC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
	5:3	DAC2_ BCLKDIV [2:0]	000	**DAC2 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC2_BCLKDIV[2:0] are reserved
R9 DAC2_CTRL3 09h	0	DAC2_ MSTR	0	**DAC2 Master Mode Select** 0 = Slave mode, DACBCLK2 and DACLRCLK2 are inputs to WM8593 1 = Master mode, DACBCLK2 and DACLRCLK2 are outputs from WM8593
R14 ADC_CTRL2 0Eh	2:0	ADC_ SR[2:0]	000	**ADC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = Reserved
	5:3	ADC_BCLK	000	**ADC BCLK Rate**

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
		DIV[2:0]		000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of ADC_BCLKDIV[2:0] are reserved
R15 ADC_CTRL3 0Fh	0	ADC_ MSTR	0	**ADC Master Mode Select** 0 = Slave mode, ADCBCLK and ADCLRCLK are inputs to WM8593 1 = Master mode, ADCBCLK and ADCLRCLK are outputs from WM8593

Table 11 ADC Master Mode Control

SLAVE MODE

In slave mode, the master clock to left/right clock ratio can be auto-detected or set manually by register write.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 DAC1_CTRL2 03h	2:0	DAC1_ SR[2:0]	000	**DAC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
R8 DAC2_CTRL2 08h	2:0	DAC2_ SR[2:0]	000	
R14 ADC_CTRL2 0Eh	2:0	ADC_ SR[2:0]	000	**ADC MCLK:LRCLK Ratio** 000 = Auto detect 001 = reserved 010 = reserved 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = Reserved

Table 12 Slave Mode MCLK to LRCLK Ratio Control

DIGITAL AUDIO DATA SAMPLING RATES

In a typical digital audio system there is one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's master clock. The WM8593 uses independent master clocks for ADC and DACs. The external master clocks can be applied directly to the ADCMCLK, DACMCLK1 and DACMCLK2 input pins. In a system where there are a number of possible sources for the reference clock, it is recommended that the clock source with the lowest jitter be used for the master clock to optimise the performance of the WM8593.

In slave clocking mode the WM8593 has a master detection circuit that automatically determines the relationship between the master clock frequency (ADCMCLK, DACMCLK1, DACMCLK2) and the sampling rate (ADCLRCLK, DACLRCLK1, DACLRCLK2), to within +/- 32 system clock periods. The master clocks must be synchronised with the left/right clocks, although the device is tolerant of phase variations or jitter on the master clocks.

The ADC supports master clock to sampling clock ratios of 256fs to 768fs and sampling rates of 32kHz to 96kHz, provided the internal signal processing of the ADC is programmed to operate at the correct rate. The DACs support master clock to sampling clock ratios of 128fs to 1152fs and sampling rates of 32kHz to 192kHz, provided the internal signal processing of the DACs is programmed to operate at the correct rate.

Table 13 shows typical master clock frequencies and sampling rates supported by the WM8593 ADC. Table 14 shows typical master clock frequencies and sampling rates supported by the WM8593 DACs.

Sampling Rate (ADCLRCLK)	MASTER CLOCK FREQUENCY (MHZ)			
	256fs	**384fs**	**512fs**	**768fs**
32kHz	8.192	12.288	16.384	24.576
44.1kHz	11.2896	16.9344	22.5792	33.8688
48kHz	12.288	18.432	24.576	36.864
88.2kHz	22.5792	33.8688	Unavailable	Unavailable
96kHz	24.576	Unavailable	Unavailable	Unavailable

Table 13 ADC Master Clock Frequency Versus Sampling Rate

Sampling Rate (DACLRCLK1 DACLRCLK2)	MASTER CLOCK FREQUENCY (MHZ)						
	128fs	**192fs**	**256fs**	**384fs**	**512fs**	**768fs**	**1152fs**
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576	36.864
44.1kHz	Unavailable	8.4672	11.2896	16.9344	22.5792	33.8688	Unavailable
48kHz	Unavailable	9.216	12.288	18.432	24.576	36.864	Unavailable
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 14 DAC Master Clock Frequency Versus Sampling Rate

DIGITAL AUDIO DATA FORMATS

The WM8593 supports a range of common audio interface formats:

- I^2S
- Left Justified (LJ)
- Right Justified (RJ)
- DSP Mode A
- DSP Mode B

All formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit RJ mode, which is not supported.

Audio data for each stereo channel is time multiplexed with the interface's left/right clock indicating whether the left or right channel is present. The left/right clock is also used as a timing reference to indicate the beginning or end of the data words.

In LJ, RJ and I^2S modes, the minimum number of bit clock periods per left/right clock period is two times the selected word length. The left/right clock must be high for a minimum of bit clock periods equivalent to the word length, and low for the same period. For example, for a word length of 24 bits, the left/right clock must be high for a minimum of 24 bit clock periods and low for a minimum of 24 bit clock periods. Any mark to space ratio is acceptable for the left/right clock provided these requirements are met.

In DSP modes A and B, left and right channels must be time multiplexed and input on DIN1. LRCLK is used as a frame synchronisation signal to identify the MSB of the first input word. The minimum number of bit clock periods per left/right clock period is two times the selected word length. Any mark to space ratio is acceptable for the left/right clock provided the rising edge is correctly positioned.

I2S MODE

In I^2S mode, the MSB of input data is sampled on the second rising edge of bit clock following a left/right clock transition. The MSB of output data changes on the first falling edge of bit clock following a left/right clock transition, and may be sampled on the next rising edge of bit clock. Left/right clocks are low during the left channel audio data samples and high during the right channel audio data samples.

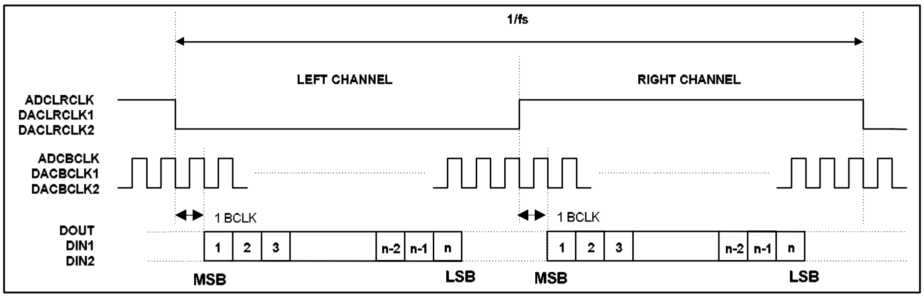


Figure 12 I2S Mode Timing

LEFT JUSTIFIED (LJ) MODE

In LJ mode, the MSB of the input data is sampled by the WM8593 on the first rising edge of bit clock following a left/right clock transition. The MSB of output data changes on the same falling edge of bit clock as left/right clock and may be sampled on the next rising edge of bit clock. Left/right clock is high during the left channel audio data samples and low during the right channel audio data samples.

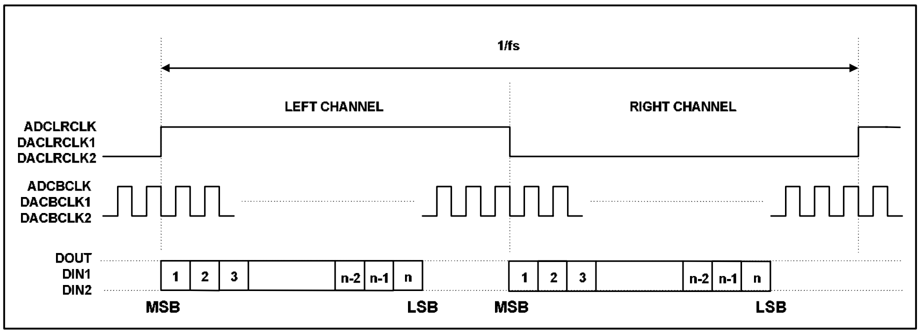


Figure 13 LJ Mode Timing

RIGHT JUSTIFIED (RJ) MODE

In RJ mode the LSB of input data is sampled on the rising edge of bit clock preceding a left/right clock transition. The LSB of output data changes on the falling edge of bit clock preceding a left/right clock transition, and may be sampled on the next rising edge of bit clock. Left/right clock is high during the left channel audio data samples and low during the right channel audio data samples.

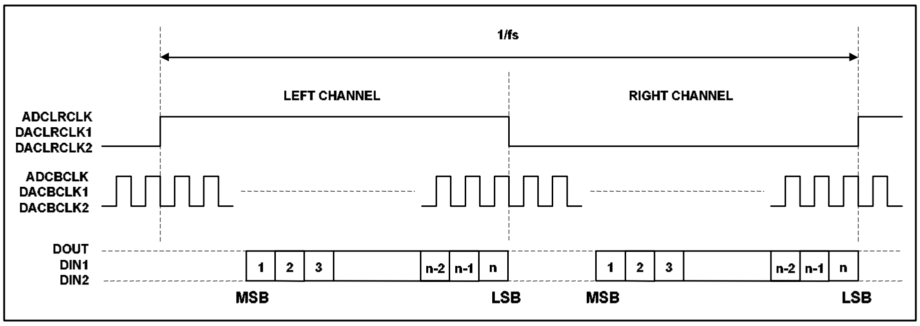


Figure 14 RJ Mode Timing

DSP MODE A

In DSP Mode A, the MSB of channel 1 left data input is sampled on the second rising edge of bit clock following a left/right clock rising edge. Channel 1 right data then follows. The MSB of output data changes on the first falling edge of bit clock following a left/right clock transition and may be sampled on the rising edge of bit clock. The right channel data is contiguous with the left channel data.

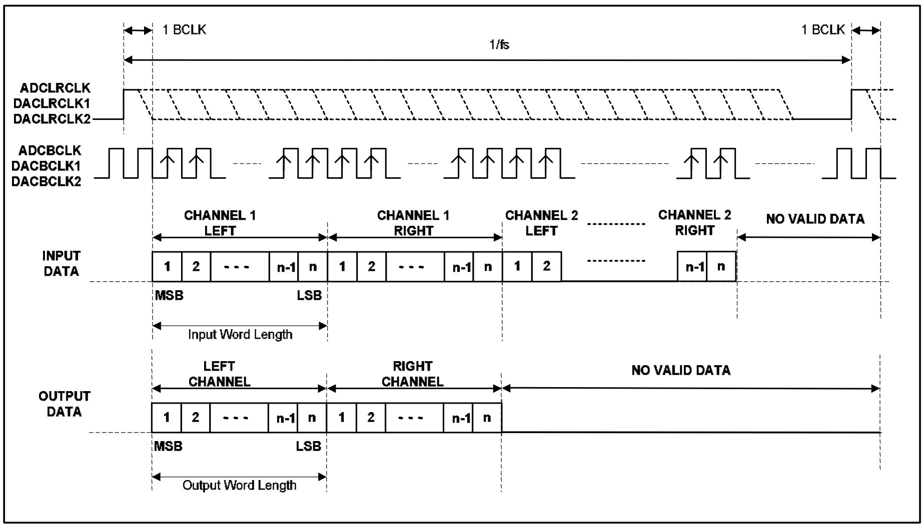


Figure 15 DSP Mode A Timing

DSP MODE B

In DSP Mode B, the MSB of channel 1 left data input is sampled on the first bit clock rising edge following a left/right clock rising edge. Channel 1 right data then follows. The MSB of output data changes on the same falling edge of BCLK as the low to high left/right clock transition and may be sampled on the rising edge of bit clock. The right channel data is contiguous with the left channel data.

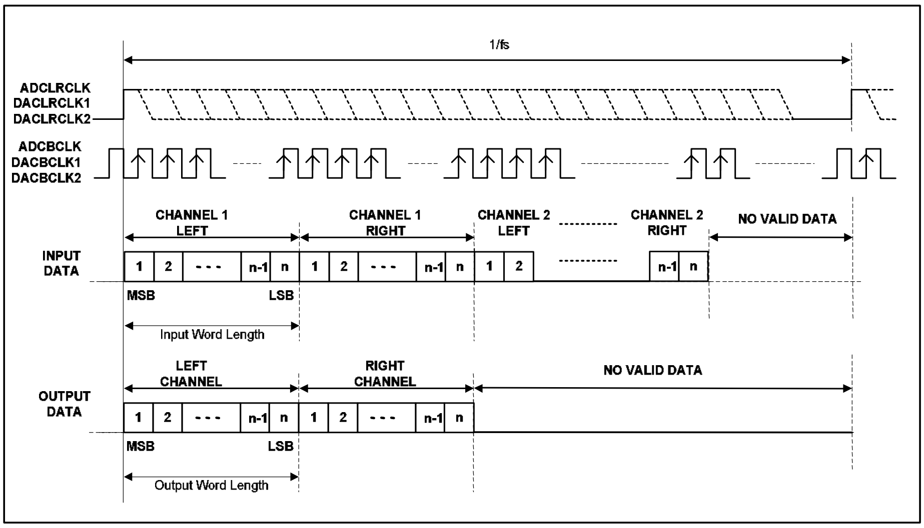


Figure 16 DSP Mode B Timing

DIGITAL AUDIO INTERFACE CONTROL

The control of the audio interface formats is achieved by register write. Dynamically changing the audio data format may cause erroneous operation and is not recommended.

Interface timing is such that the input data and left/right clock are sampled on the rising edge of the interface bit clock. Output data changes on the falling edge of the interface bit clock. By setting the appropriate bit clock and left/right clock polarity bits, the WM8593 ADC and DACs can sample data on the opposite clock edges.

The control of audio interface formats and clock polarities is summarised in Table 15.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	1:0	DAC1_ FMT[1:0]	10	**DAC1 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	DAC1_ WL[1:0]	10	**DAC1 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	DAC1_BCP	0	**DAC1 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
	5	DAC1_LRP	0	**DAC1 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
R7 DAC2_CTRL1 07h	1:0	DAC2_ FMT[1:0]	10	**DAC2 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	DAC2_ WL[1:0]	10	**DAC2 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	DAC2_BCP	0	**DAC2 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
	5	DAC2_LRP	0	**DAC2 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
R13 ADC_CTRL1 0Dh	1:0	ADC_ FMT[1:0]	10	**ADC Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:2	ADC_ WL[1:0]	10	**ADC Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	ADC_BCP	0	**ADC BCLK Polarity** 0 = ADCBCLK not inverted - data latched on rising edge of BCLK 1 = ADCBCLK inverted - data latched on falling edge of BCLK
	5	ADC_LRP	0	**ADC LRCLK Polarity** 0 = ADCLRCLK not inverted 1 = ADCLRCLK inverted

Table 15 Audio Interface Control

DAC FEATURES

The WM8593 includes two 24-bit DACs with independent clocks and independent data inputs. The DACs include digital volume control with zero cross and soft mute, de-emphasis support, and the capability to select the output channels to be stereo or a range of mono options. The DACs are enabled by writing to DAC1_EN and DAC2_EN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	8	DAC1_EN	0	**DAC1 Enable** 0 = DAC disabled 1 = DAC enabled
R7 DAC2_CTRL1 07h	8	DAC2_EN	0	**DAC2 Enable** 0 = DAC2 disabled 1 = DAC2 enabled

Table 16 DAC Enable Control

DIGITAL VOLUME CONTROL

The WM8593 DACs include independent digital volume control, allowing the digital gain to be adjusted between -100dB and +12dB in 0.5dB steps. All four DAC channels can be controlled independently. Alternatively, global update bits allow the user to write all volume changes before the volume is updated.

Volume control includes optional zero cross functionality. When zero cross is enabled, volume changes are not applied until the output level crosses VMID. Zero cross helps to prevent pop and click noise when changing volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 DAC1L_VOL 05h	7:0	DAC1L _VOL[7:0]	11001000	**DAC Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
R6 DAC1R_VOL 06h	7:0	DAC1R _VOL[7:0]		
R10 DAC2L_VOL 0Ah	7:0	DAC2L _VOL[7:0]		

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 DAC2R_VOL 0Bh	7:0	DAC2R _VOL[7:0]		
R5 DAC1L_VOL 05h	8	DAC1L_VU	0	**DAC Digital Volume Update** 0 = Latch DAC volume setting into Register Map but do not update volume 1 = Latch DAC volume setting into Register Map and update left and right channels simultaneously
R6 DAC1R_VOL 06h	8	DAC1R_VU		
R10 DAC2L_VOL 0Ah	8	DAC2L_VU		
R11 DAC2R_VOL 0Bh	8	DAC2R_VU		
R2 DAC1_CTRL1 02h	7	DAC1 _ZCEN	1	**DAC Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross
R7 DAC2_CTRL1 07h	7	DAC2 _ZCEN		

Table 17 DAC Digital Volume Control

SOFTMUTE

A soft mute can be applied to DAC1 and DAC2 independently.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	9	DAC1_ MUTE	0	**DAC Softmute** 0 = Normal operation 1 = Softmute applied
R7 DAC2_CTRL1 07h	9	DAC2_ MUTE	0	

Table 18 DAC Softmute Control

DIGITAL MONOMIX CONTROL

Each DAC can be independently set to output a range of mono and stereo options. Each DAC output channel can output left channel data, right channel data or a mix of left and right channel data.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	11:10	DAC1_OP _MUX[1:0]	00	**DAC1 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to DAC1R) 10 = Mono (Right data to DAC1L) 11 = Digital Monomix, (L+R)/2
R7 DAC2_CTRL1 07h	11:10	DAC2_OP _MUX[1:0]	00	**DAC2 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to DAC2R) 10 = Mono (Right data to DAC2L) 11 = Digital Monomix, (L+R)/2

Table 19 Digital Monomix Control

DE-EMPHASIS

A digital de-emphasis filter may be applied to the DAC outputs when the sampling frequency is 44.1kHz. The de-emphasis filter for each DAC can be applied independently. The deemphasis filter responses and error can be seen in Figure 67 and Figure 68.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	6	DAC1 _DEEMPH	0	**DAC1 De-emphasis** 0 = No de-emphasis 1 = Apply 44.1kHz de-emphasis
R7 DAC2_CTRL1 07h	6	DAC2 _DEEMPH	0	**DAC2 De-emphasis** 0 = No de-emphasis 1 = Apply 44.1kHz de-emphasis

Table 20 De-emphasis Control

ADC FEATURES

The WM8593 features a stereo 24-bit sigma-delta ADC, digital volume control with zero cross, a selectable high pass filter to remove DC offsets, and support for both master and slave clocking modes.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 ADC_CTRL1 0Dh	6	ADC_EN	0	**ADC Enable** 0 = ADC disabled 1 = ADC enabled

Table 21 ADC Enable Control

DIGITAL VOLUME CONTROL

The ADC digital volume can be adjusted between +30dB and -97dB in 0.5dB steps. Left and right channels can be controlled independently. Volume changes can be applied immediately to each channel, or volume changes can be written to both channels before writing to an update bit in order to change the volume in both channels simultaneously.

Volume control includes optional zero cross functionality. When zero cross is enabled, volume changes are not applied until the output level crosses the DC level of the ADC output. Zero cross helps to prevent pop and click noise when changing volume settings.

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>R16
ADCL_VOL
10h</td><td>7:0</td><td>ADCL
_VOL[7:0]</td><td>11000011</td><td rowspan="2">ADC Digital Volume
0000 0000 = Digital mute
0000 0001 = -97dB
0000 0010 = -96.5dB
…0.5dB steps
1100 0011 = 0dB
…0.5dB steps
1111 1110 = +29.5dB
1111 1111 = +30dB</td></tr>
<tr><td>R17
ADCR_VOL
11h</td><td>7:0</td><td>ADCR
_VOL[7:0]</td><td>11000011</td></tr>
<tr><td>R16
ADCL_VOL
10h</td><td>8</td><td>ADCL_VU</td><td>0</td><td rowspan="2">ADC Digital Volume Update
0 = Latch ADC volume setting into Register Map but do not update volume
1 = Latch ADC volume setting into Register Map and update left and right channels simultaneously</td></tr>
<tr><td>R17
ADCR_VOL
11h</td><td>8</td><td>ADCR_VU</td><td>0</td></tr>
</table>

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 ADC_CTRL1 0Dh	13	ADC_ZC_EN	1	**ADC Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross, change volume instantly 1 = Use zero cross, change volume when data crosses zero

Table 22 ADC Digital Volume Control

CHANNEL SWAP AND INVERSION

The WM8593 ADC input channels can be inverted and swapped in a number of ways to provide maximum flexibility of input path to the ADC. The default configuration provides stereo output data with the left and right channel data in the left and right channels. It is possible to swap the left and right channels, invert them independently, or select the same data from both channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 ADC_CTRL1 0Dh	7	ADC_LRSWAP	0	**ADC Left/Right Swap** 0 = Normal 1 = Swap left channel data into right channel and vice-versa
	8	ADCR_INV	0	**ADCL and ADCR Output Signal Inversion** 0 = Output not inverted 1 = Output inverted
	9	ADCL_INV	0	
	11:10	ADC_DATA_SEL[1:0]	00	**ADC Data Output Select** 00 = left data from ADCL, right data from ADCR 01 = left data from ADCL, right data from ADCL 10 = left data from ADCR, right data from ADCR 11 = left data from ADCR, right data from ADCL

Table 23 ADC Channel Swap Control

HIGH PASS FILTER

The WM8593 includes a high pass filter to remove DC offsets. The high pass filter response is shown on page 93. It is possible to disable the high pass filter by writing to ADC_HPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 ADC_CTRL1 0Dh	12	ADC_HPD	0	**ADC High Pass Filter Disable** 0 = High pass filter enabled 1 = High pass filter disabled

Table 24 High Pass Filter Disable Control

ANALOGUE ROUTING CONTROL

The WM8593 has a number of analogue paths, allowing flexible routing of a number of analogue input signals and DAC output signals at levels up to 2Vrms. The analogue paths include volume control with zero cross, optional soft ramp and soft mute, and flexible routing of analogue inputs and DAC outputs to analogue outputs.

There are a total of 16 (eight stereo) analogue input channels and four (two stereo) DAC output channels. Any two of the sixteen input channels can be routed to the ADC. Any six of the 20 total channels can be routed to the analogue outputs.

Figure 17 illustrates the various blocks of the analogue routing paths within the WM8593. The following sections describe the control bits associated with the WM8593 analogue paths. Figure 17 also shows where these control bits take affect on the WM8593.

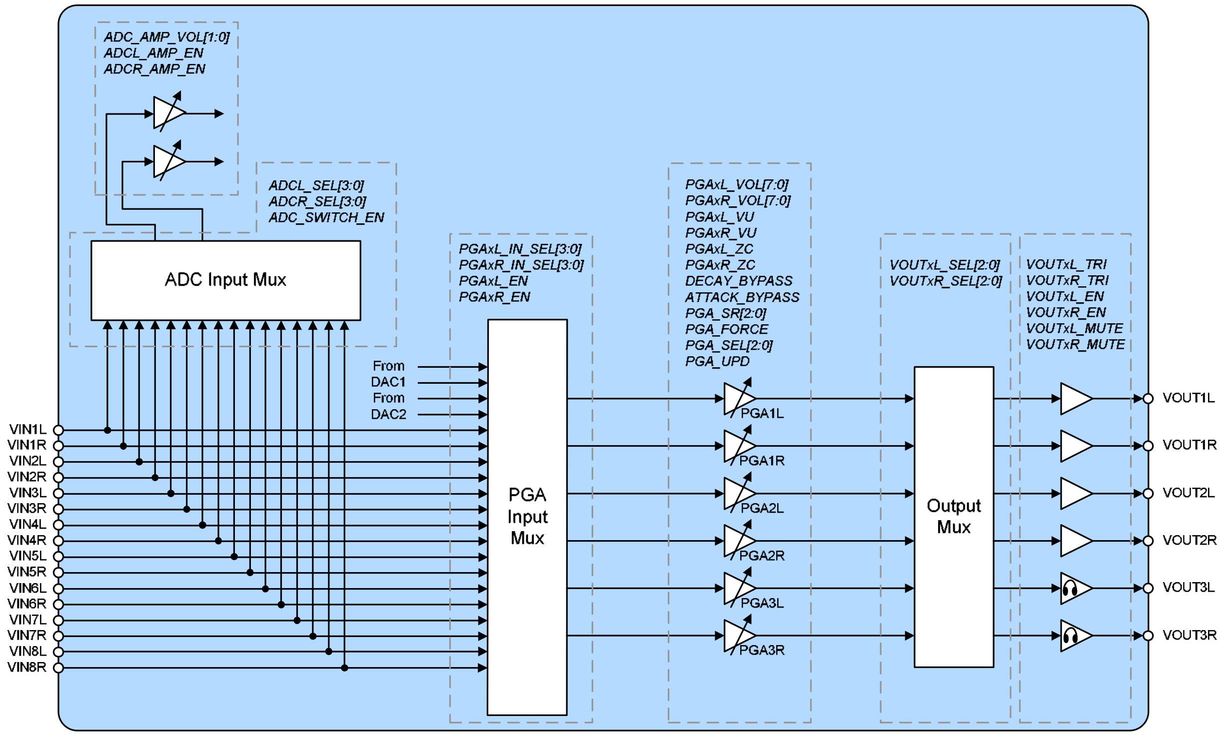


Figure 17 Analogue Routing Paths and Control

ANALOGUE VOLUME CONTROL

Each analogue bypass channel includes analogue volume control. Volume changes can be applied to each channel immediately as they are written. Alternatively, all volume changes can be written, and then all volume changes can be applied simultaneously using the volume update feature.

Volume control includes optional zero cross functionality. When zero cross is enabled, volume changes are not applied until the output level crosses the DC level of the analogue channel (VMID). Zero cross helps to prevent pop and click noise when changing volume settings.

The zero cross function includes a timeout which forces volume changes if a zero cross event does not occur. The timeout period is a maximum of 278ms.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 PGA1L_VOL 13h	7:0	PGA1L_ VOL[7:0]	00001100	**Input PGA Volume** 0000 0000 = +6dB 0000 0001 = +5.5dB …0.5dB steps 00001100 = 0dB … 1001 1110 = -73.5dB 1001 1111 = PGA Mute
R20 PGA1R_VOL 14h	7:0	PGA1R_ VOL[7:0]		
R21 PGA2L_VOL 15h	7:0	PGA2L_ VOL[7:0]		
R22 PGA2R_VOL 16h	7:0	PGA2R_ VOL[7:0]		

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 PGA3L_VOL 17h	7:0	PGA3L_ VOL[7:0]		
R24 PGA3R_VOL 18h	7:0	PGA3R_ VOL[7:0]		
R19 PGA1L_VOL 13h	8	PGA1L_ VU	0	**Input PGA Volume Update** 0 = Latch corresponding volume setting into Register Map but do not update volume 1 = Latch corresponding volume setting into Register Map and update all channels simultaneously
R20 PGA1R_VOL 14h	8	PGA1R_ VU		
R21 PGA2L_VOL 15h	8	PGA2L_ VU		
R22 PGA2R_VOL 16h	8	PGA2R_ VU		
R23 PGA3L_VOL 17h	8	PGA3L_ VU		
R24 PGA3R_VOL 18h	8	PGA3R_ VU		
R25 PGA_CTRL1 19h	2	PGA1L_ ZC	1	PGA Gain Zero Cross Enable 0 = PGA gain updates occur immediately 1 = PGA gain updates occur on zero cross
	3	PGA1R_ ZC		
	4	PGA1L_ ZC		
	5	PGA1R_ ZC		
	6	PGA1L_ ZC		
	7	PGA1R_ ZC		

Table 25 Analogue Volume Control

VOLUME RAMP

Analogue volume can be adjusted by step change or by soft ramp. The ramp rate is dependent upon the sampling rate. The sampling rate upon which the volume ramp rate is based can be selected between the DAC sampling rate or the ADC sampling rate in either slave mode or master mode. The ramp rates for common audio sample rates are shown in Table 26:

SAMPLE RATE FOR PGA (kHz)	DIVIDE BY	PGA RAMP RATE (ms/dB)
32	8	0.50
44.1	8	0.36
48	8	0.33
88.2	16	0.36
96	16	0.33
176.4	32	0.36
192	32	0.33

Table 26 Analogue Volume Ramp Rate

For example, when using a sample rate of 48kHz, the time taken for a volume change from and initial setting of 0dB to -20dB is calculated as follows:

Volume Change (dB) x PGA Ramp Rate (ms/dB) = 20 x 0.33 = 6.6ms

When changing from one PGA ramp clock source to another, it is recommended that PGA_SAFE_SW is set to 0. This forces the clock switch over to occur at a point where all relevant clock signals are zero, ensuring glitch-free operation. This process can take up to 32 left/right clock cycles.

If a faster change in PGA ramp rate clock source is required, PGA_FORCE can be set to 1. This forces the change in clock source to occur immediately regardless of the state of the relevant clock signals internally. Glitch-free operation is not guaranteed under these conditions. PGA_FORCE must be set back to 0 to initialise the timing circuits with the new clock.

If the volume ramp function is not required when increasing or decreasing volume, this block can be bypassed by setting ATTACK_BYPASS or DECAY_BYPASS to 1. Figure 18 shows the effect of these register settings:

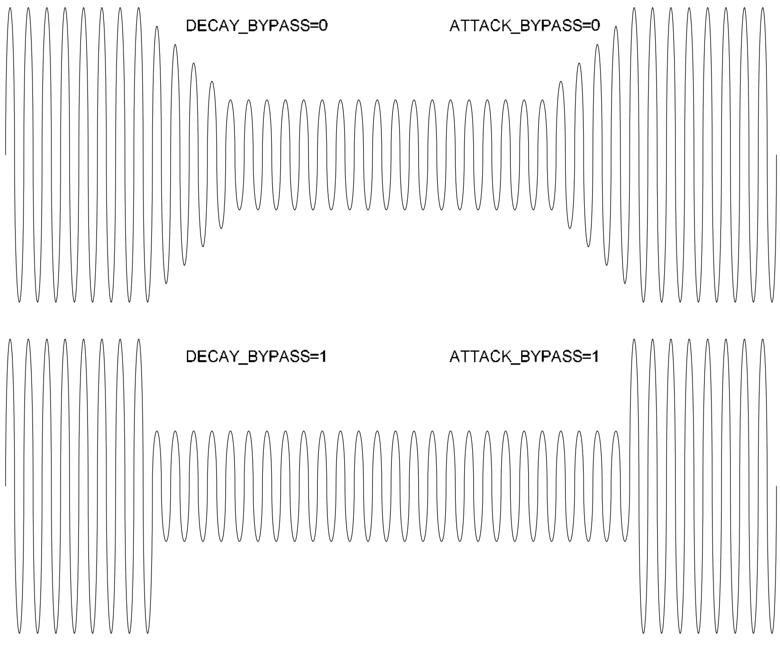


Figure 18 ATTACK_BYPASS and DECAY_BYPASS Functionality

Note: When ATTACK_BYPASS=1 or DECAY_BYPASS=1, it is recommended that the zero cross function for the PGA is used to eliminate click noise when changing volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 PGA_CTRL1 19h	0	DECAY_ BYPASS	0	**PGA Gain Decay Mode** 0 = PGA gain will ramp down 1 = PGA gain will step down
	1	ATTACK_ BYPASS	0	**PGA Gain Attack Mode** 0 = PGA gain will ramp up 1 = PGA gain will step up
R27 ADD_CTRL1 1Bh	6:4	PGA_ SR[2:0]	001	**Sample Rate for PGA** 000 = 32kHz 001 = 44.1kHz 010 = 48kHz 011 = 88.2kHz 100 = 96kHz 101 = 176.4kHz 11X = 192kHz See Table 26 for further information on PGA sample rate versus volume ramp rate.
R36 PGA_CTRL3 24h	0	PGA_ FORCE	0	**PGA Ramp Control Clock Source Mux Force Update** 0 = Wait until clocks are safe before switching PGA clock source 1 = Force PGA clock source to change immediately
	3:1	PGA_ SEL[2:0]	000	**PGA Ramp Control Clock Source** 000 = LRCLK1 001 = LRCLK2 010 = LRCLK3 011 = LRCLK4 100 = LRCLK5 101 = DACLRCLK1 (when DAC1 is being used in master mode) 110 = DACLRCLK2 (when DAC2 is being used in master mode) 111 = ADCLRCLK (when ADC is being used in master mode)
	10	PGA_UPD	0	**PGA Ramp Control Clock Source Mux Update** 0 = Do not update PGA clock source 1 = Update clock source

Table 27 Analogue Volume Ramp Control

ANALOGUE MUTE CONTROL

The analogue channel output drivers can be muted independently and are muted by default. Alternatively, all mute bits can be set using a master mute bit, MUTE_ALL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 PGA_CTRL2 1Ah	0	MUTE_ ALL	0	**Master Output Driver Mute Control** 0 = Unmute all Output Drivers 1 = Mute all Output Drivers
	1	VOUT1L_ MUTE	1	**Individual Output Driver Mute Control** 0 = Unmute Output Driver 1 = Mute Output Driver
	2	VOUT1R_ MUTE	1	
	3	VOUT2L_ MUTE	1	
	4	VOUT2R_ MUTE	1	
	5	VOUT3L_ MUTE	1	
	6	VOUT3R_ MUTE	1	

Table 28 Analogue Mute Control

INPUT SELECTOR CONTROL

Each left channel input PGA can select between all left channel analogue inputs, and both left and right DAC inputs. Each right channel input PGA can select between all right channel analogue inputs, and both left and right DAC inputs. All PGAs can be enabled and disabled independently.

Note: It is recommended to mute the PGA before changing the input to the PGA to avoid pop/click noises when selecting a different input source.

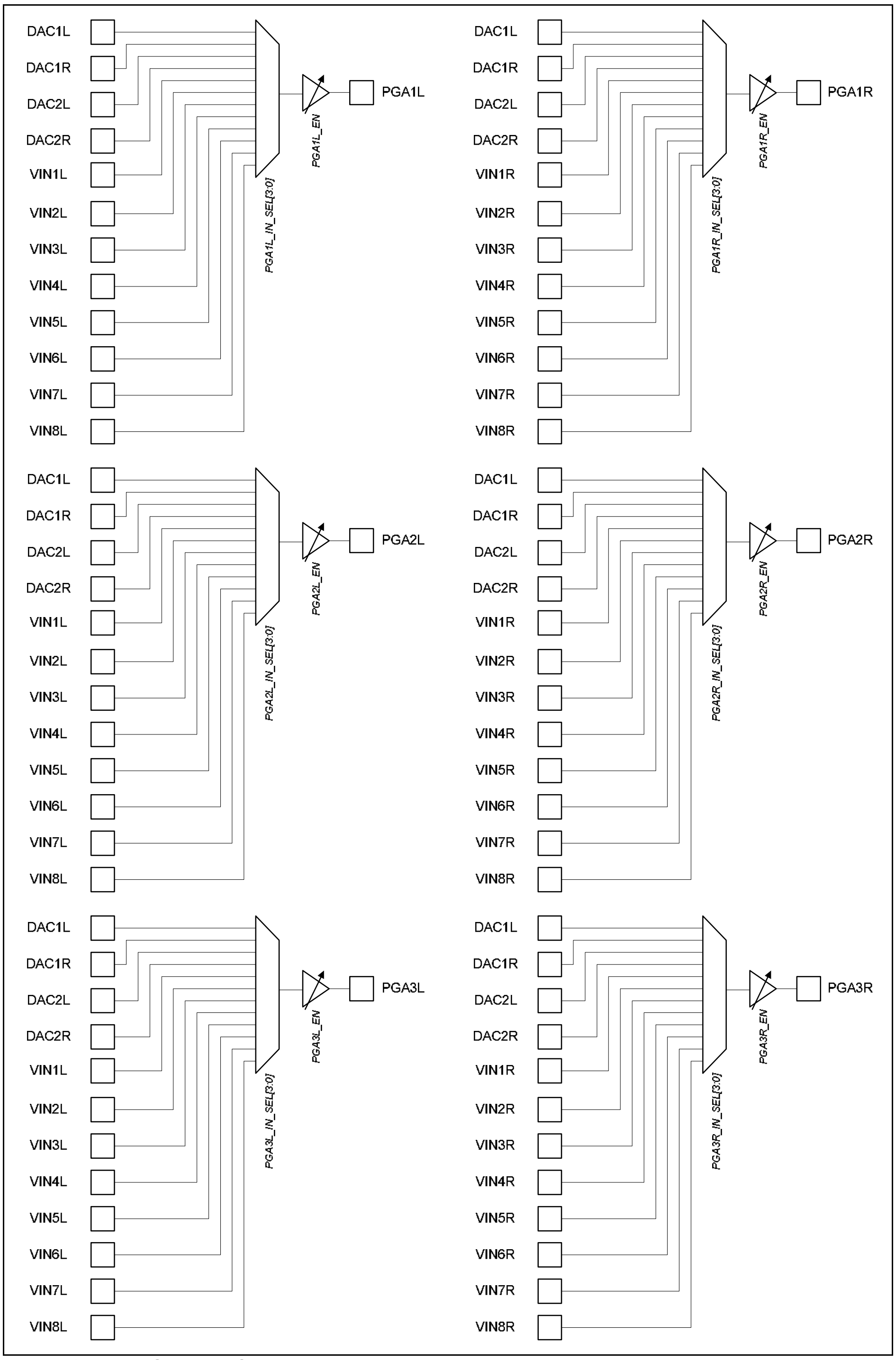


Figure 19 Input Selector Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 INPUT_CTRL1 1Ch	3:0	PGA1L_ IN_ SEL[3:0]	0000	**Left Input PGA Source Selection** 0000 = No input selected 0001 = VIN1L selected 0010 = VIN2L selected 0011 = VIN3L selected 0100 = VIN4L selected 0101 = VIN5L selected 0110 = VIN6L selected 0111 = VIN7L selected 1000 = VIN8L selected 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved
	11:8	PGA2L_ IN_ SEL[3:0]	0000	
R29 INPUT_CTRL2 1Dh	7:4	PGA3L_ IN_ SEL[3:0]	0000	
R28 INPUT_CTRL1 1Ch	7:4	PGA1R_ IN_ SEL[3:0]	0000	**Right Input PGA Source Selection** 0000 = No input selected 0001 = VIN1R selected 0010 = VIN2R selected 0011 = VIN3R selected 0100 = VIN4R selected 0101 = VIN5R selected 0110 = VIN6R selected 0111 = VIN7R selected 1000 = VIN8R selected 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved
R29 INPUT_CTRL2 1Dh	3:0	PGA2R_ IN_ SEL[3:0]	0000	
	11:8	PGA3R_ IN_ SEL[3:0]	0000	
R31 INPUT_CTRL4 1Fh	0	PGA1L_ EN	0	**Input PGA Enable Controls** 0 = PGA disabled 1 = PGA enabled
	1	PGA1R_ EN		
	2	PGA2L_ EN		
	3	PGA2R_ EN		
	4	PGA3L_ EN		
	5	PGA3R_ EN		

Table 29 PGA Input Select Control

ADC INPUT SELECTOR CONTROL

The ADC input switch can be configured to allow any combination of two inputs to be input to the ADC. Each input switch channel can be controlled independently.

The input switch also includes PGAs to provide a range of analogue gain settings between 0dB and +12dB prior to the ADC. These PGAs can be enabled and disabled independently.

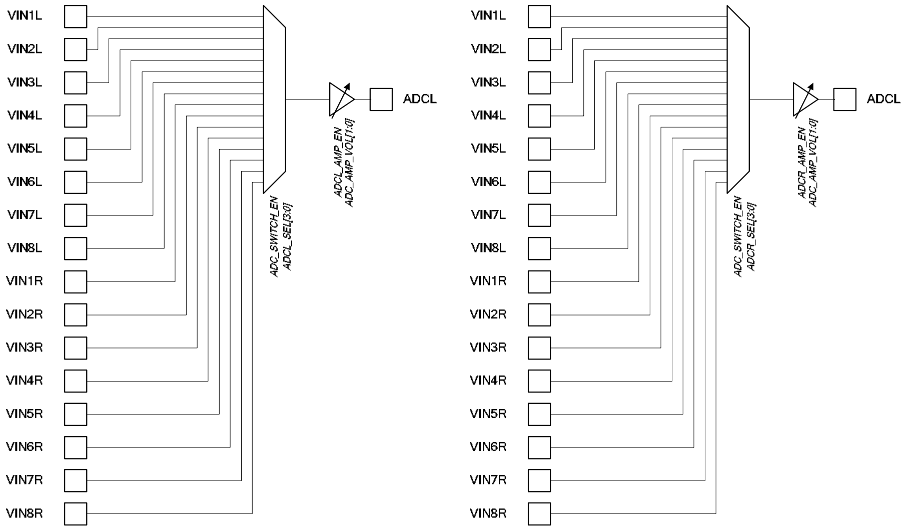


Figure 20 ADC Input Selector Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 INPUT_CTRL3 1Eh	3:0	ADCL_ SEL[3:0]	0000	**ADC Input Select** 0000 = VIN1L 0001 = VIN2L 0010 = VIN3L 0011 = VIN4L 0100 = VIN5L 0101 = VIN6L 0110 = VIN7L 0111 = VIN8L 1000 = VIN1R 1001 = VIN2R 1010 = VIN3R 1011 = VIN4R 1100 = VIN5R 1101 = VIN6R 1110 = VIN7R 1111 = VIN8R
	7:4	ADCR_ SEL[4:0]	0000	
	9:8	ADC_AMP _VOL[1:0]	10	**ADC Amplifier Gain Control** 00 = 0dB 01 = +3dB 10 = +6dB 11 = +12dB
	10	ADC_ SWITCH_ EN	0	**ADC Input Switch Control** 0 = ADC input switches open 1 = ADC input switches closed

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 INPUT_CTRL4 1Fh	6	ADCL_ AMP_EN	0	**ADC Input Amplifier Enable Controls** 0 = Amplifier disabled 1 = Amplifier enabled
	7	ADCR_ AMP_EN	0	

Table 30 ADC Input Switch Control

OUTPUT SELECTOR CONTROL

Any analogue PGA channel can be routed to any analogue output. All analogue outputs can be independently enabled and disabled. Additionally, all outputs can be tri-stated to allow the output to be connected to applications where ports can either be inputs or outputs.

Note: It is recommended to mute all the outputs before changing the output selector to avoid pop/click noises when selecting a different output source.

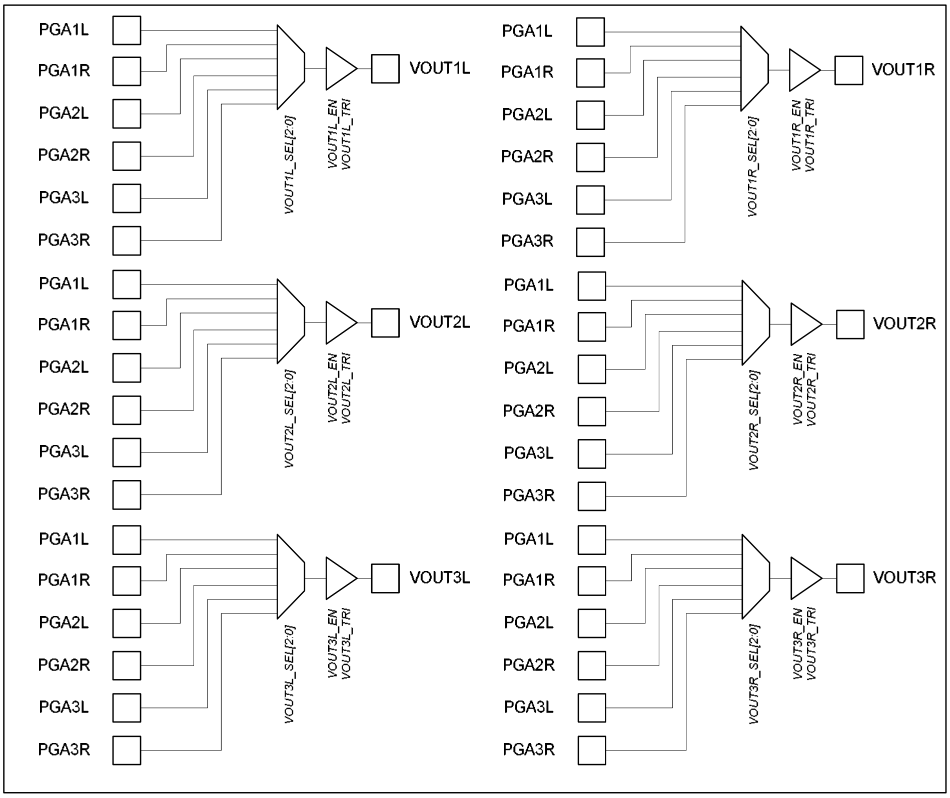


Figure 21 Output Selector Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 OUTPUT_ CTRL1 20h	2:0	VOUT1L_ SEL[2:0]	000	**Output Mux Selection** 000 = PGA1L 001 = PGA1R 010 = PGA2L 011 = PGA2R 100 = PGA3L 101 = PGA3R 11X = Reserved
	5:3	VOUT1R_ SEL[2:0]	001	
	8:6	VOUT2L_ SEL[2:0]	010	
R33 OUTPUT_ CTRL2 21h	2:0	VOUT2R_ SEL[2:0]	011	
	5:3	VOUT3L_ SEL[2:0]	100	
	8:6	VOUT3R_ SEL[2:0]	101	
R34 OUTPUT_ CTRL3 22h	0	VOUT1L_ TRI	0	**Output Amplifier Tristate Control** 0 = Normal operation 1 = Output amplifier tristate enable (Hi-Z)
	1	VOUT1R_ TRI		
	2	VOUT2L_ TRI		
	3	VOUT1R_ TRI		
	4	VOUT3L_ TRI		
	5	VOUT3R_ TRI		
	7	VOUT1L_ EN	0	**Output Amplifier Enables** 0 = Output amplifier disabled 1 = Output amplifier enabled
	8	VOUT1R_ EN		
	9	VOUT2L_ EN		
	10	VOUT2R_ EN		
	11	VOUT3L_ EN		
	12	VOUT3R_ EN		

Table 31 Output Selection

DIGITAL ROUTING CONTROL

The WM8593 includes a highly flexible digital routing multiplexer, allowing several independent systems to be directly connected to the WM8593 without the need for glue logic. The WM8593 consists of five digital audio 'ports', each with four pins, which can be configured to connect to any of the three internal WM8593 systems (ADC, DAC1 or DAC2) or to any other digital audio ports. Two GPIO pins are available as auxiliary bidirectional data pins when not used for jack detection. A simplified block diagram of the digital routing is shown in Figure 22:

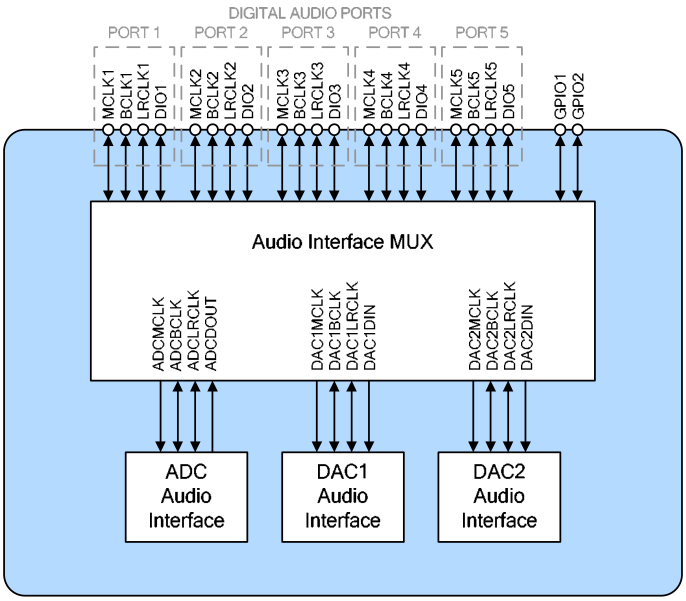


Figure 22 Digital Routing Block Diagram

DIGITAL AUDIO PORT PIN CONFIGURATION

The MCLK1 and DIO1 pins are defined individually as an input or an output using MCLK1_SEL[2:0] and DIO1_SEL[2:0] respectively. The BCLK1 and LRCLK1 pins are always defined as inputs or outputs together using WORDCLK1_SEL[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R37 AIF_MUX1 25h	3:1	MCLK1_ SEL[2:0]	000	**MCLK1 Pin Function Select** 000 = Input to WM8593 001 = Output MCLK2 010 = Output MCLK3 011 = Output MCLK4 100 = Output MCLK5 101 to 111 = Reserved
	6:4	WORD CLK1_ SEL[2:0]	000	**BCLK1 and LRCLK1 Pins Function Select** 000 = Inputs to WM8593 001 = Output BCLK2 and LRCLK2 010 = Output BCLK3 and LRCLK3 011 = Output BCLK4 and LRCLK4 100 = Output BCLK5 and LRCLK5 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
	9:7	DIO1_ SEL[2:0]	000	**DIO1 Pin Function Select** 000 = Input to WM8593 001 = Source DIO2 010 = Source DIO3 011 = Source DIO4 100 = Source DIO5 101 = Source GPIO1 110 = Source GPIO2 111 = Source ADC Data Output

Table 32 Digital Audio Port 1 Pin Configuration

The MCLK2 and DIO2 pins are defined individually as an input or an output using MCLK2_SEL[2:0] and DIO2_SEL[2:0] respectively. The BCLK2 and LRCLK2 pins are always defined as inputs or outputs together using WORDCLK2_SEL[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 AIF_MUX2 26h	3:1	MCLK2_ SEL[2:0]	001	**MCLK2 Pin Function Select** 000 = Output MCLK1 001 = Input to WM8593 010 = Output MCLK3 011 = Output MCLK4 100 = Output MCLK5 101 to 111 = Reserved
	6:4	WORD CLK2_ SEL[2:0]	001	**BCLK2 and LRCLK2 Pins Function Select** 000 = Output BCLK1 and LRCLK1 001 = Inputs to WM8593 010 = Output BCLK3 and LRCLK3 011 = Output BCLK4 and LRCLK4 100 = Output BCLK5 and LRCLK5 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
	9:7	DIO2_ SEL[2:0]	001	**DIO2 Pin Function Select** 000 = Output DIO1 001 = Input to WM8593 010 = Output DIO3 011 = Output DIO4 100 = Output DIO5 101 = Output GPIO1 110 = Output GPIO2 111 = Output ADC Data Output

Table 33 Digital Audio Port 2 Pin Configuration

The MCLK3 and DIO3 pins are defined individually as an input or an output using MCLK3_SEL[2:0] and DIO3_SEL[2:0] respectively. The BCLK3 and LRCLK3 pins are always defined as inputs or outputs together using WORDCLK3_SEL[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R39 AIF_MUX3 27h	3:1	MCLK3_ SEL[2:0]	010	**MCLK3 Pin Function Select** 000 = Output MCLK1 001 = Output MCLK2 010 = Input to WM8593 011 = Output MCLK4 100 = Output MCLK5 101 to 111 = Reserved
	6:4	WORD CLK3_ SEL[2:0]	010	**BCLK3 and LRCLK3 Pins Function Select** 000 = Output BCLK1 and LRCLK1 001 = Output BCLK2 and LRCLK2 010 = Inputs to WM8593 011 = Output BCLK4 and LRCLK4 100 = Output BCLK5 and LRCLK5 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
	9:7	DIO3_ SEL[2:0]	010	**DIO3 Pin Function Select** 000 = Output DIO1 001 = Output DIO2 010 = Input to WM8593 011 = Output DIO4 100 = Output DIO5 101 = Output GPIO1 110 = Output GPIO2 111 = Output ADC Data Output

Table 34 Digital Audio Port 3 Pin Configuration

The MCLK4 and DIO4 pins are defined individually as an input or an output using MCLK4_SEL[2:0] and DIO4_SEL[2:0] respectively. The BCLK4 and LRCLK4 pins are always defined as inputs or outputs together using WORDCLK4_SEL[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 AIF_MUX4 28h	3:1	MCLK4_ SEL[2:0]	011	**MCLK4 Pin Function Select** 000 = Output MCLK1 001 = Output MCLK2 010 = Output MCLK3 011 = Input to WM8593 100 = Output MCLK5 101 to 111 = Reserved
	6:4	WORD CLK4_ SEL[2:0]	011	**BCLK4 and LRCLK4 Pins Function Select** 000 = Output BCLK1 and LRCLK1 001 = Output BCLK2 and LRCLK2 010 = Output BCLK3 and LRCLK3 011 = Inputs to WM8593 100 = Output BCLK5 and LRCLK5 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
	9:7	DIO4_ SEL[2:0]	011	**DIO4 Pin Function Select** 000 = Output DIO1 001 = Output DIO2 010 = Output DIO3 011 = Input to WM8593 100 = Output DIO5 101 = Output GPIO1 110 = Output GPIO2 111 = Output ADC Data Output

Table 35 Digital Audio Port 4 Pin Configuration

The MCLK5 and DIO5 pins are defined individually as an input or an output using MCLK5_SEL[2:0] and DIO5_SEL[2:0] respectively. The BCLK5 and LRCLK5 pins are always defined as inputs or outputs together using WORDCLK5_SEL[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 AIF_MUX5 29h	3:1	MCLK5_ SEL[2:0]	100	**MCLK5 Pin Function Select** 000 = Output MCLK1 001 = Output MCLK2 010 = Output MCLK3 011 = Output MCLK4 100 = Input to WM8593 101 to 111 = Reserved
	6:4	WORD CLK5_ SEL[2:0]	100	**BCLK5 and LRCLK5 Pins Function Select** 000 = Output BCLK1 and LRCLK1 001 = Output BCLK2 and LRCLK2 010 = Output BCLK3 and LRCLK3 011 = Output BCLK4 and LRCLK4 100 = Inputs to WM8593 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
	9:7	DIO5_ SEL[2:0]	100	**DIO5 Pin Function Select** 000 = Output DIO1 001 = Output DIO2 010 = Output DIO3 011 = Output DIO4 100 = Input to WM8593 101 = Output GPIO1 110 = Output GPIO2 111 = Output ADC Data Output

Table 36 Digital Audio Port 5 Pin Configuration

ADC AUDIO INTERFACE CLOCK CONFIGURATION

The WM8593 ADC has an independent audio interface which can be configured to select the required signals from any of the digital audio ports. The audio interface is not restricted to take each signal from the same digital audio port, although the BCLK and LRCLK signals are selected together. For example, it is possible to use MCLK1, BCLK2, LRCLK2 and DIO5 as the digital audio port pins that connect to the ADC audio interface through the audio interface mux if required.

The MCLK is always an input to the ADC audio interface is selected using ADCMCLK_SEL[2:0]. The BCLK and LRCLK are always selected together, and can be either an input to the ADC audio interface (when the ADC is in slave mode) or an output from the ADC audio interface (when the ADC is in master mode). BCLK and LRCLK are selected using ADCWORDCLK_SEL[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 AIF_MUX8 2Ch	3:1	ADC MCLK_ SEL[2:0]	000	**ADCMCLK Select** 000 = Use MCLK1 001 = Use MCLK2 010 = Use MCLK3 011 = Use MCLK4 100 = Use MCLK5 101 to 111 = Reserved
	6:4	ADC WORD CLK_ SEL[2:0]	000	**ADC BCLK and LRCLK Select** 000 = Use BCLK1 and LRCLK1 001 = Use BCLK2 and LRCLK2 010 = Use BCLK3 and LRCLK3 011 = Use BCLK4 and LRCLK4 100 = Use BCLK5 and LRCLK5 101 = Use DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Use DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)

Table 37 ADC Audio Interface Clock Configuration

DAC1 AND DAC2 AUDIO INTERFACE CLOCK CONFIGURATION

Both DACs on the WM8593 have independent audio interfaces which can be configured to select the required signals from any of the digital audio ports. The audio interfaces are not restricted to take each signal from the same digital audio ports, although the BCLK and LRCLK signals are selected together. For example, it is possible to use MCLK1, BCLK2, LRCLK2 and DIO5 as the digital audio port pins that connect to the DAC1 audio interface through the audio interface mux, while using MCLK2, BCLK1, LRCLK1 and DIO3 for DAC2 if required.

DAC1MCLK and DAC2MCLK are always inputs to the DAC1 and DAC2 audio interfaces and are selected using DAC1MCLK_SEL[2:0] and DAC2MCLK_SEL[2:0] respectively.

DAC1BCLK and DAC1LRCLK are always selected together, and can be either an input to the DAC1 audio interface (when DAC1 is in slave mode) or an output from the DAC1 audio interface (when DAC1 is in master mode). DAC2BCLK and DAC2LRCLK are always selected together, and can be either an input to the DAC2 audio interface (when DAC2 is in slave mode) or an output from the DAC2 audio interface (when DAC2 is in master mode). DAC1BCLK and DAC1LRCLK are selected using DAC1WORDCLK_SEL[2:0], while DAC2BCLK and DAC2LRCLK are selected using DAC2WORDCLK_SEL[2:0].

Finally, the data input to the DAC1 audio interface is configured using DAC1DIN_SEL[2:0] and the data input to the DAC2 audio interface is configured using DAC2DIN_SEL[2:0]

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>R42
AIF_MUX6
2Ah</td><td rowspan="2">3:1</td><td>DAC1
MCLK_
SEL[2:0]</td><td rowspan="2">001</td><td rowspan="2">DAC MCLK Select
000 = Use MCLK1
001 = Use MCLK2
010 = Use MCLK3
011 = Use MCLK4
100 = Use MCLK5
101 to 111 = Reserved</td></tr>
<tr><td>R43
AIF_MUX7
2Bh</td><td>DAC2
MCLK_
SEL[2:0]</td></tr>
<tr><td>R42
AIF_MUX6
2Ah</td><td rowspan="2">6:4</td><td>DAC1
WORD
CLK_
SEL[2:0]</td><td rowspan="2">001</td><td rowspan="2">DAC BCLK and DAC LRCLK Select
000 = Use BCLK1 and LRCLK1
001 = Use BCLK2 and LRCLK2
010 = Use BCLK3 and LRCLK3
011 = Use BCLK4 and LRCLK4
100 = Use BCLK5 and LRCLK5
101 = Use DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode)
110 = Use DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode)
111 = Use ADCBCLK and ADCBCLK (when ADC is master mode)</td></tr>
<tr><td>R43
AIF_MUX7
2Bh</td><td>DAC2
WORD
CLK_
SEL[2:0]</td></tr>
<tr><td>R42
AIF_MUX6
2Ah</td><td rowspan="2">9:7</td><td>DAC1
DIN_
SEL[2:0]</td><td rowspan="2">001</td><td rowspan="2">DAC DIN Select
000 = Use DIO1
001 = Use DIO2
010 = Use DIO3
011 = Use DIO4
100 = Use DIO5
101 = Use GPIO1
110 = Use GPIO2
111 = Use ADCDOUT</td></tr>
<tr><td>R43
AIF_MUX7
2Bh</td><td>DAC2
DIN_
SEL[2:0]</td></tr>
</table>

Table 38 DAC1 and DAC2 Audio Interface Clock Configuration

UPDATE FUNCTION

To prevent clock contention issues during setup of the digital audio interface mux, an update system has been implemented. This allows the registers to be configured as required and the update to be applied with the last register write synchronise the configuration of the digital audio mux. An update can be generated using any of the update bits shown in Table 39.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R37 AIF_MUX1 25h	10	PORT1_ UPD	0	**Update** 0 = Latch corresponding settings into Register Map but do not update 1 = Latch corresponding settings into Register Map and update all simultaneously
R38 AIF_MUX2 26h	10	PORT2_ UPD		
R39 AIF_MUX3 27h	10	PORT3_ UPD		
R40 AIF_MUX4 28h	10	PORT4_ UPD		
R41 AIF_MUX5 29h	10	PORT5_ UPD		
R42 AIF_MUX6 2Ah	10	DAC1_ UPD		
R43 AIF_MUX7 2Bh	10	DAC2_ UPD		
R44 AIF_MUX8 2Ch	10	ADC_ UPD		

Table 39 Audio Interface Mux Update Bits

DETAILS ON CLOCK SWITCHING

In order to avoid short clock pulses (glitches) when switching between two independent clock sources, the MCLK and BCLK switching is carefully controlled within the WM8593 using various feedback and logic mechanisms. This controlled switching applies to all MCLK and BCLK digital audio port pins, and also when switching MCLK and BCLK sources in the ADC, DAC1 and DAC2 audio interfaces.

Example: Switching from MCLK2 to MCLK3 using the MCLK4 pin

CLK_A is applied to the MCLK2 pin, and CLK_B is applied to the MCLK3 pin. Initially, MCLK4_SEL[2:0]=001, so CLK_A is output on the MCLK4 pin. To change the output clock to CLK_B, set MCLK4_SEL[2:0]=010. The logic waits until CLK_A (MCLK2 pin) is low then disconnects CLK_A from the output (MCLK4) pin. The output pin (MCLK4) now outputs logic 0 for two rising edges of CLK_B (MCLK3 pin) before starting to output CLK_B. This behaviour is shown in Figure 23:

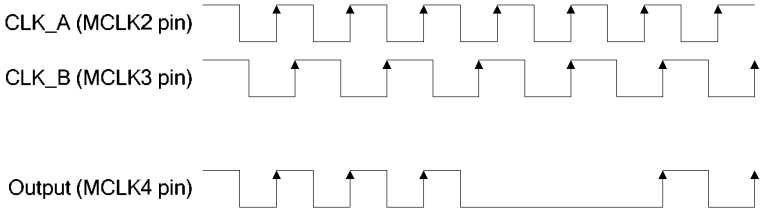


Figure 23 Clock Switching Example

If CLK_A in the previous example is not running the logic that controls switching between clocks will not function. In this case, it is possible to force an update on any individual digital audio port or audio interface using the relevant force bit. If this functionality is required, the relevant force bit should be set to '1' and then set back to '0' again.

Example: Switching from MCLK2 to MCLK3 using the MCLK4 pin when MCLK2 is not present

CLK_A is applied to the MCLK2 pin, and CLK_B is applied to the MCLK3 pin. Initially, MCLK4_SEL[2:0]=001, so CLK_A is output on the MCLK4 pin. However, CLK_A is not running. To change the output clock to CLK_B, set MCLK4_SEL[2:0]=010 and PORT4_FORCE=1. Finally, set PORT4_FORCE=0 to complete the switch.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R37 AIF_MUX1 25h	0	PORT1_ FORCE	0	**Force Clocks to Change** 0 = Wait until clocks are safe before switching between clock sources 1 = Force clock sources to change immediately **Note:** These bits must be returned to '0' before clocks will be output
R38 AIF_MUX2 26h	0	PORT2_ FORCE		
R39 AIF_MUX3 27h	0	PORT3_ FORCE		
R40 AIF_MUX4 28h	0	PORT4_ FORCE		
R41 AIF_MUX5 29h	0	PORT5_ FORCE		
R42 AIF_MUX6 2Ah	0	DAC1_ FORCE		
R43 AIF_MUX7 2Bh	0	DAC2_ FORCE		
R44 AIF_MUX8 2Ch	0	ADC_ FORCE		

Table 40 Audio Interface Mux Force Bits

USING GPIO PINS AS ADDITIONAL DATA PINS

There are two GPIO pins, GPIO1 and GPIO2, which can be used as additional pins to connect to external devices. GPIO1 is controlled by GPIO1_SEL[2:0] and GPIO2 by GPIO2_SEL[2:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 AIF_MUX9 2Dh	3:1	GPIO1_ SEL[2:0]	000	**GPIO1 Pin Function Select** 000 = Source DIO1 001 = Source DIO2 010 = Source DIO3 011 = Source DIO4 100 = Source DIO5 101 = Input to WM8593 110 = Source GPIO2 111 = Source ADC Data Output
	10	GPIO1_ UPD	0	**GPIO1 Update** 0 = Latch corresponding GPIO1 settings into Register Map but do not update 1 = Latch corresponding GPIO1 settings into Register Map and update

Table 41 GPIO1 Audio Interface Mux Configuration

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 AIF_MUX10 2Eh	3:1	GPIO2_ SEL[2:0]	000	**GPIO2 Pin Function Select** 000 = Source DIO1 001 = Source DIO2 010 = Source DIO3 011 = Source DIO4 100 = Source DIO5 101 = Source GPIO1 110 = Input to WM8593 111 = Source ADC Data Output
	10	GPIO2_ UPD	0	**GPIO2 Update** 0 = Latch corresponding GPIO2 settings into Register Map but do not update 1 = Latch corresponding GPIO2 settings into Register Map and update

Table 42 GPIO2 Audio Interface Mux Configuration

JACK DETECT

When using the WM8593 with headphones, a jack detect function is available using the GPIO pins. The jack detect function is controlled using GPIO1_APP and GPIO2_APP. The polarity of the jack detect signal can be inverted using JD_INV. When a jack is detected, the WM8593 will automatically mute PGAs as defined by JD_PGA1L_MUTE, JD_PGA1R_MUTE, JD_PGA2L_MUTE, JD_PGA2R_MUTE, JD_PGA3L_MUTE and JD_PGA3R_MUTE.

See Application Information section for details of connections to the headphone jack.

Example: Mute speakers when headphone is inserted

Assume PGA1L is connected to VOUT1L, PGA1R is connected to VOUT1R and so on. VOUT1L and VOUT1R are used to drive the speaker amplifier, and VOUT3L and VOUT3R are used to drive headphones directly. Set GPIO1_APP=1 to enable jack detect on GPIO1, then set JD_PGA1L_MUTE=1 and JD_PGA1R_MUTE=1 to mute PGA1L and PGA1R when a set of headphones is inserted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 GEN 1Bh	0	GPIO1_ APP	0	**GPIO1 Application Select** 0 = Use GPIO1 as data pin for audio interface mux 1 = Use GPIO1 as input for jack detect
	1	GPIO2_ APP	0	**GPIO2 Application Select** 0 = Use GPIO2 as data pin for audio interface mux 1 = Use GPIO2 as input for jack detect
	2	JD_INV	0	**Jack Detect Polarity** 0 = Normal (active low) 1 = Inverted (active high)
R26 PGA_CTRL2 1Ah	7	JD_ PGA1L_ MUTE	0	**Jack Detect Mute Control** 0 = Do not mute PGA when jack is detected 1 = Mute PGA when jack is detected
	8	JD_ PGA1R_ MUTE	0	
	9	JD_ PGA2L_ MUTE	0	
	10	JD_ PGA2R_ MUTE	0	
	11	JD_ PGA3L_ MUTE	0	
	12	JD_ PGA3R_ MUTE	0	

Table 43 Jack Detect Control

POP AND CLICK PERFORMANCE

The WM8593 includes a number of features designed to minimise pops and clicks in various phases of operation including power up, power down, changing analogue paths and starting/stopping clocks. In order to ensure optimum performance, the following sequences should be followed.

POWERUP SEQUENCE

1. Apply power to the WM8593 (see Power On Reset).
2. Set-up initial internal biases:
   - SOFT_ST=1
   - FAST_EN=1
   - POBCTRL=1
3. Enable output drivers to allow the AC coupling capacitors at the output stage to be pre-charged to DACVMID:
   - VOUTxL_EN=1
   - VOUTxR_EN=1
4. Enable DACVMID. 500k selected here for optimum pop reduction:
   - VMID_SEL=10
5. Wait until DACVMID has fully charged. The time is dependent on the capacitor values used to AC-couple the outputs and to decouple DACVMID, and the VMID_SEL value chosen. An approximate delay of 6xRCms can be used, where R is the DACVMID resistance and C is the decoupling capacitor on DACVMID. For DACVMID resistance of 50kΩ and C=4.7uF, the delay should be approximately 1.5 seconds.
   - Insert delay
6. Enable the master bias and DACVMID buffer:
   - BIAS_EN=1
   - BUFIO_EN=1
7. Switch the output drivers to use the master bias instead of the power up (fast) bias:
   - POBCTRL=0
8. Enable all functions (DACs, ADC, PGAs) required for use. Outputs are muted by default so the write order is not important.
9. Unmute the outputs and switch DACVMID resistance to 50k for normal operation:
   - VOUTxL_MUTE=0
   - VOUTxR_MUTE=0
   - VMID_SEL=01

POWERDOWN SEQUENCE

1. Mute all outputs:
   - MUTE_ALL=1
2. Set up biases for power down mode:
   - FAST_EN=1
   - VMID_SEL=01
   - BIAS_EN=1
   - BUFIO_EN=1
   - VMIDTOG=1
   - SOFT_ST=0
3. Switch outputs to use fast bias instead of master bias:
   - POBCTRL=1
4. Power down all WM8593 functions (ADC, DACs, PGAs etc.). The outputs are muted so the write order is not important.
5. Power down VMID to allow the analogue outputs to ramp gently to ground in a pop-free manner.
   - VMID_SEL=00
6. Wait until DACVMID has fully discharged. The time taken depends on system capacitance.
   - Insert delay
7. Clamp outputs to ground.
   - APE_B=0
8. Power down outputs.
   - VOUTxL_EN=0
   - VOUTxR_EN=0
9. Disable remaining bias control bits.
   - FAST_EN=0
   - POBCTRL=0
   - BIAS_EN=0

Power supplies can now be safely removed from the WM8593 if desired. Table 44 describes the various bias control bits for power up/down control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 BIAS 23h	0	POBCTRL	0	**Bias Source for Output Amplifiers** 0 = Output amplifiers use master bias 1 = Output amplifiers use fast bias
	1	VMIDTOG	0	**VMID Power Down Characteristic** 0 = Slow ramp 1 = Fast ramp
	2	FAST_EN	0	**Fast Bias Enable** 0 = Fast bias disabled 1 = Fast bias enabled
	3	BUFIO_ EN	0	**VMID Buffer Enable** 0 = VMID Buffer disabled 1 = VMID Buffer enabled
	4	SOFT_ST	1	**VMID Soft Ramp Enable** 0 = Soft ramp disabled 1 = Soft ramp enabled
	5	BIAS_EN	0	**Master Bias Enable** 0 = Master bias disabled 1 = Master bias enabled Also powers down ADCVMID
	7:6	VMID_ SEL[1:0]	00	**VMID Resistor String Value Selection (DACVMID only)** 00 = off (no VMID) 01 = 100k 10 = 500k 11 = 10k The selection is the total resistance of the string from DACREFP to DACREFN. The ADCVMID resistance is fixed at 200kΩ.

Table 44 Bias Control

REGISTER MAP

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Hex Default
0	00	DEVICE_ID	Read: DEVICE_ID[15:0] / Write: SW_RST																0x8594
1	01	REVISION	0	0	0	0	0	0	0	0	REVNUM[7:0]								0x0000
2	02	DAC1_CTRL1	0	0	0	0	DAC1_OP_MUX[1:0]		DAC1_MUTE	DAC1_EN	DAC1_ZCEN	DAC1_DEEMPH	DAC1_LRP	DAC1_BCP	DAC1_WL[1:0]		DAC1_FMT[1:0]		0x008A
3	03	DAC1_CTRL2	0	0	0	0	0	0	0	0	0	0	DAC1_BCLKDIV[2:0]			DAC1_SR[2:0]			0x0000
4	04	DAC1_CTRL3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC1_MSTR	0x0000
5	05	DAC1L_VOL	0	0	0	0	0	0	0	DAC1L_VU	DAC1L_VOL[7:0]								0x00C8
6	06	DAC1R_VOL	0	0	0	0	0	0	0	DAC1R_VU	DAC1R_VOL[7:0]								0x00C8
7	07	DAC2_CTRL1	0	0	0	0	DAC2_OP_MUX[1:0]		DAC2_MUTE	DAC2_EN	DAC2_ZCEN	DAC2_DEEMPH	DAC2_LRP	DAC2_BCP	DAC2_WL[1:0]		DAC2_FMT[1:0]		0x008A
8	08	DAC2_CTRL2	0	0	0	0	0	0	0	0	0	0	DAC2_BCLKDIV[2:0]			DAC2_SR[2:0]			0x0000
9	09	DAC2_CTRL3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC2_MSTR	0x0000
10	0A	DAC2L_VOL	0	0	0	0	0	0	0	DAC2L_VU	DAC2L_VOL[7:0]								0x00C8
11	0B	DAC2R_VOL	0	0	0	0	0	0	0	DAC2R_VU	DAC2R_VOL[7:0]								0x00C8
12	0C	ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GLOBAL_EN	0x0000
13	0D	ADC_CTRL1	0	0	ADC_ZC_EN	ADC_HPD	ADC_DATA_SEL[1:0]		ADCL_INV	ADCR_INV	ADC_LRSWAP	ADC_EN	ADC_LRP	ADC_BCP	ADC_WL[1:0]		ADC_FMT[1:0]		0x200A
14	0E	ADC_CTRL2	0	0	0	0	0	0	0	0	0		ADC_BCLKDIV[2:0]			ADC_SR[2:0]			0x0000
15	0F	ADC_CTRL3	0	0	0	0	0	0	0	0	0	0	0	0	0	0		ADC_MSTR	0x0000
16	10	ADCL_VOL	0	0	0	0	0	0	0	ADCL_VU	ADCL_VOL[7:0]								0x00C3
17	11	ADCR_VOL	0	0	0	0	0	0	0	ADCR_VU	ADCR_VOL[7:0]								0x00C3
19	13	PGA1L_VOL	0	0	0	0	0	0	0	PGA1L_VU	PGA1L_VOL[7:0]								0x000C
20	14	PGA1R_VOL	0	0	0	0	0	0	0	PGA1R_VU	PGA1R_VOL[7:0]								0x000C
21	15	PGA2L_VOL	0	0	0	0	0	0	0	PGA2L_VU	PGA2L_VOL[7:0]								0x000C
22	16	PGA2R_VOL	0	0	0	0	0	0	0	PGA2R_VU	PGA2R_VOL7:0]								0x000C
23	17	PG3L_VOL	0	0	0	0	0	0	0	PGA3L_VU	PGA3L_VOL[7:0]								0x000C
24	18	PGA3R_VOL	0	0	0	0	0	0	0	PGA3R_VU	PGA3R_VOL[7:0]								0x000C
25	19	PGA_CTRL1	0	0	0	0	0	0	0	0	PGA3R_ZC	PGA3L_ZC	PGA2R_ZC	PGA2L_ZC	PGA1R_ZC	PGA1L_ZC	ATTACK_BYPASS	DECAY_BYPASS	0x00FC
26	1A	PGA_CTRL2	0	0	0	JD_PGA3R_MUTE	JD_PGA3L_MUTE	JD_PGA2R_MUTE	JD_PGA2L_MUTE	JD_PGA1R_MUTE	JD_PGA1L_MUTE	VOUT3R_MUTE	VOUT3L_MUTE	VOUT2R_MUTE	VOUT2L_MUTE	VOUT1R_MUTE	VOUT1L_MUTE	MUTE_ALL	0x007E
27	1B	GEN	0	0	0	0	0	0	0	0	0	PGA_SR[2:0]			AUTO_INC	JD_INV	GPIO2_APP	GPIO1_APP	0x0048
28	1C	INPUT_CTRL1	0	0	0	0	PGA2L_IN_SEL[3:0]				PGA1R_IN_SEL[3:0]				PGA1L_IN_SEL[3:0]				0x0000
29	1D	INPUT_CTRL2	0	0	0	0	PGA3R_IN_SEL[3:0]				PGA3L_IN_SEL[3:0]				PGA2R_IN_SEL[3:0]				0x0000
30	1E	INPUT_CTRL3	0	0	0	0	0	ADC_SWITCH_EN	ADC_AMP_VOL[1:0]		ADCR_SEL[3:0]				ADCL_SEL[3:0]				0x0008
31	1F	INPUT_CTRL4	0	0	0	0	0	0	0	0	ADCR_AMP_EN	ADCL_AMP_EN	PGA3R_EN	PGA3L_EN	PGA2R_EN	PGA2L_EN	PGA1R_EN	PGA1L_EN	0x0000
32	20	OUTPUT_CTRL1	0	0	0	0	0	0	0	VOUT2L_SEL[2:0]			VOUT1R_SEL[2:0]			VOUT1L_SEL[2:0]			0x0088
33	21	OUTPUT_CTRL2	0	0	0	0	0	0	0	VOUT3R_SEL[2:0]			VOUT3L_SEL[2:0]			VOUT2R_SEL[2:0]			0x0163
34	22	OUTPUT_CTRL3	0	0	0	VOUT3R_EN	VOUT3L_EN	VOUT2R_EN	VOUT2L_EN	VOUT1R_EN	VOUT1L_EN	APE_B	VOUT3R_TRI	VOUT3L_TRI	VOUT2R_TRI	VOUT2L_TRI	VOUT1R_TRI	VOUT1L_TRI	0x0040
35	23	BIAS	0	0	0	0	0	0	0	0	VMID_SEL[1:0]		BIAS_EN	SOFT_ST	BUFIOEN	FAST_EN	VMIDTOG	POBCTRL	0x0010
36	24	PGA_CTRL_3	0	0	0	0	0	PGA_UPD	0	0	0	0	0	0	PGA_SEL[2:0]			PGA_SAFE_SW	0x0002
37	25	AIF_MUX1	0	0	0	0	0	PORT1_UPD	DIO1_SEL[2:0]			WORDCLK1_SEL[2:0]			MCLK1_SEL[2:0]			PORT1_FORCE	0x0000
38	26	AIF_MUX2	0	0	0	0	0	PORT2_UPD	DIO2_SEL[2:0]			WORDCLK2_SEL[2:0]			MCLK2_SEL[2:0]			PORT2_FORCE	0x0092
39	27	AIF_MUX3	0	0	0	0	0	PORT3_UPD	DIO3_SEL[2:0]			WORDCLK3_SEL[2:0]			MCLK3_SEL[2:0]			PORT3_FORCE	0x0124
40	28	AIF_MUX4	0	0	0	0	0	PORT4_UPD	DIO4_SEL[2:0]			WORDCLK4_SEL[2:0]			MCLK4_SEL[2:0]			PORT4_FORCE	0x01B6
41	29	AIF_MUX5	0	0	0	0	0	PORT5_UPD	DIO5_SEL[2:0]			WORDCLK5_SEL[2:0]			MCLK5_SEL[2:0]			PORT5_FORCE	0x0248
42	2A	AIF_MUX6	0	0	0	0	0	DAC1_UPD	DAC1DIN_SEL[2:0]			DAC1WORDCLK_SEL[2:0]			DAC1MCLK_SEL[2:0]			DAC1_FORCE	0x0092
43	2B	AIF_MUX7	0	0	0	0	0	DAC2_UPD	DAC2DIN_SEL[2:0]			DAC2WORDCLK_SEL[2:0]			DAC2MCLK_SEL[2:0]			DAC2_FORCE	0x0092
44	2C	AIF_MUX8	0	0	0	0	0	ADC_UPD	ADCDOUT_SEL[2:0]			ADCWORDCLK_SEL[2:0]			ADCMCLK_SEL[2:0]			ADC_FORCE	0x0248
45	2D	AIF_MUX9	0	0	0	0	0	GPIO1_UPD	0	0	0	0	0	0	GPIO1_SEL[2:0]			0	0x0000
46	2E	AIF_MUX10	0	0	0	0	0	GPIO2_UPD	0	0	0	0	0	0	GPIO2_SEL[2:0]			0	0x0000

R0 (0h) – Software Reset / Device ID Register (DEVICE_ID)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	DEVICE_ID[15:8]							
Write	SW_RST							
Default	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DEVICE_ID[7:0]							
Write	SW_RST							
Default	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DEVICEID[15:0]	**Device ID** A read of this register will return the device ID. In this case 0x8593.
SW_RST	**Software Reset** A write of any value to this register will generate a software reset.

Figure 24 R0 – Software Reset / Device ID

R1 (01h) – Device Revision Register (REVISION)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	REVNUM[7:0]							
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
N/A = Not Applicable (no function implemented)								

Function	Description
REVNUM[7:0]	**Device Revision** A read of this register will return the device revision number. This number is sequentially incremented if the device design is updated.

Figure 25 R1 – Device Revision Register

R2 (02h) – DAC Control Register 1 (DAC1_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	DAC1_OP_MUX[1:0]		DAC1_MUTE	DAC1_EN
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC1_ZCEN	DAC1_ DEEMPH	DAC1_LRP	DAC1_BCP	DAC1_WL[1:0]		DAC1_FMT[1:0]	
Write								
Default	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1_FMT[1:0]	**DAC1 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
DAC1_WL[1:0]	**DAC1 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
DAC1_BCP	**DAC1 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
DAC1_LRP	**DAC1 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
DAC1_DEEMPH	**DAC1 Deemphasis** 0 = No deemphasis 1 = Apply 44.1kHz deemphasis
DAC1_ZCEN	**DAC1 Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross
DAC1_EN	**DAC1 Enable** 0 = DAC disabled 1 = DAC enabled
DAC1_MUTE	**DAC1 Softmute** 0 = Normal operation 1 = Softmute applied
DAC1_OP_MUX[1:0]	**DAC1 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to DAC1R) 10 = Mono (Right data to DAC1L) 11 = Digital Monomix, (L+R)/2

Figure 26 R2 – DAC1 Control Register 1

R3 (03h) – DAC1 Control Register 2 (DAC1_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	DAC1_BCLKDIV[2:0]			DAC1_SR[2:0]		
Write	N/A	N/A						
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1_SR[2:0]	**DAC1 MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
DAC1_ BCLKDIV [2:0]	**DAC1 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC1_BCLKDIV[2:0] are reserved

Figure 27 R3 – DAC1 Control Register 2

R4 (04h) – DAC1 Control Register 3 (DAC1_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	0	DAC1_MSTR
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1_MSTR	**DAC1 Master Mode Select** 0 = Slave mode, DACBCLK1 and DACLRCLK1 are inputs to WM8593 1 = Master mode, DACBCLK1 and DACLRCLK1 are outputs from WM8593

Figure 28 R4 – DAC1 Control Register 3

R5 (05h) – DAC1L Digital Volume Control Register (DAC1L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC1L_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC1L_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1L_VOL[7:0]	**DAC1L Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC1L_VU	**DAC1L Digital Volume Update** 0 = Latch DAC1L_VOL[7:0] into Register Map but do not update volume 1 = Latch DAC1L_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 29 R5 – DAC1L Digital Volume Control Register

R6 (06h) – DAC1R Digital Volume Control Register (DAC1R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC1R_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC1R_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1R_VOL[7:0]	**DAC1R Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC1R_VU	**DAC1R Digital Volume Update** 0 = Latch DACR_VOL[7:0] into Register Map but do not update volume 1 = Latch DACR_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 30 R6 – DAC1R Digital Volume Control Register

<table>
<tr><th colspan="9">R7 (07h) – DAC2 Control Register 1 (DAC2_CTRL1)</th></tr>
<tr><td>Bit #</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2" rowspan="2">DAC2_OP_MUX[1:0]</td><td rowspan="2">DAC2_MUTE</td><td rowspan="2">DAC2_EN</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit #</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Read</td><td rowspan="2">DAC2_ZCEN</td><td rowspan="2">DAC2_
DEEMPH</td><td rowspan="2">DAC2_LRP</td><td rowspan="2">DAC2_BCP</td><td colspan="2" rowspan="2">DAC2_WL[1:0]</td><td colspan="2" rowspan="2">DAC2_FMT[1:0]</td></tr>
<tr><td>Write</td></tr>
<tr><td>Default</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td colspan="9">N/A = Not Applicable (no function implemented)</td></tr>
</table>

Function	Description
DAC2_FMT[1:0]	**DAC2 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
DAC2_WL[1:0]	**DAC2 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
DAC2_BCP	**DAC2 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
DAC2_LRP	**DAC2 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
DAC2_DEEMPH	**DAC2 Deemphasis** 0 = No deemphasis 1 = Apply 44.1kHz deemphasis
DAC2_ZCEN	**DAC2 Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross
DAC2_EN	**DAC2 Enable** 0 = DAC2 disabled 1 = DAC2 enabled
DAC2_MUTE	**DAC2 Softmute** 0 = Normal operation 1 = Softmute applied
DAC2_OP_MUX[1:0]	**DAC2 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to Right DAC2) 10 = Mono (Right data to Left DAC2) 11 = Digital Monomix, (L+R)/2

Figure 31 R7 – DAC2 Control Register 1

R8 (08h) – DAC2 Control Register 2 (DAC2_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	DAC2_BCLKDIV[2:0]			DAC2_SR[2:0]		
Write	N/A	N/A						
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
DAC2_SR[2:0]	**DAC2 MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
DAC2_BCLKDIV[2:0]	**DAC2 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC2_BCLKDIV[2:0] are reserved

Figure 32 R8 – DAC2 Control Register 2

R9 (09h) – DAC2 Control Register 3 (DAC2_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	0	DAC2_MSTR
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
DAC2_MSTR	**DAC2 Master Mode Select** 0 = Slave mode, DACBCLK2 and DACLRCLK2 are inputs to WM8593 1 = Master mode, DACBCLK2 and DACLRCLK2 are outputs from WM8593

Figure 33 R9 – DAC2 Control Register 3

R10 (0Ah) – DAC2L Digital Volume Control Register (DAC2L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC2L_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC2L_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	**Description**
DAC2L_VOL[7:0]	**DAC2 Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC2L_VU	**DAC2 Digital Volume Update** 0 = Latch DAC2L_VOL[7:0] into Register Map but do not update volume 1 = Latch DAC2L_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 34 R10 – DAC2L Digital Volume Control Register

R11 (0Bh) – DAC2R Digital Volume Control Register (DAC2R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC2R_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC2R_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	**Description**
DAC2R_VOL[7:0]	**DAC2R Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC2R_VU	**DAC2R Digital Volume Update** 0 = Latch DAC2R_VOL[7:0] into Register Map but do not update volume 1 = Latch DAC2R_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 35 R11 – DAC2R Digital Volume Control Register

R12 (0Ch) – Device Enable Register (ENABLE)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	0	GLOBAL_EN
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
GLOBAL_EN	**Device Global Enable** 0 = ADC, DAC and PGA ramp control circuitry disabled 1 = ADC, DAC and PGA ramp control circuitry enabled

Figure 36 R12 – Device Enable Register

R13 (0Dh) – ADC Control Register 1 (ADC_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	ADC_ZCEN	ADC_HPD	ADC_DATA_SEL[1:0]		ADCL_INV	ADCR_INV
Write	N/A	N/A						
Default	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADC_ LRSWAP	ADC_EN	ADC_LRP	ADC_BCP	ADC_WL[1:0]		ADC_FMT[1:0]	
Write								
Default	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
ADC_FMT[1:0]	**ADC Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
ADC_WL[1:0]	**ADC Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
ADC_BCP	**ADC BCLK Polarity** 0 = ADCBCLK not inverted - data latched on rising edge of BCLK 1 = ADCBCLK inverted - data latched on falling edge of BCLK
ADC_LRP	**ADC LRCLK Polarity** 0 = ADCLRCLK not inverted 1 = ADCLRCLK inverted
ADC_EN	**ADC Enable** 0 = ADC disabled 1 = ADC enabled
ADC_LRSWAP	**ADC Left/Right Swap** 0 = Normal 1 = Swap left channel data into right channel and vice-versa

ADCR_INV ADCL_INV	**ADCL and ADCR Output Signal Inversion** 0 = Output not inverted 1 = Output inverted
ADC_DATA_SEL[1:0]	**ADC Data Output Select** 00 = left data from ADCL, right data from ADCR (Normal Stereo) 01 = left data from ADCL, right data from ADCL (Mono Left) 10 = left data from ADCR, right data from ADCR (Mono Right) 11 = left data from ADCR, right data from ADCL (Reverse Stereo)
ADC_HPD	**ADC High Pass Filter Disable** 0 = High pass filter enabled 1 = High pass filter disabled
ADC_ZC_EN	**ADC Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross, change volume instantly 1 = Use zero cross, change volume when data crosses zero

Figure 37 R13 – ADC Control Register 1

R14 (0Eh) – ADC Control Register 2 (ADC_CTRL2)

Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	ADC_BCLKDIV[2:0]			ADC_SR[2:0]		
Write	N/A	N/A						
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	**Description**
ADC_SR[2:0]	**ADC MCLK:LRCLK Ratio** 000 = Auto detect 001 = reserved 010 = reserved 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = Reserved
ADC_BCLKDIV[2:0]	**ADC BCLK Rate (when ADC in Master Mode)** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of ADC_BCLKDIV[2:0] are reserved

Figure 38 R14 – ADC Control Register 2

R15 (0Fh) – ADC Control Register 3 (ADC_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	0	ADC_MSTR
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
ADC_MSTR	**ADC Master Mode Select** 0 = Slave mode, ADCBCLK and ADCLRCLK are inputs to WM8593 1 = Master mode, ADCBCLK and ADCLRCLK are outputs from WM8593

Figure 39 R15 – ADC Control Register 3

R16 (10h) – Left ADC Digital Volume Control Register (ADCL_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	ADCL_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADCL_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
N/A = Not Applicable (no function implemented)								

Function	Description
ADCL_VOL[7:0]	**Left ADC Digital Volume** 0000 0000 = Digital mute 0000 0001 = -97dB 0000 0010 = -96.5dB …0.5dB steps 1100 0011 = 0dB …0.5dB steps 1111 1110 = +29.5dB 1111 1111 = +30dB
ADCL_VU	**Left DAC Digital Volume Update** 0 = Latch ADCL_VOL[7:0] into Register Map but do not update volume 1 = Latch ADCL_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 40 R16 – Left ADC Digital Volume Control Register

R17 (11h) – Right ADC Digital Volume Control Register (ADCR_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	ADCR_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADCR_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
N/A = Not Applicable (no function implemented)								

Function	Description
ADCR_VOL[7:0]	**Right ADC Digital Volume** 0000 0000 = Digital mute 0000 0001 = -97dB 0000 0010 = -96.5dB …0.5dB steps 1100 0011 = 0dB …0.5dB steps 1111 1110 = +29.5dB 1111 1111 = +30dB
ADCR_VU	**Right ADC Digital Volume Update** 0 = Latch ADCR_VOL[7:0] into Register Map but do not update volume 1 = Latch ADCR_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 41 R17 – Right ADC Digital Volume Control Register

R19 (13h) – PGA1L Volume Control Register (PGA1L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA1L_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA1L_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R20 (14h) – PGA1R Volume Control Register (PGA1R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA1R_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA1R_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R21 (15h) – PGA2L Volume Control Register (PGA2L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA2L_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA2L_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R22 (16h) – PGA2R Volume Control Register (PGA2R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA2R_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA2R_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

…Continued on next page

R23 (17h) – PGA3L Volume Control Register (PGA3L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA3L_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA3L_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R24 (18h) – PGA3R Volume Control Register (PGA3R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA3R_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA3R_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

PGA1L_VOL[7:0] PGA1R_VOL[7:0] PGA2L_VOL[7:0] PGA2R_VOL[7:0] PGA3L_VOL[7:0] PGA3R_VOL[7:0]	**Input PGA Volume** 0000 0000 = +6dB 0000 0001 = +5.5dB …0.5dB steps 00001100 = 0dB … 1001 1110 = -73.5dB 1001 1111 = PGA Mute
PGA1L_VU PGA1R_VU PGA2L_VU PGA2R_VU PGA3L_VU PGA3R_VU	**Input PGA Volume Update** 0 = Latch corresponding volume setting into Register Map but do not update volume 1 = Latch corresponding volume setting into Register Map and update all channels simultaneously

Figure 42 R19-24 – PGA Volume Control Registers

R25 (19h) – PGA Control Register 1 (PGA_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read / Write	PGA3R_ZC	PGA3L_ZC	PGA2R_ZC	PGA2L_ZC	PGA1R_ZC	PGA1L_ZC	ATTACK_ BYPASS	DECAY_ BYPASS
Default	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
DECAY_BYPASS	**PGA Gain Decay Mode** 0 = PGA gain will ramp down 1 = PGA gain will step down
ATTACK_BYPASS	**PGA Gain Attack Mode** 0 = PGA gain will ramp up 1 = PGA gain will step up
PGA1L_ZC PGA1R_ZC PGA2L_ZC PGA2R_ZC PGA3L_ZC PGA3R_ZC	**PGA Gain Zero Cross Enable** 0 = PGA gain updates occur immediately 1 = PGA gain updates occur on zero cross Zero cross must be disabled to use gain ramp

Figure 43 R25 – PGA Control Register 1

R26 (1Ah) – PGA Control Register 2 (PGA_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	JD_PGA3R_MUTE	JD_PGA3L_MUTE	JD_PGA2R_MUTE	JD_PGA2L_MUTE	JD_PGA1R_MUTE
Write	N/A	N/A	N/A					
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	JD_PGA1L_MUTE	VOUT3R_MUTE	VOUT3L_MUTE	VOUT2R_MUTE	VOUT2L_MUTE	VOUT1R_MUTE	VOUT1L_MUTE	MUTE_ALL
Write								
Default	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
MUTE_ALL	**Master Output Driver Mute Control** 0 = Unmute all output drivers 1 = Mute all output drivers
VOUT1L_MUTE VOUT1R_MUTE VOUT2L_MUTE VOUT2R_MUTE VOUT3L_MUTE VOUT3R_MUTE	**Individual Output Drivers Mute Control** 0 = Unmute output driver 1 = Mute output driver
JD_PGA1L_MUTE JD_PGA1R_MUTE JD_PGA2L_MUTE JD_PGA2R_MUTE JD_PGA3L_MUTE JD_PGA3R_MUTE	**Jack Detect Mute Control** 0 = Do not mute PGA when jack is detected 1 = Mute PGA when jack is detected

Figure 44 R26 – PGA Control Register 2

R27 (1Bh) – Additional Control Register 1 (ADD_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	PGA_SR[2:0]			AUTO_INC	JD_INV	GPIO2_APP	GPIO1_APP
Write	N/A							
Default	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
GPIO1_APP	**GPIO1 Application Select** 0 = Use GPIO1 as data pin for audio interface mux 1 = Use GPIO1 as input for jack detect
GPIO2_APP	**GPIO2 Application Select** 0 = Use GPIO2 as data pin for audio interface mux 1 = Use GPIO2 as input for jack detect
JD_INV	**Jack Detect Polarity** 0 = Normal (active high) 1 = Inverted (active low)
AUTO_INC	**2-wire Software Mode Auto Increment Enable** 0 = Auto increment disabled 1 = Auto increment enabled
PGA_SR[2:0]	**Sample Rate for PGA** 000 = 32kHz 001 = 44.1kHz 010 = 48kHz 011 = 88.2kHz 100 = 96kHz 101 = 176.4kHz 11X = 192kHz See Table 26 for further information on PGA sample rate versus volume ramp rate.

Figure 45 R27 – Additional Control Register 1

R28 (1Ch) – Input Control Register 1 (INPUT_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	PGA2L_IN_SEL[3:0]			
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA1R_IN_SEL[3:0]				PGA1L_IN_SEL[3:0]			
Write								
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R29 (1Dh) – Input Control Register 2 (INPUT_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	PGA3R_IN_SEL[3:0]			
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA3L_IN_SEL[3:0]				PGA2R_IN_SEL[3:0]			
Write								
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PGA1L_IN_SEL[3:0] PGA2L_IN_SEL[3:0] PGA3L_IN_SEL[3:0]	**Left Input PGA Source Selection** 0000 = No input selected 0001 = VIN1L selected 0010 = VIN2L selected 0011 = VIN3L selected 0100 = VIN4L selected 0101 = VIN5L selected 0110 = VIN6L selected 0111 = VIN7L selected 1000 = VIN8L selected 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved
PGA1R_IN_SEL[3:0] PGA2R_IN_SEL[3:0] PGA3R_IN_SEL[3:0]	**Right Input PGA Source Selection** 0000 = No input selected 0001 = VIN1R selected 0010 = VIN2R selected 0011 = VIN3R selected 0100 = VIN4R selected 0101 = VIN5R selected 0110 = VIN6R selected 0111 = VIN7R selected 1000 = VIN8R selected 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved

Figure 46 R28-29 – Input Control Registers 1-2

R30 (1Eh) – Input Control Register 3 (INPUT_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	ADC_SWITCH_EN	ADC_AMP_VOL[1:0]	
Write	N/A	N/A	N/A	N/A	N/A			
Default	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADCR_SEL[3:0]				ADCL_SEL[3:0]			
Write								
Default	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
ADCL_SEL[3:0] ADCR_SEL[3:0]	**ADC Input Select** 0000 = VIN1L 0001 = VIN2L 0010 = VIN3L 0011 = VIN4L 0100 = VIN5L 0101 = VIN6L 0110 = VIN7L 0111 = VIN8L 1000 = VIN1R 1001 = VIN2R 1010 = VIN3R 1011 = VIN4R 1100 = VIN5R 1101 = VIN6R 1110 = VIN7R 1111 = VIN8R
ADC_AMP_VOL[1:0]	**ADC Amplifier Gain Control** 00 = 0dB 01 = +3dB 10 = +6dB 11 = +12dB
ADC_SWITCH_EN	**ADC Input Switch Control** 0 = ADC input switches open 1 = ADC input switches closed

Figure 47 R30 – Input Control Register 3

R31 (1Fh) – Input Control Register 4 (INPUT_CTRL4)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read / Write	ADCR_AMP_EN	ADCL_AMP_EN	PGA3R_EN	PGA3L_EN	PGA2R_EN	PGA2L_EN	PGA1R_EN	PGA1L_EN
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PGA1L_EN PGA1R_EN PGA2L_EN PGA2R_EN PGA3L_EN PGA3R_EN	**Input PGA Enable Controls** 0 = PGA disabled 1 = PGA enabled
ADCL_AMP_EN ADCR_AMP_EN	**ADC Input Amplifier Enable Controls** 0 = Amplifier disabled 1 = Amplifier enabled

Figure 48 R31 – Input Control Register 4

R32 (20h) – Output Control Register 1 (OUTPUT_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	VOUT2L_SEL[2]
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read / **Write**	VOUT2L_SEL[1:0]		VOUT1R _SEL[2:0]			VOUT1L_SEL[2:0]		
Default	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R33 (21h) – Output Control Register 2 (OUTPUT_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	VOUT3R_SEL[2]
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read / **Write**	VOUT3R_SEL [1:0]		VOUT3L_SEL [2:0]			VOUT2R_SEL[2:0]		
Default	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**
N/A = Not Applicable (no function implemented)								

Function	Description
VOUT1L_SEL[3:0] VOUT1R_SEL [3:0] VOUT2L_SEL [3:0] VOUT2R_SEL [3:0] VOUT3L_SEL [3:0] VOUT3R_SEL [3:0]	**Output Mux Selection** 000 = PGA1L 001 = PGA1R 010 = PGA2L 011 = PGA2R 100 = PGA3L 101 = PGA3R 11X = Reserved

Figure 49 R32-33 – Output Control Registers 1-2

R34 (22h) – Output Control Register 3 (OUTPUT_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	VOUT3R_EN	VOUT3L_EN	VOUT2R_EN	VOUT2L_EN	VOUT1R_EN
Write	N/A	N/A	N/A					
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read / **Write**	VOUT1L_EN	APE_B	VOUT3R_TRI	VOUT3L_TRI	VOUT2R_TRI	VOUT2L_TRI	VOUT1R_TRI	VOUT1L_TRI
Default	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
VOUT1L_TRI VOUT1R_TRI VOUT2L_TRI VOUT2R_TRI VOUT3L_TRI VOUT3R_TRI	**Output Amplifier Tristate Control** 0 = Normal operation 1 = Output amplifier tristate enable (Hi-Z)
APE_B	**Clamp Outputs to Ground** 0 = clamp active 1 = clamp not active
VOUT1L_EN VOUT1R_EN VOUT2L_EN VOUT2R_EN VOUT3L_EN VOUT3R_EN	**Output Amplifier Enables** 0 = Output amplifier disabled 1 = Output amplifier enabled

Figure 50 R34 – Output Control Register 3

<table>
<tr><td colspan="9">R35 (23h) – Bias Control Register (BIAS)</td></tr>
<tr><td>Bit #</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit #</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Read</td><td colspan="2" rowspan="2">VMID_SEL[1:0]</td><td rowspan="2">BIAS_EN</td><td rowspan="2">SOFT_ST</td><td rowspan="2">BUFIO_EN</td><td rowspan="2">FAST_EN</td><td rowspan="2">VMIDTOG</td><td rowspan="2">POBCTRL</td></tr>
<tr><td>Write</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="9">N/A = Not Applicable (no function implemented)</td></tr>
</table>

Function	Description
POBCTRL	**Bias Source for Output Amplifiers** 0 = Output amplifiers use master bias 1 = Output amplifiers use fast bias
VMIDTOG	**VMID Power Down Characteristic** 0 = Slow ramp 1 = Fast ramp
FAST_EN	**Fast Bias Enable** 0 = Fast bias disabled 1 = Fast bias enabled
BUFIO_EN	**VMID Buffer Enable** 0 = VMID Buffer disabled 1 = VMID Buffer enabled
SOFT_ST	**VMID Soft Ramp Enable** 0 = Soft ramp disabled 1 = Soft ramp enabled
BIAS_EN	**Master Bias Enable** 0 = Master bias disabled 1 = Master bias enabled Also powers down ADCVMID
VMID_SEL[1:0]	**VMID Resistor String Value Selection (DACVMID only)** 00 = off (no VMID) 01 = 100k 10 = 500k 11 = 10k The selection is the total resistance of the string from DACREFP to DACREFN. The ADCVMID resistance is fixed at 200k.

Figure 51 R35 – Bias Control Register

R36 (24h) – PGA Control Register 3 (PGA_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	PGA_UPD	0	0
Write	N/A	N/A	N/A	N/A	N/A		N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	PGA_SEL[2:0]			PGA_FORCE
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PGA_FORCE	**PGA Ramp Control Clock Source Mux Force Update** 0 = Wait until clocks are safe before switching PGA clock source 1 = Force PGA clock source to change immediately See page 36 for details of use.
PGA_SEL[2:0]	**PGA Ramp Control Clock Source** 000 = LRCLK1 001 = LRCLK2 010 = LRCLK3 011 = LRCLK4 100 = LRCLK5 101 = DAC1LRCLK (when DAC1 is being used in master mode) 110 = DAC2LRCLK (when DAC2 is being used in master mode) 111 = ADCLRCLK (when ADC is being used in master mode)
PGA_UPD	**PGA Ramp Control Clock Source Mux Update** 0 = Do not update PGA clock source 1 = Update clock source

Figure 52 R36 – PGA Control Register 3

R37 (25h) – Audio Interface MUX Configuration Register 1 (AIF_MUX1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	PORT1_UPD	DIO1_SEL[2:1]	
Write	N/A	N/A	N/A	N/A	N/A			
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DIO1_SEL[0]	WORDCLK1_SEL[2:0]			MCLK1_SEL[2:0]			PORT1_FORCE
Write								
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
PORT1_FORCE	**Force Port 1 Clocks to Change** 0 = Wait until clocks are safe before switching between clock sources 1 = Force clock sources to change immediately See Table 40 for details of use.
MCLK1_SEL[2:0]	**MCLK1 Pin Function Select** 000 = Input to WM8593 001 = Output MCLK2 010 = Output MCLK3 011 = Output MCLK4 100 = Output MCLK5 101 to 111 = Reserved
WORDCLK1_SEL[2:0]	**BCLK1 and LRCLK1 Pins Function Select** 000 = Inputs to WM8593 001 = Source BCLK2 and LRCLK2 010 = Source BCLK3 and LRCLK3 011 = Source BCLK4 and LRCLK4 100 = Source BCLK5 and LRCLK5 101 = Source DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Source DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Source ADCBCLK and ADCBCLK (when ADC is master mode)
DIO1_SEL[2:0]	**DIO1 Pin Function Select** 000 = Input to WM8593 001 = Source DIO2 010 = Source DIO3 011 = Source DIO4 100 = Source DIO5 101 = Source GPIO1 110 = Source GPIO2 111 = Source ADC Data Output
PORT1_UPD	**Port 1 Update** 0 = Latch corresponding Port 1 settings into Register Map but do not update 1 = Latch corresponding Port 1 settings into Register Map and update all simultaneously

Figure 53 R37 – Audio Interface MUX Configuration Register 1

R38 (26h) – Audio Interface MUX Configuration Register 2 (AIF_MUX2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	PORT2_UPD	DIO2_SEL[2:1]	
Write	N/A	N/A	N/A	N/A	N/A			
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DIO2_ SEL[0]	WORDCLK2_SEL[2:0]			MCLK2_SEL[2:0]			PORT2_ FORCE
Write								
Default	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PORT2_FORCE	**Force Port 2 Clocks to Change** 0 = Wait until clocks are safe before switching between clock sources 1 = Force clock sources to change immediately See Table 40 for details of use.
MCLK2_SEL[2:0]	**MCLK2 Pin Function Select** 000 = Output MCLK1 001 = Input to WM8593 010 = Output MCLK3 011 = Output MCLK4 100 = Output MCLK5 101 to 111 = Reserved
WORDCLK2_SEL[2:0]	**BCLK2 and LRCLK2 Pins Function Select** 000 = Output BCLK1 and LRCLK1 001 = Inputs to WM8593 010 = Output BCLK3 and LRCLK3 011 = Output BCLK4 and LRCLK4 100 = Output BCLK5 and LRCLK5 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
DIO2_SEL[2:0]	**DIO2 Pin Function Select** 000 = Output DIO1 001 = Input to WM8593 010 = Output DIO3 011 = Output DIO4 100 = Output DIO5 101 = Output GPIO1 110 = Output GPIO2 111 = Output ADC Data Output
PORT2_UPD	**Port 2 Update** 0 = Latch corresponding Port 2 settings into Register Map but do not update 1 = Latch corresponding Port 2 settings into Register Map and update all simultaneously

Figure 54 R38 – Audio Interface MUX Configuration Register 2

R39 (27h) – Audio Interface MUX Configuration Register 3 (AIF_MUX3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	PORT3_UPD	DIO3_SEL[2:1]	
Write	N/A	N/A	N/A	N/A	N/A			
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DIO3_SEL[0]	WORDCLK3_SEL[2:0]			MCLK3_SEL[2:0]			PORT3_FORCE
Write								
Default	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PORT3_FORCE	**Force Port 3 Clocks to Change** 0 = Wait until clocks are safe before switching between clock sources 1 = Force clock sources to change immediately See Table 40 for details of use.
MCLK3_SEL[2:0]	**MCLK3 Pin Function Select** 000 = Output MCLK1 001 = Output MCLK2 010 = Input to WM8593 011 = Output MCLK4 100 = Output MCLK5 101 to 111 = Reserved
WORDCLK3_SEL[2:0]	**BCLK3 and LRCLK3 Pins Function Select** 000 = Output BCLK1 and LRCLK1 001 = Output BCLK2 and LRCLK2 010 = Inputs to WM8593 011 = Output BCLK4 and LRCLK4 100 = Output BCLK5 and LRCLK5 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
DIO3_SEL[2:0]	**DIO3 Pin Function Select** 000 = Output DIO1 001 = Output DIO2 010 = Input to WM8593 011 = Output DIO4 100 = Output DIO5 101 = Output GPIO1 110 = Output GPIO2 111 = Output ADC Data Output
PORT3_UPD	**Port 3 Update** 0 = Latch corresponding Port 3 settings into Register Map but do not update 1 = Latch corresponding Port 3 settings into Register Map and update all simultaneously

Figure 55 R39 – Audio Interface MUX Configuration Register 3

<table>
<tr><td colspan="9">R40 (28h) – Audio Interface MUX Configuration Register 4 (AIF_MUX4)</td></tr>
<tr><td>Bit #</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">PORT4_UPD</td><td rowspan="2" colspan="2">DIO4_SEL[2:1]</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit #</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Read</td><td rowspan="2">DIO4_
SEL[0]</td><td rowspan="2" colspan="3">WORDCLK4_SEL[2:0]</td><td rowspan="2" colspan="3">MCLK4_SEL[2:0]</td><td rowspan="2">PORT4_
FORCE</td></tr>
<tr><td>Write</td></tr>
<tr><td>Default</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td colspan="9">N/A = Not Applicable (no function implemented)</td></tr>
<tr><td colspan="2">Function</td><td colspan="7">Description</td></tr>
<tr><td colspan="2">PORT4_FORCE</td><td colspan="7">Force Port 4 Clocks to Change
0 = Wait until clocks are safe before switching between clock sources
1 = Force clock sources to change immediately
See Table 40 for details of use.</td></tr>
<tr><td colspan="2">MCLK4_SEL[2:0]</td><td colspan="7">MCLK4 Pin Function Select
000 = Output MCLK1
001 = Output MCLK2
010 = Output MCLK3
011 = Input to WM8593
100 = Output MCLK5
101 to 111 = Reserved</td></tr>
<tr><td colspan="2">WORDCLK4_SEL[2:0]</td><td colspan="7">BCLK4 and LRCLK4 Pins Function Select
000 = Output BCLK1 and LRCLK1
001 = Output BCLK2 and LRCLK2
010 = Output BCLK3 and LRCLK3
011 = Inputs to WM8593
100 = Output BCLK5 and LRCLK5
101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode)
110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode)
111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)</td></tr>
<tr><td colspan="2">DIO4_SEL[2:0]</td><td colspan="7">DIO4 Pin Function Select
000 = Output DIO1
001 = Output DIO2
010 = Output DIO3
011 = Input to WM8593
100 = Output DIO5
101 = Output GPIO1
110 = Output GPIO2
111 = Output ADC Data Output</td></tr>
<tr><td colspan="2">PORT4_UPD</td><td colspan="7">Port 4 Update
0 = Latch corresponding Port 4 settings into Register Map but do not update
1 = Latch corresponding Port 4 settings into Register Map and update all simultaneously</td></tr>
</table>

Figure 56 R40 – Audio Interface MUX Configuration Register 4

R41 (29h) – Audio Interface MUX Configuration Register 5 (AIF_MUX5)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	PORT5_UPD	DIO5_SEL[2:1]	
Write	N/A	N/A	N/A	N/A	N/A			
Default	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DIO5_ SEL[0]	WORDCLK5_SEL[2:0]			MCLK5_SEL[2:0]			PORT5_ FORCE
Write								
Default	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PORT5_FORCE	**Force Port 5 Clocks to Change** 0 = Wait until clocks are safe before switching between clock sources 1 = Force clock sources to change immediately See Table 40 for details of use.
MCLK5_SEL[2:0]	**MCLK5 Pin Function Select** 000 = Output MCLK1 001 = Output MCLK2 010 = Output MCLK3 011 = Output MCLK4 100 = Input to WM8593 101 to 111 = Reserved
WORDCLK5_SEL[2:0]	**BCLK5 and LRCLK5 Pins Function Select** 000 = Output BCLK1 and LRCLK1 001 = Output BCLK2 and LRCLK2 010 = Output BCLK3 and LRCLK3 011 = Output BCLK4 and LRCLK4 100 = Inputs to WM8593 101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
DIO5_SEL[2:0]	**DIO5 Pin Function Select** 000 = Output DIO1 001 = Output DIO2 010 = Output DIO3 011 = Output DIO4 100 = Input to WM8593 101 = Output GPIO1 110 = Output GPIO2 111 = Output ADC Data Output
PORT5_UPD	**Port 5 Update** 0 = Latch corresponding Port 5 settings into Register Map but do not update 1 = Latch corresponding Port 5 settings into Register Map and update all simultaneously

Figure 57 R41 – Audio Interface MUX Configuration Register 5

<table>
<tr><td colspan="9">R42 (2Ah) – Audio Interface MUX Configuration Register 6 (AIF_MUX6)</td></tr>
<tr><td>Bit #</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">DAC1_UPD</td><td rowspan="2" colspan="2">DAC1DIN_SEL[2:1]</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit #</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Read</td><td rowspan="2">DAC1DIN_
SEL[0]</td><td rowspan="2" colspan="3">DAC1WORDCLK_SEL[2:0]</td><td rowspan="2" colspan="3">DAC1MCLK_SEL[2:0]</td><td rowspan="2">DAC1_
FORCE</td></tr>
<tr><td>Write</td></tr>
<tr><td>Default</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td colspan="9">N/A = Not Applicable (no function implemented)</td></tr>
<tr><td colspan="2">Function</td><td colspan="7">Description</td></tr>
<tr><td colspan="2">DAC1_FORCE</td><td colspan="7">Force DAC1 Clocks to Change
0 = Wait until clocks are safe before switching between clock sources
1 = Force clock sources to change immediately
See Table 40 for details of use.</td></tr>
<tr><td colspan="2">DAC1MCLK_SEL[2:0]</td><td colspan="7">DAC1MCLK Select
000 = Use MCLK1
001 = Use MCLK2
010 = Use MCLK3
011 = Use MCLK4
100 = Use MCLK5
101 to 111 = Reserved</td></tr>
<tr><td colspan="2">DAC1WORDCLK_
SEL[2:0]</td><td colspan="7">DAC1BCLK and DAC1LRCLK Select
000 = Use BCLK1 and LRCLK1
001 = Use BCLK2 and LRCLK2
010 = Use BCLK3 and LRCLK3
011 = Use BCLK4 and LRCLK4
100 = Use BCLK5 and LRCLK5
101 = Output DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode)
110 = Use DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode)
111 = Use ADCBCLK and ADCBCLK (when ADC is master mode)</td></tr>
<tr><td colspan="2">DAC1DIN_SEL[2:0]</td><td colspan="7">DAC1DIN Select
000 = Use DIO1
001 = Use DIO2
010 = Use DIO3
011 = Use DIO4
100 = Use DIO5
101 = Use GPIO1
110 = Use GPIO2
111 = Use ADCDOUT</td></tr>
<tr><td colspan="2">DAC1_UPD</td><td colspan="7">DAC1 Clock Update
0 = Latch corresponding DAC1 clock settings into Register Map but do not update
1 = Latch corresponding DAC1 clock settings into Register Map and update all simultaneously</td></tr>
</table>

Figure 58 R42 – Audio Interface MUX Configuration Register 6

<table>
<tr><td colspan="9">R43 (2Bh) – Audio Interface MUX Configuration Register 7 (AIF_MUX7)</td></tr>
<tr><td>Bit #</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">DAC2_UPD</td><td rowspan="2" colspan="2">DAC2DIN_SEL[2:1]</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit #</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Read</td><td rowspan="2">DAC2DIN_
SEL[0]</td><td rowspan="2" colspan="3">DAC2WORDCLK_SEL[2:0]</td><td rowspan="2" colspan="3">DAC2MCLK_SEL[2:0]</td><td rowspan="2">DAC2_
FORCE</td></tr>
<tr><td>Write</td></tr>
<tr><td>Default</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td colspan="9">N/A = Not Applicable (no function implemented)</td></tr>
<tr><td colspan="2">Function</td><td colspan="7">Description</td></tr>
<tr><td colspan="2">DAC2_FORCE</td><td colspan="7">Force DAC2 Clocks to Change
0 = Wait until clocks are safe before switching between clock sources
1 = Force clock sources to change immediately
See Table 40 for details of use.</td></tr>
<tr><td colspan="2">DAC2MCLK_SEL[2:0]</td><td colspan="7">DAC2MCLK Select
000 = Use MCLK1
001 = Use MCLK2
010 = Use MCLK3
011 = Use MCLK4
100 = Use MCLK5
101 to 111 = Reserved</td></tr>
<tr><td colspan="2">DAC2WORDCLK_
SEL[2:0]</td><td colspan="7">DAC2BCLK and DAC2LRCLK Select
000 = Use BCLK1 and LRCLK1
001 = Use BCLK2 and LRCLK2
010 = Use BCLK3 and LRCLK3
011 = Use BCLK4 and LRCLK4
100 = Use BCLK5 and LRCLK5
101 = Use DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode)
110 = Output DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode)
111 = Use ADCBCLK and ADCBCLK (when ADC is master mode)</td></tr>
<tr><td colspan="2">DAC2DIN_SEL[2:0]</td><td colspan="7">DAC2DIN Select
000 = Use DIO1
001 = Use DIO2
010 = Use DIO3
011 = Use DIO4
100 = Use DIO5
101 = Use GPIO1
110 = Use GPIO2
111 = Use ADCDOUT</td></tr>
<tr><td colspan="2">DAC2_UPD</td><td colspan="7">DAC2 Clock Update
0 = Latch corresponding DAC2 clock settings into Register Map but do not update
1 = Latch corresponding DAC2 clock settings into Register Map and update all simultaneously</td></tr>
</table>

Figure 59 R43 – Audio Interface MUX Configuration Register 7

R44 (2Ch) – Audio Interface MUX Configuration Register 8 (AIF_MUX8)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	ADC_UPD	0	0
Write	N/A	N/A	N/A	N/A	N/A		N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	ADCWORDCLK_SEL[2:0]			ADCMCLK_SEL[2:0]			ADC_ FORCE
Write	N/A							
Default	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
ADC_FORCE	**Force ADC Clocks to Change** 0 = Wait until clocks are safe before switching between clock sources 1 = Force clock sources to change immediately See Table 40 for details of use.
ADCMCLK_SEL[2:0]	**ADCMCLK Select** 000 = Use MCLK1 001 = Use MCLK2 010 = Use MCLK3 011 = Use MCLK4 100 = Use MCLK5 101 to 111 = Reserved
ADCWORDCLK_ SEL[2:0]	**ADCBCLK and ADCLRCLK Select** 000 = Use BCLK1 and LRCLK1 001 = Use BCLK2 and LRCLK2 010 = Use BCLK3 and LRCLK3 011 = Use BCLK4 and LRCLK4 100 = Use BCLK5 and LRCLK5 101 = Use DAC1BCLK and DAC1LRCLK (when DAC1 is in master mode) 110 = Use DAC2BCLK and DAC2LRCLK (when DAC2 is in master mode) 111 = Output ADCBCLK and ADCBCLK (when ADC is master mode)
ADC_UPD	**ADC Clock Update** 0 = Latch corresponding ADC clock settings into Register Map but do not update 1 = Latch corresponding ADC clock settings into Register Map and update all simultaneously

Figure 60 R44 – Audio Interface MUX Configuration Register 8

<table>
<tr><th colspan="9">R45 (2Dh) – Audio Interface MUX Configuration Register 9 (AIF_MUX9)</th></tr>
<tr><th>Bit #</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">GPIO1_UPD</td><td>0</td><td>0</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><th>Bit #</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2" colspan="3">GPIO1_SEL[2:0]</td><td>0</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="9">N/A = Not Applicable (no function implemented)</td></tr>
</table>

Function	Description
GPIO1_SEL[2:0]	**GPIO1 Pin Function Select** 000 = Source DIO1 001 = Source DIO2 010 = Source DIO3 011 = Source DIO4 100 = Source DIO5 101 = Input to WM8593 110 = Source GPIO2 111 = Source ADC Data Output
GPIO1_UPD	**GPIO1 Update** 0 = Latch corresponding GPIO1 settings into Register Map but do not update 1 = Latch corresponding GPIO1 settings into Register Map and update

Figure 61 R45 – Audio Interface MUX Configuration Register 9

<table>
<tr><th colspan="9">R46 (2Eh) – Audio Interface MUX Configuration Register 10 (AIF_MUX10)</th></tr>
<tr><th>Bit #</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">GPIO2_UPD</td><td>0</td><td>0</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><th>Bit #</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2" colspan="3">GPIO2_SEL[2:0]</td><td>0</td></tr>
<tr><td>Write</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>Default</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="9">N/A = Not Applicable (no function implemented)</td></tr>
</table>

Function	Description
GPIO2_SEL[2:0]	**GPIO2 Pin Function Select** 000 = Source DIO1 001 = Source DIO2 010 = Source DIO3 011 = Source DIO4 100 = Source DIO5 101 = Input to WM8593 110 = Source GPIO2 111 = Source ADC Data Output
GPIO2_UPD	**GPIO2 Update** 0 = Latch corresponding GPIO2 settings into Register Map but do not update 1 = Latch corresponding GPIO2 settings into Register Map and update all simultaneously

Figure 62 R46 – Audio Interface MUX Configuration Register 10

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	± 0.05dB			0.454fs	
Passband Ripple				0.05	dB
Stopband		0.546fs			
Stopband Attenuation		-60			dB
Group Delay			16		fs
DAC Filter – 32kHz to 96kHz					
Passband	± 0.1dB			0.454fs	
Passband Ripple				0.1	dB
Stopband		0.546fs			
Stopband attenuation	f > 0.546fs	-50			dB
Group Delay			10		Fs
DAC Filter – 176.4kHz to 192kHz					
Passband	± 0.1dB			0.247fs	
Passband Ripple				0.1	dB
Stopband		0.753fs			
Stopband attenuation	f > 0.546fs	-50			dB
Group Delay			10		Fs

DAC FILTER RESPONSES

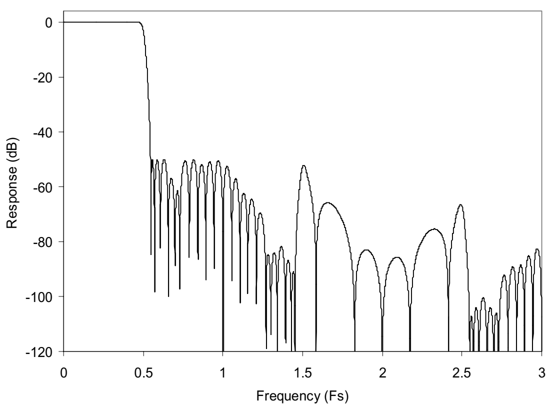


Figure 63 DAC Digital Filter Frequency Response – 44.1, 48 and 96KHz

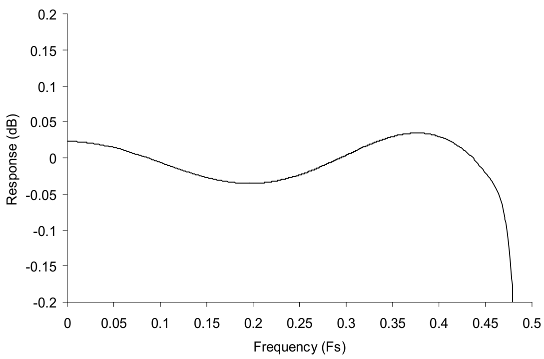


Figure 64 DAC Digital Filter Ripple –44.1, 48 and 96kHz

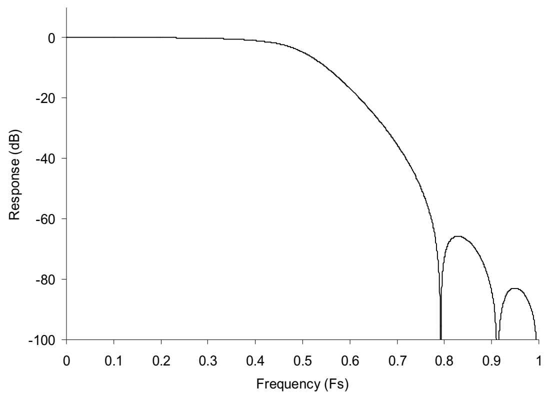


Figure 65 DAC Digital Filter Frequency Response – 192KHz

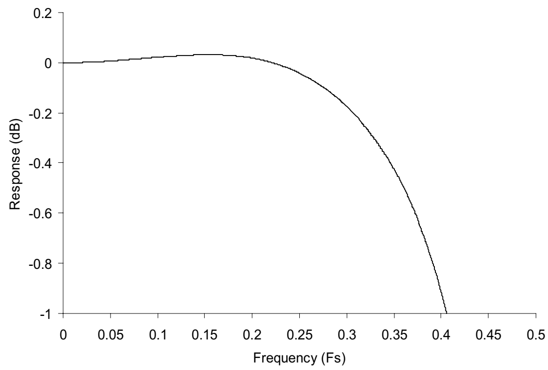


Figure 66 DAC Digital Filter Ripple – 192kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

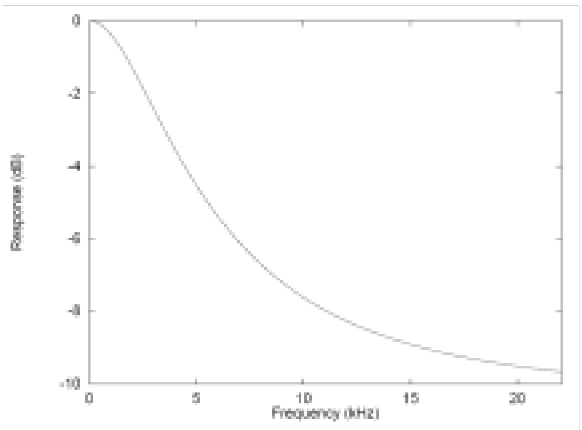


Figure 67 De-Emphasis Frequency Response (44.1KHz)

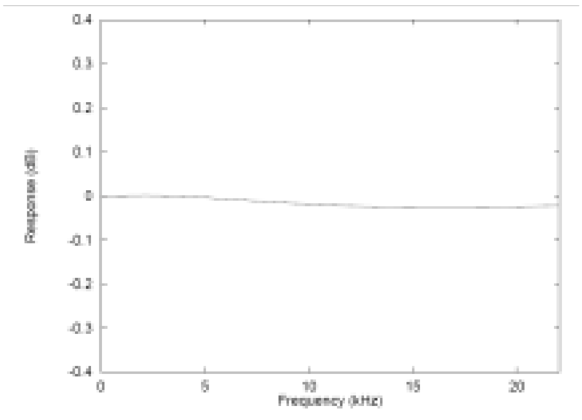


Figure 68 De-Emphasis Error (44.1KHz)

ADC FILTER RESPONSES

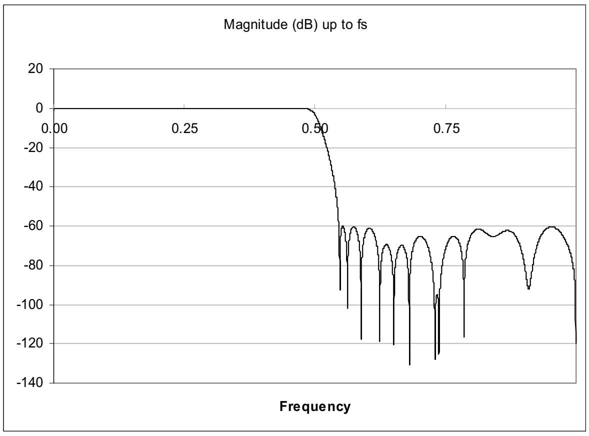


Figure 69 ADC Digital Filter Frequency Response

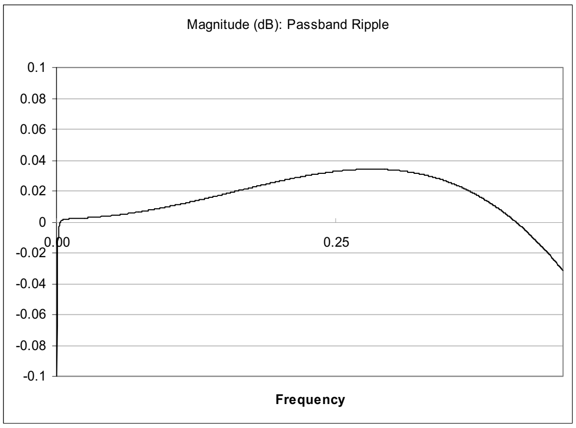


Figure 70 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8593 has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

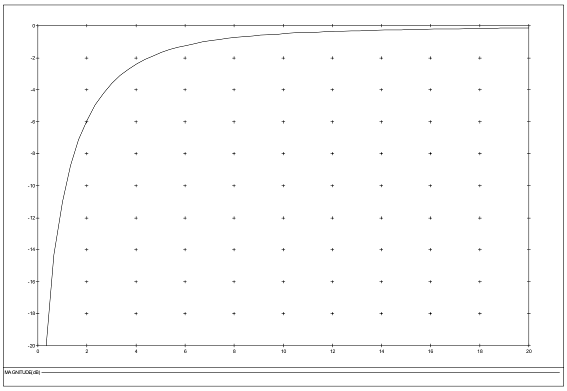
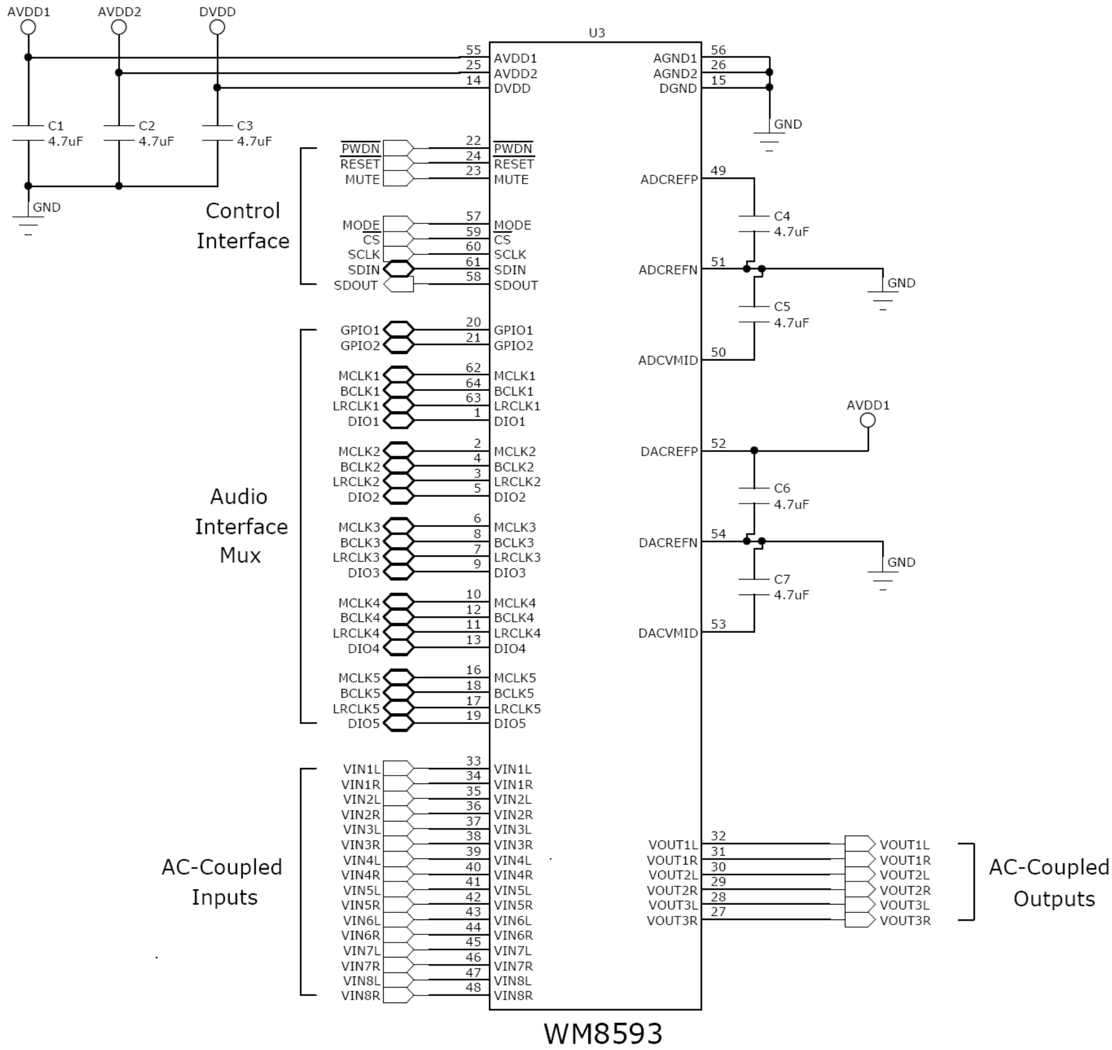


Figure 71 ADC Highpass Filter Response

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



Notes:

1. AGND and DGND should ideally share a continuous ground plane. Where this is not possible, it is recommended that AGND and DGND are connected as close to the WM8593 as possible.

2. Decoupling capacitors shown are very low-ESR, multilayer ceramic capacitors and should be placed as near to the WM8593 as possible. Equally good results may be obtained using 0.1µF ceramic capacitors near to the WM8593, with a 10µF electrolytic capacitor nearby.

RECOMMENDED ANALOGUE LOW PASS FILTER

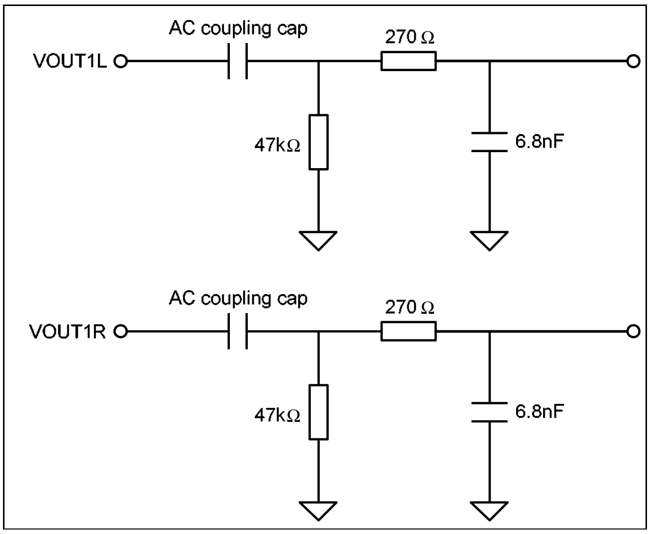


Figure 72 Recommended Analogue Low Pass Filter (shown for VOUT1L/R)

Note: See WAN0176 for AC coupling capacitor selection information.

An external single pole RC filter is recommended (see Figure 72) if the device is driving a wideband amplifier. Other filter architectures may provide equally good results.

EXTENDED INPUT IMPEDANCE CONFIGURATION

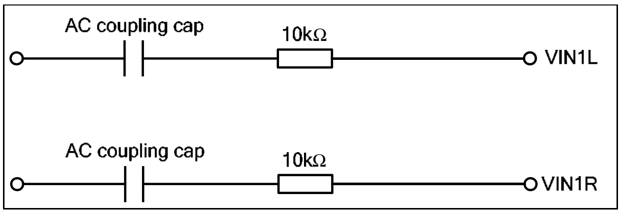


Figure 73 Extended Input Impedance Configuration

Note: See WAN0176 for AC coupling capacitor selection information.

The input impedance to the WM8593 is specified in the Electrical Characteristics section beginning on p8, and is fixed across gain setting and signal routing options. If this input impedance is not enough for the intended application, an alternative input configuration (Figure 73) is possible.

This configuration increases the input impedance to the WM8593 by 10kΩ, but reduces the overall gain in the ADC and Bypass paths by -6dB. In order to compensate for this reduction in gain, +6dB of gain should be set in the ADC Input PGA (by using ADC_AMP_VOL[1:0]) and in the bypass PGA (by using PGAxx_VOL[7:0]).

Examples:

- If a $2V_{RMS}$ signal is applied to VIN1L and VIN1R and routed to VOUT1L and VOUT1R using PGA1L and PGA1R, then setting PGA1L_VOL[7:0] and PGA1R_VOL[7:0] =0x00 is necessary to see $2V_{RMS}$ at VOUT1L and VOUT1R.
- If a $2V_{RMS}$ signal is applied to VIN1L and VIN1R and routed to ADCL and ADCR, then setting ADC_AMP_VOL[1:0]=10 is necessary to see 0dBFS at the ADC outputs.

EXAMPLE CONFIGURATION FOR JACK DETECT

The WM8593 contains a jack detect function as described on page 54. In order to use this function, it is necessary to connect the required GPIO pin to the headphone connector to detect the insertion of the jack. Figure 74 shows a typical connection scheme:

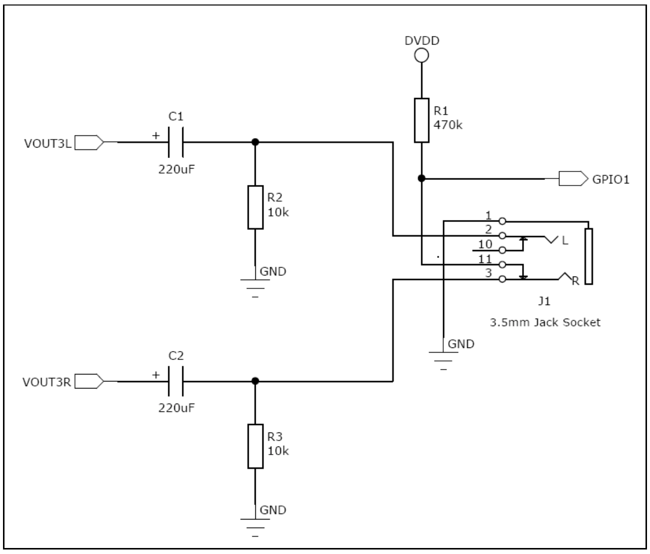


Figure 74 Example Jack Detect Circuitry

When a jack is not inserted, the mechanical switch in the 3.5mm jack socket is closed and a short between pin 11 and pin 3 is present. There is a potential divider between DVDD and GND formed by R1 and R3, and this causes the voltage level at GPIO1 to be:

DVDD * [R3 / (R1 +R3)] = DVDD * [10 / (470 + 10)] = 0.02 * DVDD = logic 0

When a jack is inserted, the mechanical switch in the 3.5mm jack socket is opened and there is no longer a short between pin 11 and pin 3. The voltage level at GPIO1 is then pulled up to DVDD through R1 and is therefore logic 1. Therefore, the function of the circuit in Figure 74 is:

JACK STATUS	LOGIC LEVEL AT GPIO1
Not Inserted	Logic 0
Inserted	Logic 1

Table 45 Example Jack Detect Configuration Operation

RELEVANT APPLICATION NOTES

The following application notes, available from www.wolfsonmicro.com, may provide additional guidance for the use of the WM8593.

DEVICE PERFORMANCE:

WAN0129 – Decoupling and Layout Methodology for Wolfson DACs, ADCs and CODECs

WAN0144 – Using Wolfson Audio DACs and CODECs with Noisy Supplies

WAN0176 – AC Coupling Capacitor Selection

GENERAL:

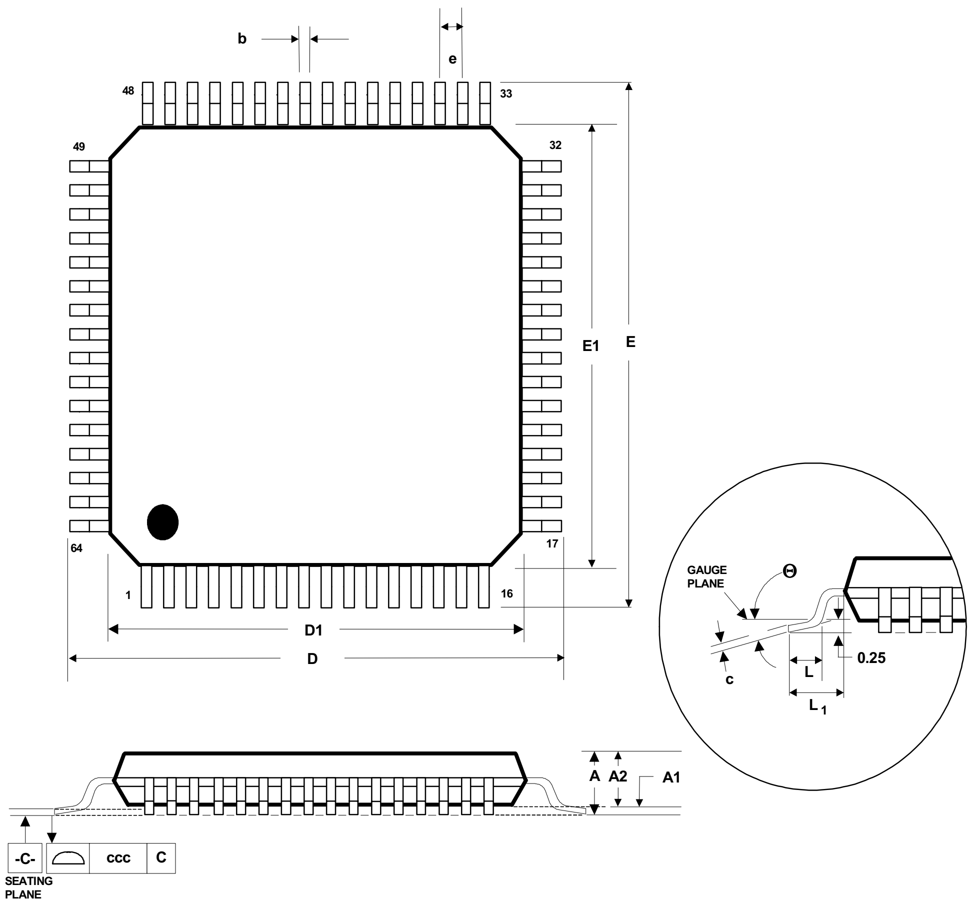
WAN0108 – Moisture Sensitivity Classification and Plastic IC Packaging

WAN0109 – ESD Damage in Integrated Circuits: Causes and Prevention

WAN0158 – Lead-Free Solder Profiles for Lead-Free Components

PACKAGE DIMENSIONS

FT: 64 PIN TQFP (10 x 10 x 1.0 mm) **DM027.B**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	12.00 BSC		
D_1	10.00 BSC		
E	12.00 BSC		
E_1	10.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
Θ	0^o	3.5^o	7^o
	Tolerances of Form and Position		
ccc	0.08		
REF:	JEDEC.95, MS-026, VARIATION ACD		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ACD. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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