Ordering number: EN 4375

Thick-film Hybrid Integrated Circuit (HIC)

SANYO No.4375

STK301-020

7-band, 2-channel Electronic Graphic Equalizer

Overview

The STK301-020 is a hybrid IC (HIC) for electronically controlled graphic equalizer applications and is equipped with on-chip electronic volume for 7-band, 2-channel graphic equalization thereby permiting one-touch up-down control of all band gains. The STK301-020 is a hybrid IC which combines SC system and photoresist techniques with folded board construction while incorporating Sanyo's unique insulated metal substrate technology (IMST) to the base.

Applications

- Car stereos
- Portable radio-cassette players
- Home stereos

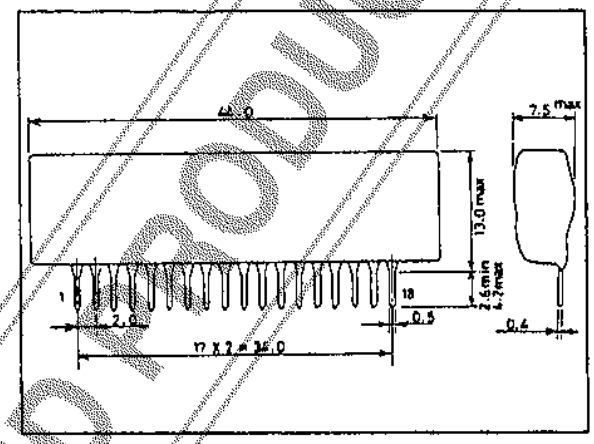
Features

- All bands are set for L/R simultaneous 2 dB incremental operation (typ).
- All bands are equipped with 13 positions and range between +12 dB maximum boost to –12 dB maximum cut.
- Crossover frequencies include fo; 60 Hz, 150 Hz, 400 Hz, 1 kHz, 2.5 kHz, 6 kHz and 15 kHz.
- The following features can be made available with an electronic graphic equalizer system which incorporates the 3-IC construction consisting of the STK301-020, a controller (LC7060 or universal microcontroller such as LC6502) along with the display LSI (LC7560→LCD, LC7565→FLT, LED).
  1) One-touch up-down control of all band gains.
  2) Immediate recall of preferred frequency levels tailored to suit musical selections. This is possible using preset functions to retrieving items from one-touch memory.
  3) Such functions as setting all bands to 0 dB (flat function), or switching frequency characteristics from 0 dB to center (reverse function) may be simply performed with supported software.
  4) Dual control lines permit mutual use with display LSI and help to simplify wiring between microcontroller and LSI.

Package Dimensions

unit : mm

4133



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

				unit
Maximum supply voltage	V_{DD}-V_{EE} max		16	V
	$V_{CC}1$ max		20	V
	$V_{CC}2$ max		7	V
Input voltage	V_I1	CLK, DI, IN1, IN2	0 to $V_{CC}2$ + 0.3	V
	V_I2	CLK, DI, IN1, IN2	V_{EE}–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		1080	mW
Operating temperature	Topg		–20 to +70	°C
Storage temperature range	Tstg		–40 to +100	°C

Specifications and information herein are subject to change without notice.

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Recommended Operational Voltage at Ta = 25 °C, V_{SS} = 0 V

				unit
Supply voltage	V_{DD}-V_{EE}, $V_{CC}1$	V_{EE} = V_{SS} = 0V	14	V
	$V_{CC}2$	V_{EE} = V_{SS} = 0V	5	V

Allowable Operating Conditions at Ta = 25°C, V_{SS} = 0V

				unit
Supply voltage	V_{DD}-V_{EE}, $V_{CC}1$		7.5 to 15.0	V
	$V_{CC}2$		4.5 to 5.5	V
"H" Level input voltage	V_{IH}	CLK, DI	0.8$V_{CC}2$ to $V_{CC}2$	V
"L" Level input voltage	V_{IL}	CLK, DI	0.2$V_{CC}2$	V
Input pulse width	t_{pW}	CLK	1 to	μs
Setup time	t_{setup}	DI	1 to	μs
Hold time	t_{hold}	DI	1 to	μs
Operational frequency	f_{opg}	CLK	to 330	kHz

Operating Characteristics

at Ta = 25°C, V_{SS} = V_{EE} = 0V, V_{DD} = $V_{CC}1$ = 14V, $V_{CC}2$ = 5V

All bands flat, via specified Test Circuit

			min	typ	max	unit
Current consumption	I_{DD}	V_{SS} = V_{EE} = 0V, V_{DD} = $V_{CC}1$ = 14V, $V_{CC}2$ = 5V			1	mA
	$I_{CC}1$			23	32	mA
	$I_{CC}2$				1	mA
Current consumption 2	I_{DD}	$V_{CC}1$ = ±7V, V_{DD}/V_{EE} = ±7V			1	mA
	$I_{CC}1$	$V_{CC}1$ = ±7V, V_{DD}/V_{EE} = ±7V		23	32	mA
Voltage gain	VG	V_{IN} = -10dBm	-4.8	-1.8	+1.2	dB
Total harmonic distortion	THD	f = 1kHz, V_O = 1V, 30kHz L.P.F		0.02	0.1	%
Crosstalk	C.T.	f = 20kHz, V_{IN} = 0dBm	45	55		dB
Output noise voltage	V_{NO}	Rg = 0Ω, 10Hz to 30kHz B.P.F		7	40	μV
Setting error	ΔB		-1		+1	dB
Frequency response	f (1)	f = 60Hz	±10	±12	±14	dB
	f (2)	f = 150Hz	±10	±12	±14	dB
	f (3)	f = 400Hz	±10	±12	±14	dB
	f (4)	f = 1kHz	±10	±12	±14	dB
	f (5)	f = 2.5k	±10	±12	±14	dB
	f (6)	f = 6kHz	±10	±12	±14	dB
	f (7)	f = 15kHz	±10	±12	±14	dB

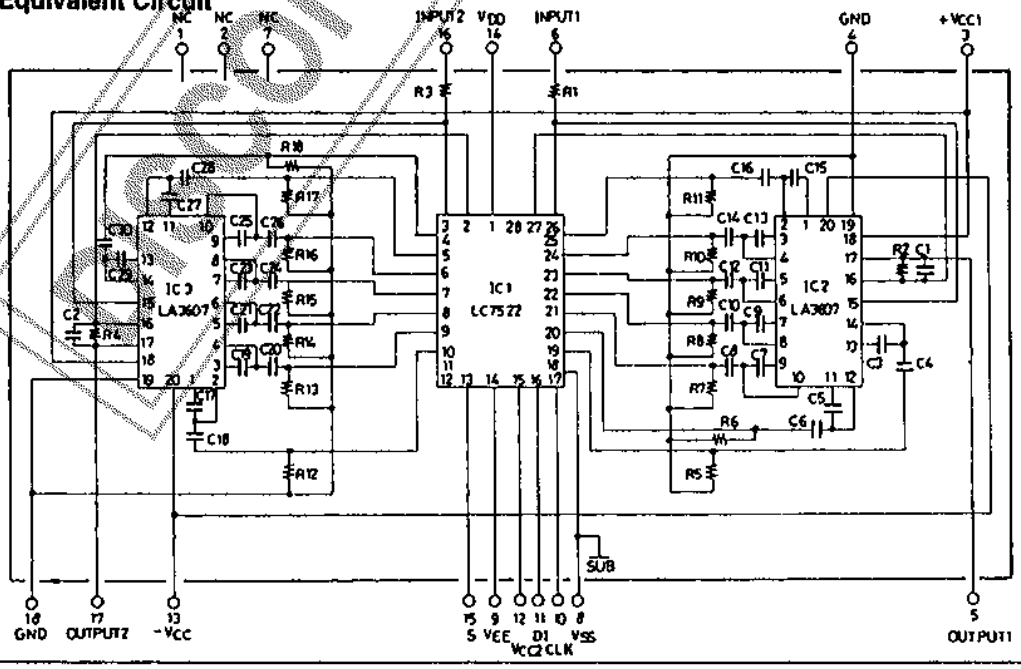
When operating at f = 1 kHz, all bands flat and V_O = -10 dB set at 0 dB

Note: With constant voltage power supply.

In addition to the above items, the STK301-020 is joined by STK301-020A and STK301-020B which differ in crossover frequency.

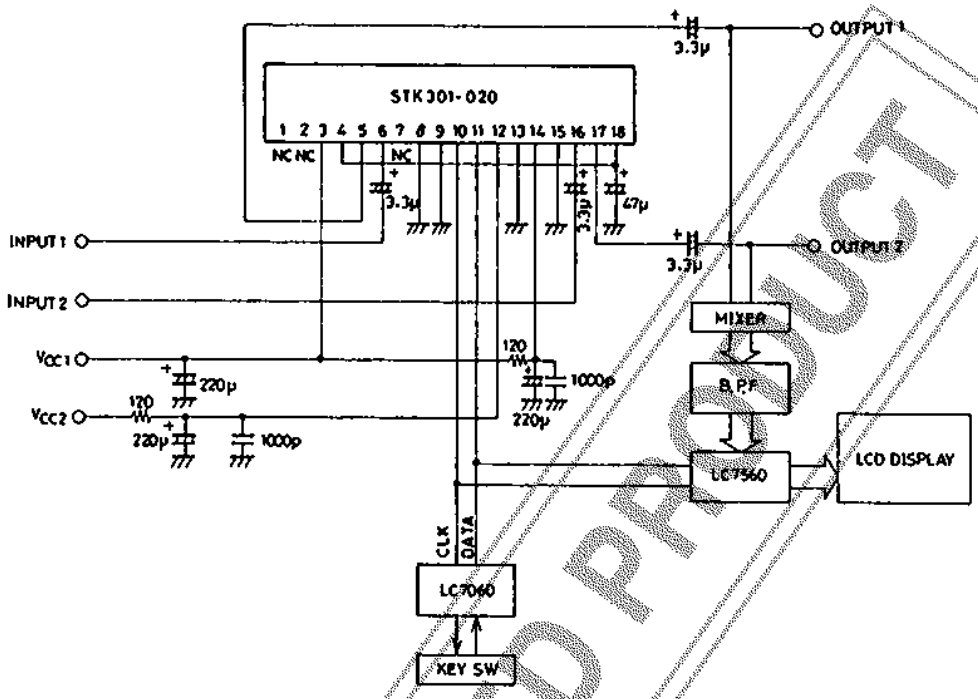
IC name	f (1)	f (2)	f (3)	f (4)	f (5)	f (6)	f (7)
STK301-020	60Hz	150Hz	400Hz	1kHz	2.5kHz	6kHz	15kHz
STK301-020A	60Hz	126Hz	250Hz	500Hz	1kHz	3.5kHz	10kHz
STK301-020B	60Hz	125Hz	250Hz	500Hz	1kHz	3.5kHz	12kHz

Internal Equivalent Circuit

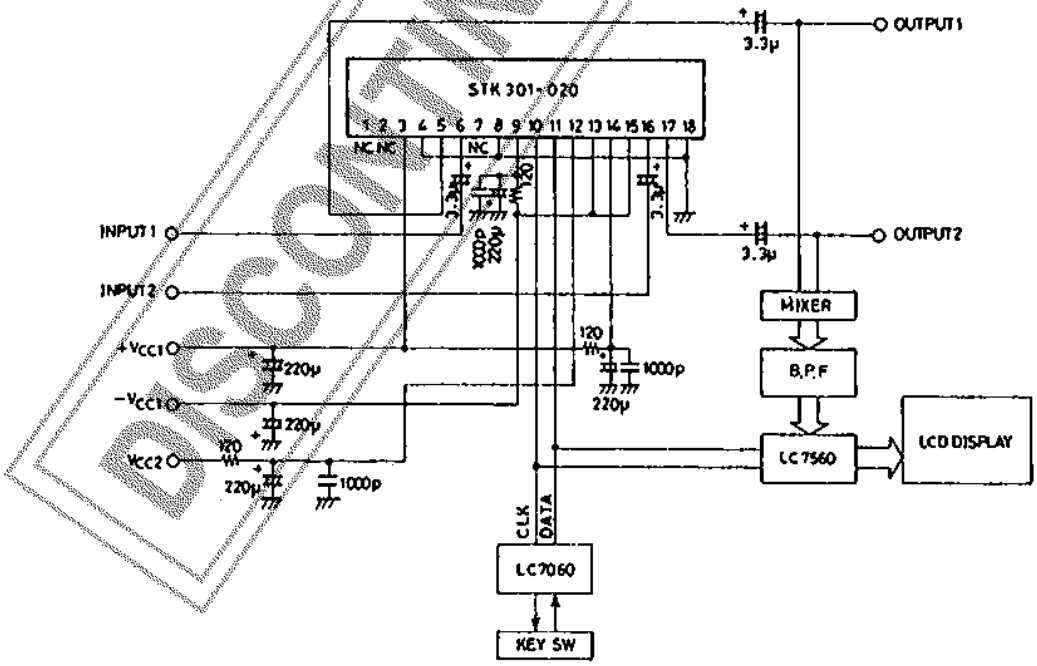


Application Circuit Example

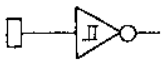
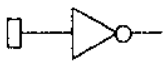
■ + Power Supply



■ ± Power Supply



Pin Descriptions

Pin No.	Pin name	Functions	
3	$+V_{CC}1$	Power supply pin used for + power supply to IC2 and IC3 graphic equalizer.	
4, 18	DC	Pin for 1/2 $V_{CC}1$ decoupling capacitor of graphic equalizer IC. When shortened, power supply becomes more effective and ripples are vulnerable.	
5	OUTPUT 1	Output pin 1.	
6	INPUT 1	Input impedance for input pin 1 rated at approximately 60Ω (1 kHz, flat).	
8	V_{SS}	Power supply pin connected to ground (GND).	
9	V_{EE}	Power supply pin used for audio signal power supply to electronic volume section. When single power supply is used, connect to V_{SS}.	
10	CLK		Input pin for data from CPU according to Schmitt inverter format.
11	DI		Input pin for clock from the CPU according to Schmitt inverter format.
12	$+V_{CC}2$	Power supply pin rated at +5 V (typ). Make sure that $V_{CC}2$ does not onset before V_{DD}.	
13	GND ($-V_{CC}1$)	Power supply pin for ground (- power supply) of IC2 and IC3 graphic equalizer.	
14	V_{DD}	Power supply pin used for audio signal power supply to electronic volume section.	
15	S		Select pin for applications using two ICs. Input "1" to initiate key code 7C3 for connecting to V_{DD}. Input "2" to initiate key code 7C2 for connecting to V_{EE}.
16	INPUT 2	Input impedance for input pin 2 rated at approximately 60Ω (1 kHz, flat).	
17	OUTPUT 2	Output pin 2.	

Note: 1. Pins 1, 2, 7 are designated as NC pins (pins with no connections).

2. Refer to LC7522 or LC7523 specifications concerning pins which do not appear here and are hybrid IC (HIC) pins connected directly to a LC7522 or LC7523 pins.

Description of Operation

The STK301-020 is a hybrid IC (HIC) with a 7 – component 2-channel construction for electronically controlled graphic equalizer applications. It employees a LC7522 for graphic equalizer electronic volume and a LA3607 for 7 – component graphic equalizer functions.

Equivalent Circuit Block Diagram

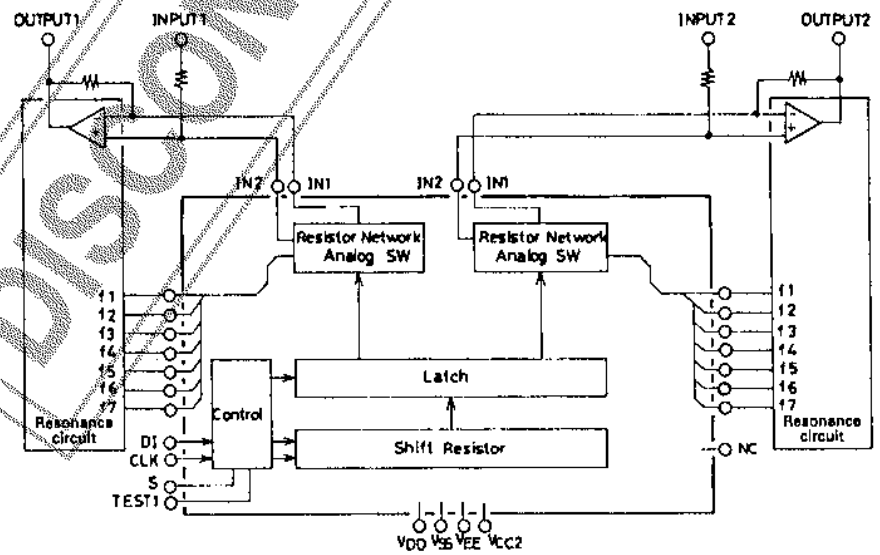
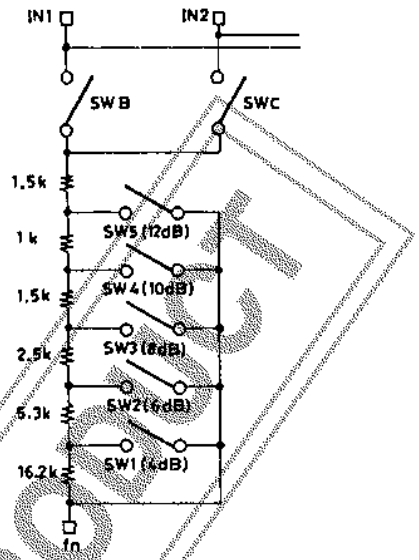


Fig. 1 Equivalent Circuit Block Diagram

Pins f(1) through f(7) are used as pin connections for the LC7522 band filter. Supported frequencies and their pin assignments are listed in the following.

Pin Name	Frequency
f (1)	60Hz
f (2)	150Hz
f (3)	400Hz
f (4)	1kHz
f (5)	2.5kHz
f (6)	6kHz
f (7)	15kHz

In order to minimize the noise which occurs during changeover, connections are made using 1 MΩ resistors from pins f(1) through f(7) to 1/2 V_{CC}1.



Resistor Equivalent Circuit
(single band)

Principles of Operation

The graphic equalizer section is constructed from 7 resonance circuits and output buffer amplifiers (every channel); variable resistors (LC7522) and resonance circuit capacitors C1 and C2 are built-in. Resonance circuits utilize semiconductor inductors and apply resonation to reduced impedance; all frequency gains are altered.

(1) Resonance Circuit

Semiconductor inductors replace the L of the R, L, C series resonance circuit with a CR element passing through the buffer function of active elements such as the transistor and op-amp (operational amplifier) thereby effecting the equivalent operation of a R, L, C series resonance circuit. The STK301-020 resonance circuit buffer is constructed using transistors and arranged as illustrated in Figure 2.

Resonance frequency f_0 is determined using the following formula:

$$f_0 = \frac{1}{2\pi\sqrt{C1 \cdot C2 \cdot R1 \cdot R2}}$$

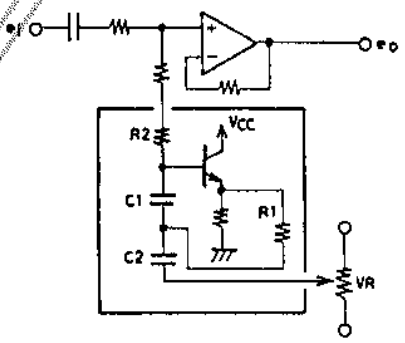
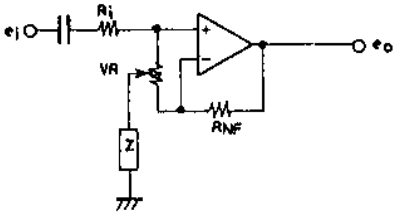


Fig. 2 Resonance Circuit

(2) Flat, Boost and Cut

Gains matching resonance circuit frequency gains are altered by altering the built-in resonance circuits and electronic volume. Figure 3 is presented to describe the equivalent circuit. Z represents the impedance of the resonance circuit in Figure 2.

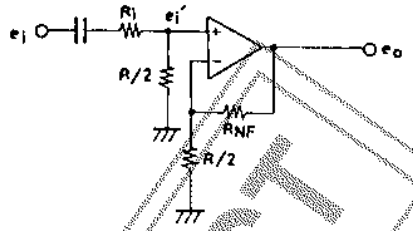


Z : Resonance circuit impedance
VR : Equivalent to LC7522

Fig. 3 Equivalent Circuit

(3) Flat

When the volume is set to the midrange position and Ri=R_{NF}, the following relationships are established:



$$ei' = \frac{R/2}{Ri = R/2} \cdot ei$$

$$A_V = \frac{R_{NF} + R/2}{R/2} \text{ in which}$$

$$eo = A_V \cdot ei' = ei$$

with no relation to the resonance circuit and frequency characteristics become flat.

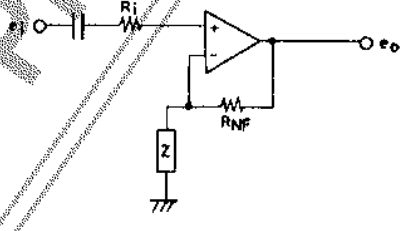
When VR is set to R, the resistance value using a VR sector position becomes R/2.

(4) Boost

When the volume is set to the boost position, resonance circuit is linked to the NF loop of the output buffer amplifier. Under these circumstances and when R≫Ri and R_{NF}, the following relationship exist:

$$A_V = \frac{R_{NF} + Z}{Z}$$

is established and output voltage$_{eo}$ is calculated as

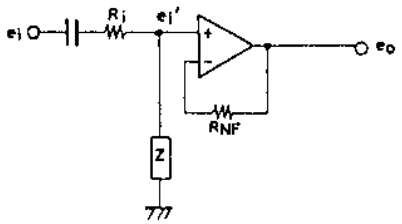


$$eo = A_V \cdot ei = \frac{R_{NF} + Z}{Z} \cdot ei$$

The gain becomes a minimum when the resonance circuit has Z at a minimum so that the frequency option is boosted.

(5) Cut

When volume is set to the cut side, resonance circuit is linked to the input side of the output buffer amplifier. Under these circumstances and when ignoring R similarly to boost, the following relationship exist:



$$ei' = \frac{Z}{Ri+Z} \cdot ei, \; A_V = 1$$

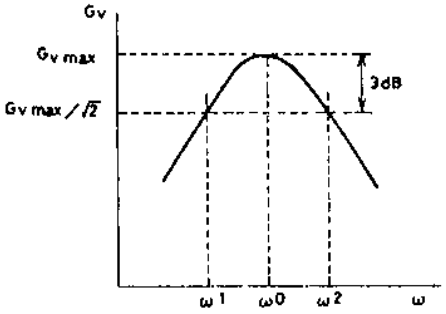
is established and output voltage$_{eo}$ is calculated as

$$eo = A_V \cdot ei' = \frac{Z}{Ri+Z} \cdot ei$$

The gain becomes a minimum when the resonance circuit has Z at a minimum so that the frequency option is cut.

(6) Resonance Circuit Crest Acuteness (Q)

Resonance circuit crest acuteness is determined by comparing frequency widths ϖ2 - ϖ1 for G_V max/$\sqrt{2}$ where G_V max represents point ϖ0 as the maximum value of the resonance circuit crest.

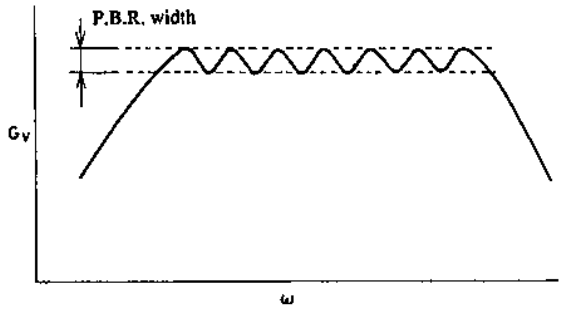


The following formula is used to calculate the value for Q:

$$Q = \sqrt{\frac{C1 \cdot R2}{C2 \cdot R1}}$$

As the value for Q becomes larger, the participating frequency bandwidth of the resonance circuit becomes narrower. Although neighboring bands distinction is precise, the swell of frequency characteristics under total boost is larger while the peak of the resultant frequency is lowered.

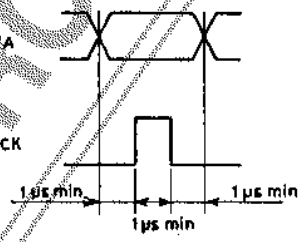
With the STK301-020, few crossover bands exist with an increase in swell during total boost. Pass-band-ripple (P.B.R.) width at this time is 4 dB with Q set at 3.5 fore and aft.

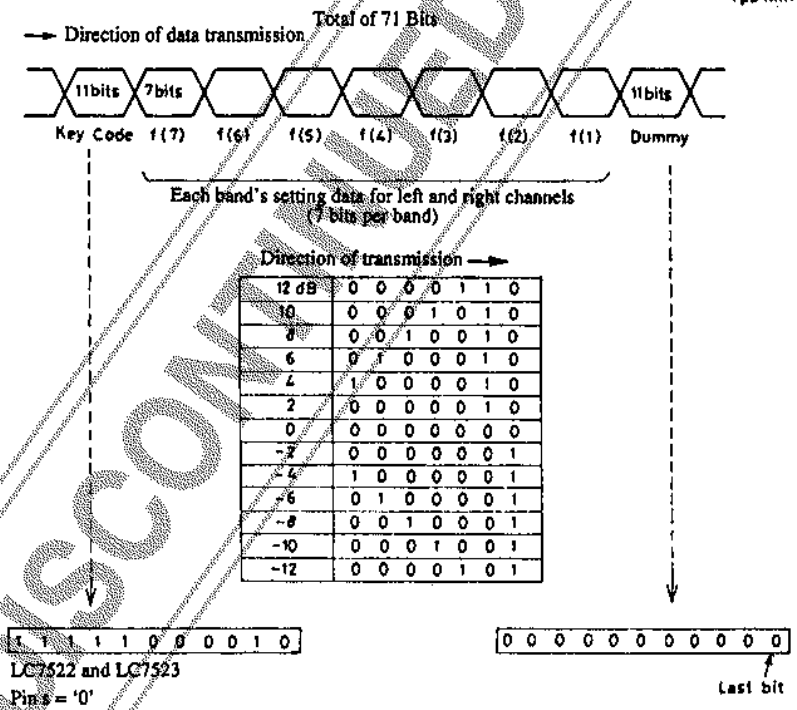


Data Code

(1) Turning on the power initiates a process which transmits no data (0) for 60 clock cycles (initialization clock). When data is stopped in route, the remaining data is sent only after the clock has been initialized.

(2) Using DI and CLK in conjunction with LC7560 (or equivalent) involves the transmission of the maximum initialization clock to those devices involved.

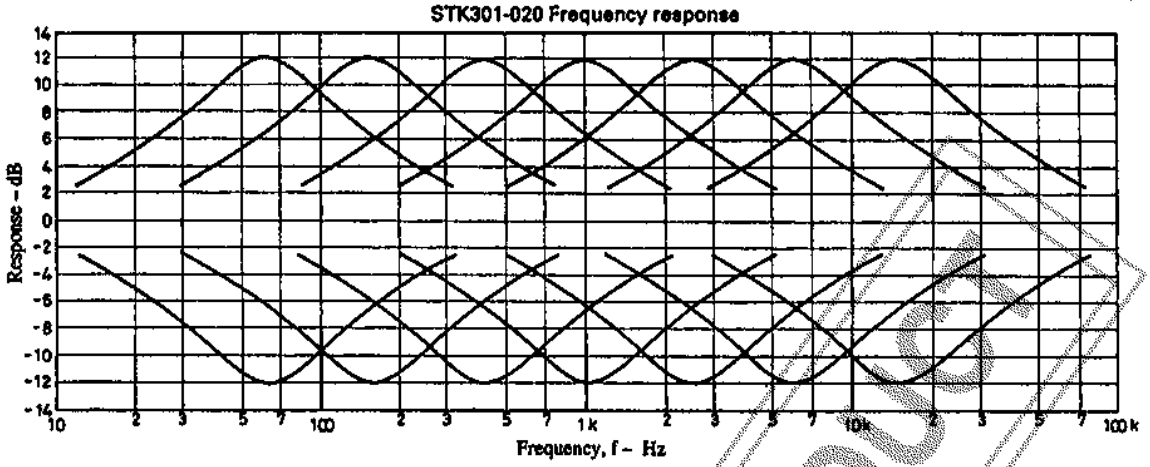




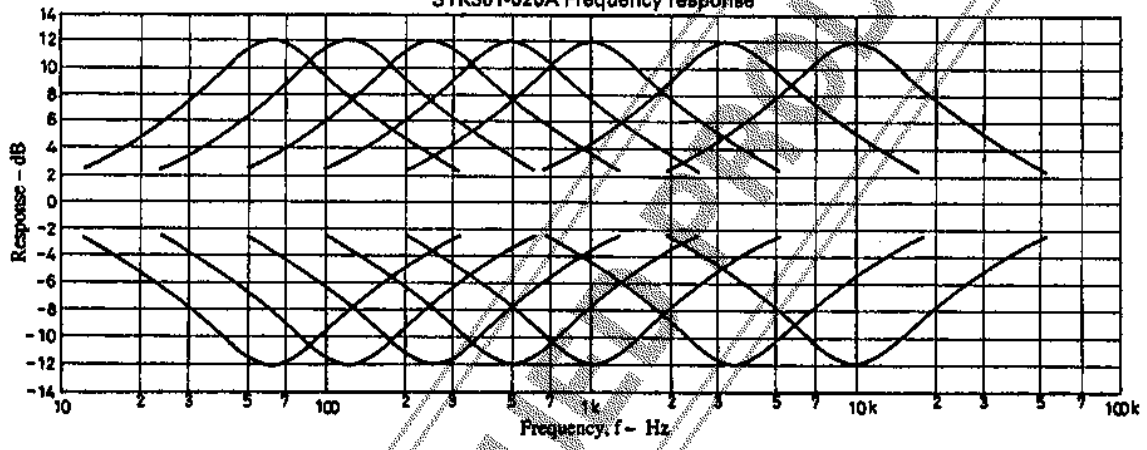
Things to Note

1. A 1000pF rated capacitor (or higher) should be installed between the current pin and V_{SS}.
2. When the control signal on the microcontroller side onsets faster than STK301-020's V_{DD}, a resistor rated at 2kΩ or more should be placed on the DI and CLK line.
3. Since the STK301-020 is equipped with a built-in CMOS LSI, sufficient caution should be extended to damage caused by static electricity.
4. Refer to the specification sheet for itemized details about the LC7522.

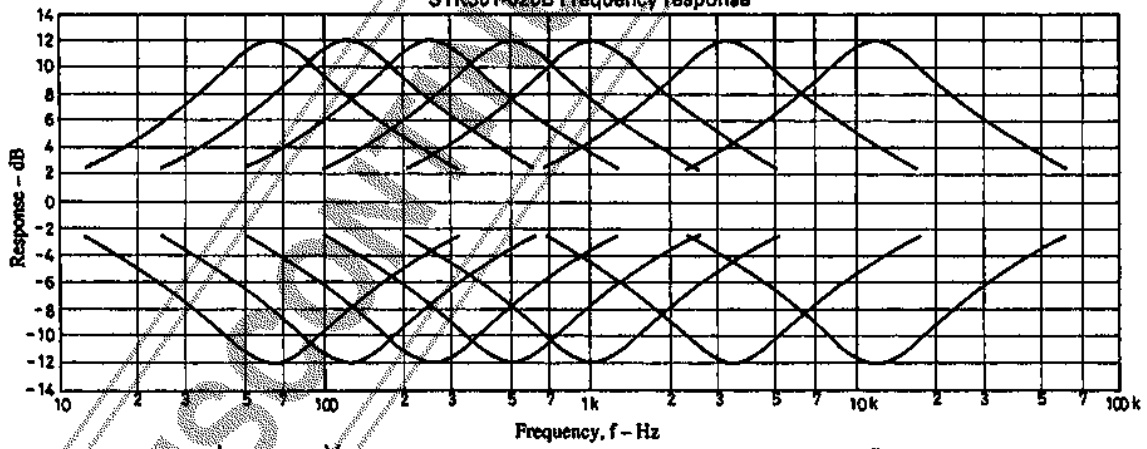
STK301-020 Frequency response



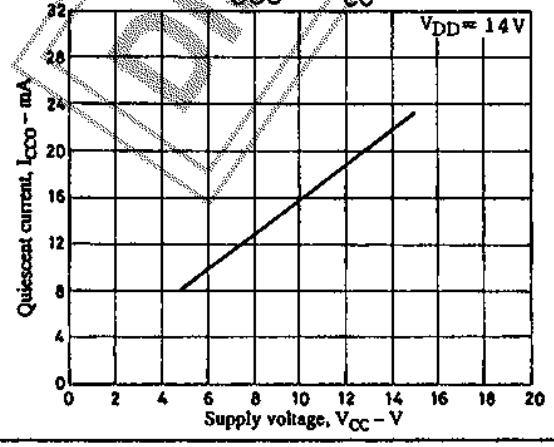
STK301-020A Frequency response



STK301-020B Frequency response



I_{CCO} – V_{CC}



THD – f