19-0302; Rev 0; 9/94

MAXIM

Low-Cost, High-Resolution, 200MHz Video CRT Driver

General Description

The MAX445 is a high-performance, monolithic, variable-gain transconductance amplifier with a high-voltage open-collector output capable of directly driving a video display (CRT cathode). A 2.5ns rise time is achieved using a peaking network with a 200Ω load resistor and an 8pF total load (CRT and parasitic capacitance).

Differential inputs and a linear adjustable gain stage with an output offset adjustment make the versatile MAX445 well suited for many video display applications. A buffered bandgap reference voltage is available for the gain (contrast) and offset adjustments along with a TTL BLANK input to turn off the output current, independent of signal input.

The MAX445 is available in a 24-pin power-tab DIP package. A suitable heatsink must be attached to maintain the junction temperature within the recommended operating range.

Applications

CRT Driver for High-Resolution Monochrome and Color Displays

High-Voltage, Variable-Gain Transconductance Amplifier

Features

- **2.5ns Rise/Fall Time into an 8pF Load**
- **200MHz Small-Signal Bandwidth**
- **50Vp-p Output**
- **Ground Referenced Differential Inputs**
- **Linear Variable Gain for Contrast Control**
- **Offset Adjustment for Black Level**
- **5.5V Bandgap Reference**
- **Drives 1280 x 1024 and 1530 x 1280 Displays**

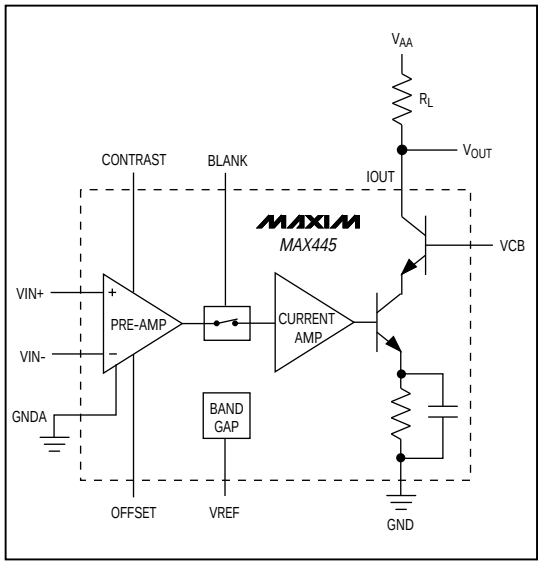
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX445CPG	0°C to +70°C*	24 Power-Tab DIP
MAX445C/D	0°C to +70°C**	Dice

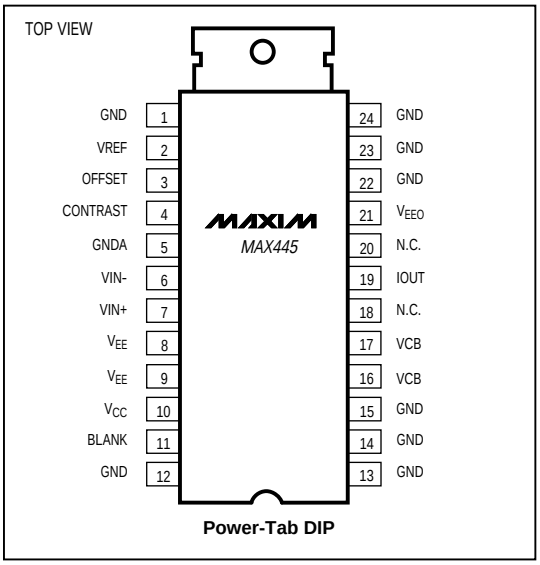
** Case temperature range, T_{CASE} = 0°C to +90°C. See Absolute Maximum Ratings and Applications Information for thermal/heat sink considerations.*

***Dice are specified at T_J = +25°C, DC parameters only.*

Functional Diagram



Pin Configuration



Power-Tab DIP

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ABSOLUTE MAXIMUM RATINGS

V_{AA} Output Supply 80V
V_{AA} Output Supply with Respect to VCB 70V
VCB Common-Base Supply 20V
V_{CC} Positive Supply 12.5V
V_{EE} Negative Supply .....-12.5V
Differential Input Voltage 2V
Common-Mode Input Voltage .....±2V
Contrast Input Voltage .....-1V to +6V
Offset Input Voltage .....-1V to +6V
Blank Input Voltage .....-1V to +6V
Bandgap-Reference Output Current .....-5mA
Continuous Power Dissipation
derate at 170mW/°C above T_{CASE} = +90°C 10W
Operating Junction Temperature .....-55°C to +150°C
Storage Temperature .....-55°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AA} = 20V, VCB = 10V ±0.5V, V_{CC} = 10V ±0.5V, V_{EE} = -10.5V ±0.5V, VIN = (VIN+) - (VIN-) = 0V, CONTRAST = 1.0V, OFFSET = 1.0V, R_L = 0Ω, BLANK = 0.4V, T_{CASE} = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Common-Base Supply Current	I_{CB}				40	mA
Positive Supply Current	I_{CC}				70	mA
Negative Supply Current	I_{EE}	I_{VEE} + I_{VEEO}	-100			mA
Power-Supply Rejection Ratio	PSRR	V_{CC}, V_{EE} = ±5%, VIN = +250mV, CONTRAST = 5.0V, referred to input	25			dB
Low Blank Input Bias Current	I_{IL}	BLANK = 0.4V	-0.6		0	mA
High Blank Input Bias Current	I_{IH}	BLANK = 2.4V	-0.4		0	mA
Contrast Input Bias Current	I_{IC}	CONTRAST = 5.0V	0		10	µA
Offset Input Bias Current	I_{IB}	OFFSET = 1.0V	0		10	µA
VIN+ or VIN- Signal Input Current	I_{IS}		-50		50	µA
Input Common-Mode Rejection Ratio	CMRR	V_{CM} = ±0.5V, CONTRAST = 5.0V	36			dB
VIN+ or VIN- DC Input Impedance	R_{VIN}		10			kΩ
VIN+ or VIN- Input Capacitance	C_{IN}			2		pF
Reference Output Voltage	V_{REF}	I_{LOAD} = 2mA	5.25		5.75	V
Output Current (Blanked)	I_{OUT}	BLANK = 2.4V, OFFSET = 1V, V_{AA} = 75V			±1	mA
		BLANK = 2.4V, OFFSET = 3V			±1	
Output Current	I_{OUT}	OFFSET = 0V, CONTRAST = 4.0V	-0.1		25	mA
		OFFSET = 5.0V, CONTRAST = 1V	80		140	
Output Current Change vs. Temperature	ΔI_{OUT}	T_C = +25°C to +90°C		±3		mA
Output Current Change vs. Contrast ADJ	ΔI_{OUT}	CONTRAST = 0V to 5V			±10	mA
Output Current Change vs. VIN, Blanked	ΔI_{OUT}	BLANK = 2.4V, CONTRAST = 5.0V, ΔVIN- = 0.3V			±1	mA
Transconductance, I_{OUT} to VIN	Gm	CONTRAST = 5.0V	400		600	mA/V
		CONTRAST = 1.0V	70		120	
		CONTRAST = 0V	-25		25	
Amplifier Linearity Error ($\Delta Gm/\Delta V_{IN}$)		CONTRAST = 4.0V, OFFSET = 1.0V			±2	%
Contrast Linearity Error (ΔGm/ΔContrast)		VIN = 0.2V, OFFSET = 0V			±3	%
Bandwidth, 3dB	BW	OFFSET = 0V, R_{LOAD} = 100Ω		200		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{AA} = 20V, VCB = 10V ±0.5V, V_{CC} = 10V ±0.5V, V_{EE} = -10.5V ±0.5V, VIN = (VIN+) - (VIN-) = 0V, CONTRAST = 1.0V, OFFSET = 1.0V, R_L = 0Ω, BLANK = 0.4V, T_{CASE} = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rise/Fall Time (10% to 90%)	t_r, t_f	R_L = 200Ω, C_L = 8pF, V_{AA} = 75V, t_r(VIN) < 1ns,	No peaking, OUTp-p = 50V		3.6		ns
			With peaking, OUTp-p = 45V		2.5		
Settling Time (90% to 100% ±2%)	t_S	C_L = 8pF, no peaking			8		ns
Thermal Distortion					±2		%

Pin Description

PIN	NAME	FUNCTION
1, 12, 13, 14, 15, 22, 23, 24	GND	High-Current Ground. Connect all pins to ground plane.
2	VREF	Reference Output (+5.5V)
3	OFFSET	Output Voltage Offset-Adjustment Input
4	CONTRAST	Output Gain-Adjustment Input
5	GNDA	Pre-Amp Ground
6	VIN-	Inverting Signal Input
7	VIN+	Noninverting Signal Input
8, 9	V_{EE}	Negative Supply (-10.5V)
10	V_{CC}	Positive Supply (+10V)
11	BLANK	Blanking Input, TTL
16, 17	VCB	Output Common-Base Supply (+10V)
18, 20	N.C.	No Connection—leave open
19	IOUT	Open-Collector Current Output
21	V_{EEO}	Negative Supply for Output Stage (-10.5V)

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Applications Information

Differential Inputs

VIN+ and VIN- are differential video input pins designed to allow DC coupling of a 0V to +1V signal into VIN+, with respect to VIN-. For correct operation, it is recommended that the signals applied to these inputs be kept within ±1V, with respect to ground. Although large signals and offsets can be handled safely without damage, exceeding these limits may cause output linearity to suffer.

Contrast Control

The contrast control is the overall DC-gain control that will vary the voltage gain from 0V/V to -90V/V (with a 200Ω load resistor). An internal reference supply pin, VREF, provides the nominal 5.5V needed to drive the contrast input. Normally, a 5kΩ potentiometer between VREF and ground is used to vary the contrast, but an external source can be used instead of VREF, with some degradation of gain stability with temperature.

The contrast control is a linear relationship. Vary the input from 0V to 5V to achieve a voltage-gain range of 0V/V to -90V/V. This yields the following relationship for overall voltage gain of this device (for IOUT < 250mA):

$$V_{AA} - V_O = [V_{IN} (Gm) + V_{OFFSET} (0.02)] (R_L)$$
$$V_{AA} - V_O = [V_{IN} (V_{CONTRAST}) (0.09) + V_{OFFSET} (0.02)] (R_L)$$

The MAX445's overall gain can vary by ±20% due to normal process variations of internal components. Also, if multiple devices are used in a system, all devices must track thermally (i.e., a common heatsink).

Offset Control

The offset control is used to set the output quiescent current from 5mA to 110mA (typ) when the control input is adjusted from 0V to 5V. Normally, offset is adjusted using a 5kΩ potentiometer between VREF and ground.

Blank Control

When asserted (BLANK = TTL high), this input will disable the video signal and allow the output to rise to the V_{AA} supply independent of offset control.

Bandgap Reference

VREF is a bandgap bias reference for easy adjustment of the offset and contrast inputs. This reference has a nominal output voltage of 5.5V ±5% that can source up to 4mA.

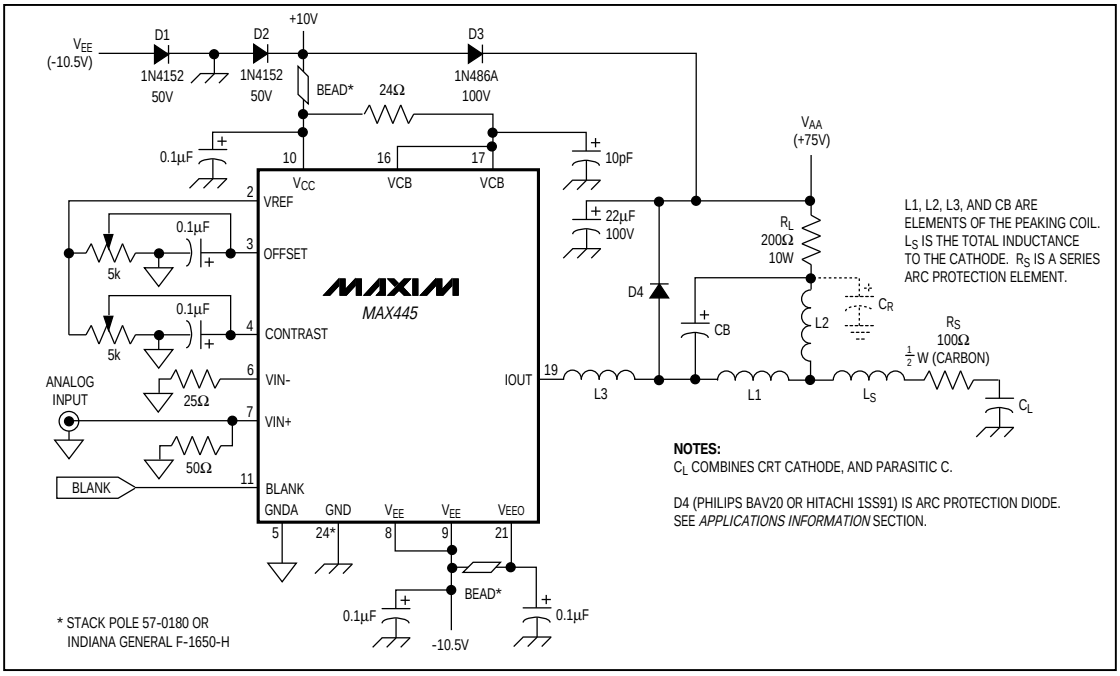

Figure 1. Typical Connection Diagram

IOUT

The MAX445's output is an open collector of a cascode amplifier. This output is designed to work with nominal output supplies of V_{AA} = +75V. The high-voltage supply must be greater than any applied VCB voltage for proper operation. The MAX445 sinks up to 250mA. Optimum performance into a capacitive load can be achieved when an impedance-matching network is used.

VCB

The output stage consists of a common-base, high-voltage stage and a high-speed, low-voltage current amplifier in a cascode arrangement. The VCB input is the base connection to the common-base device of this stage. Be sure to provide a stable DC voltage at this pin of nominally +10V. High-frequency compensation at this input is required to avoid output oscillations. Use a series 24Ω resistor to supply, shunted with a 10pF capacitor to ground (Figure 1). Smaller values of this RC combination will improve output rise/fall times, but can cause output oscillations.

Power Supplies

+10V and -10.5V supplies are required for proper operation. These supplies can be set to ±12V for convenience, however this will add additional component power dissipation. The high-voltage supply, V_{AA}, can be any voltage between VCB + 10V and VCB + 65V.

V_{EEO} (pin 21) is the negative supply to the output stage and must be DC connected to V_{EE} (pins 8 and 9), the most negative voltage applied to the device. However, V_{EEO} must be decoupled from V_{EE} to prevent output oscillations. A ferrite bead and separate 0.1µF decoupling capacitors, as shown in Figure 1, will provide appropriate decoupling.

Power-Supply Sequencing

Power-supply sequencing is important to avoid internal device latchup. To avoid sequencing problems, external diodes should be placed from V_{EE} to ground, from ground to V_{CC}, and from V_{CC} to the output supply (V_{AA}), as shown in Figure 1. With diodes used as shown, special power-supply sequencing is not required.

CRT Arc Protection

The MAX445 must be protected from electrostatic discharge ("arcs") from the CRT. It is recommended that the output be clamped with a low-capacitance (less than 2pF) diode to the V_{AA} supply. The peak current-handling capability required of the diode is a function of the CRT arc characteristics, but typically should be 1A or more, such as Philips BAV20 or Hitachi 1SS91. For additional information regarding arc protection, contact Maxim's applications department.

Impedance Matching Network

For maximum speed from the MAX445, be sure to "match" the output to the CRT. Figure 1's typical connection diagram shows a network (including parasitic reactances) associated with arc protection devices, CRT wiring and grid structure, and load resistors. These parasitic reactances are all detrimental to good transient response and should be minimized as much as possible.

C_L is the grid-to-cathode capacitance of the CRT, plus any parasitic capacitance to ground associated with the cathode structure. This capacitance varies from tube-type to tube-type over the 4pF to 12pF range.

In Figure 1, L_S is the inductance of the lead from the amplifier board to the CRT cathode and the return path from the grid to circuit ground. A wire in free space has an inductance of 20nH/inch to 25nH/inch. With care, the total path through the CRT gun can be kept at 1.5 to 2 inches, such that L_S ranges from 30nH to 50nH. Excessive lead length will cause undesirable overshoot and ringing in the transient response.

The peaking networks assume that 2pF of parasitic capacitance is associated with the CRT arc protection diode connected at the junction of L3 and L1.

Lr is the parasitic inductance of the load resistor, R_L. In some cases, C_R may be needed to improve step response.

R_S is a damping resistor in series with the CRT grid. It also provides current limiting in the event of CRT arcing.

The equations for determining optimum peaking network values are as follows:

$$L1 = (R_L)^2 (C_L) / 4$$

$$L2 = 3(R_L)^2 (C_L) / 4$$

$$C_B = C_L / 5$$

$$R_S = R_L / 2$$

$$L3 = k_3 (R_L)^2 [2.5 \times 10^{-12}]$$

$$C_R \text{ (optional)} = Lr / (2R_L^2)$$

k_3 is an empirically determined factor increasing with C_L and varying from 0 for C_L ~ 2pF to 1 for C_L ~ 12pF. However, L3 >100nH will compromise large-signal performance.

Table 1 shows peaking networks for the nominal load, R_L = 200Ω (and R_S = 100Ω).

Optimum peaking depends on board layout and CRT construction. The values given by these equations should be used as starting points for empirically determining optimum values.

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Table 1. Peaking Networks (R_L = 200Ω, R_S = 100Ω)

C_L (pF)	L3 (nH)	L1 (nH)	L2 (nH)	C_B (pF)	t_R (ns)
2	0	20	60	0.4	1.7
4	0	40	120	0.8	1.9
6	20	60	180	1.1	2.1
8	50	80	240	1.5	2.3
10	75	100	300	2.0	2.7
12	100	120	360	2.2	3.0

Inductors L1, L2, and L3 should be air or ferrite-core coils with self-resonant frequencies higher than 500MHz.

Thermal Environment

The MAX445 can dissipate a large amount of power depending on speed and load-driving requirements. The power-tab package provides a low thermal resistance path from the chip to an external heatsink. Be sure the board design provides sufficient heatsinking capacity for the intended operating range. When mounting to a chassis, it should be noted that the device tab is attached to V_{EE} (-10.5V). This tab should be electrically isolated from ground through a thermally conductive insulator.

It is highly recommended that the external heatsink be connected to ground, since an arc or electrostatic discharge entering the heatsink may break down or bypass the tab insulator and damage the device. Also, the grounded heatsink to package tab capacitance will help to bypass the V_{EE} supply. Another option would be to bypass the heatsink to ground with a 0.01µF capacitor with no tab insulator. Inadvertently shorting the package tab to ground for less than 10 seconds will not cause component damage. Junction-to-case thermal resistance is rated at 6°C/W for the power-tab DIP package. Table 2 shows the relationship of output voltage and duty cycle to total power.

Table 2. Power Dissipation at V_{AA} = 70V and Load Resistor = 200Ω

Output Level Relative to Black (V)	Duty Cycle (%)	IC Power (W)	Load Power (W)	Total (W)
0	0	1.6	0	1.6
35	100	7.8	6.1	13.9
35	80	6.5	4.9	11.4
50	80	5.6	10.0	15.6

Circuit Layout and Bypassing

Due to the extremely high-speed performance of the MAX445, layout design precautions are required to realize the display driver's full high-speed capability. The precautions are as follows:

1) A printed circuit board with a good, unbroken, low-inductance ground plane is required.
2) Place a decoupling capacitor (0.01µF ceramic) as close to V_{CC} as possible.
3) Pay close attention to the decoupling capacitors' resonant frequency and keep leads short.
4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the display driver.
5) Solder the MAX445 directly to the printed circuit board. Do not use sockets.

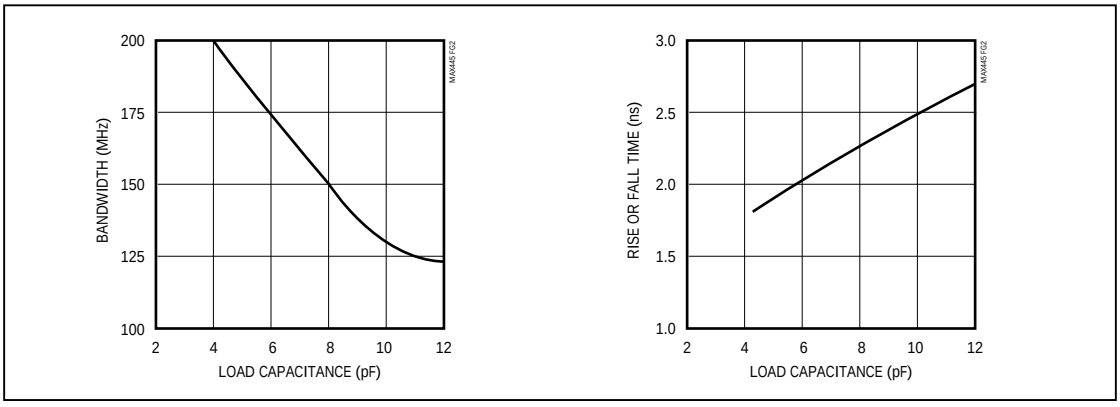

Figure 2. Typical Rise/Fall Time vs. Loading, with Peaking Network Optimized for Load Capacitance

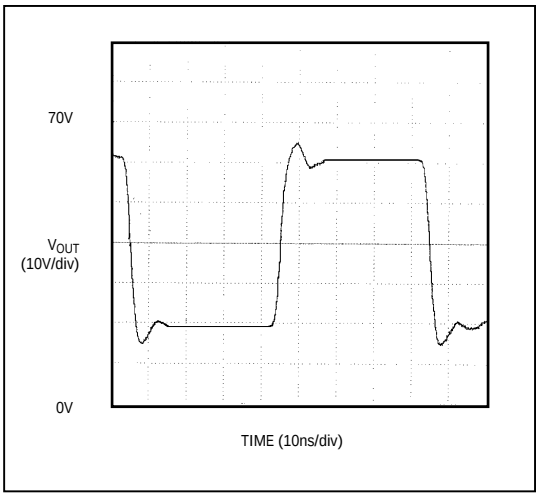

Figure 3. Step Response Showing Typical Rise/Fall Times from MAX445 EV Kit Using a Tektronix 11401 Oscilloscope

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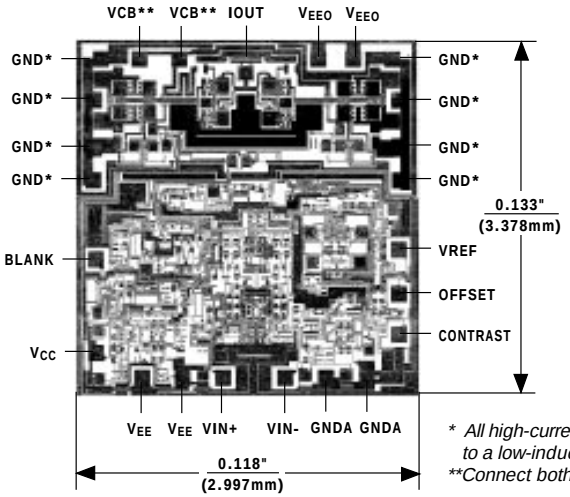
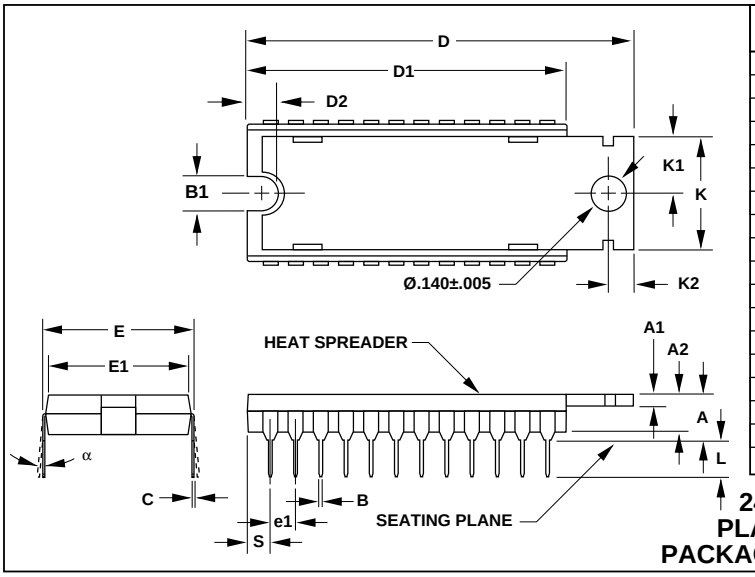
Chip Topography



* *All high-current ground pads must be bonded and connected to a low-inductance ground plane.*
***Connect both VCB pads.*

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.200	4.318	5.080
A1	0.048	0.052	1.219	1.321
A2	0.145	0.155	3.683	3.937
B	0.016	0.020	0.406	0.508
B1	0.145	0.155	3.683	3.937
C	0.009	0.011	0.229	0.279
D	1.590	1.610	40.386	40.894
D1	1.330	1.345	33.782	33.163
D2	0.135	0.145	3.429	3.683
E	0.600 BSC		15.240 BSC	
E1	0.545	0.555	13.843	14.097
e1	0.100 BSC		2.540 BSC	
L	0.120	0.130	3.048	3.302
S	0.110	0.120	2.794	3.048
K	0.398	0.402	10.109	10.211
K1	0.195	0.205	4.953	5.207
K2	0.098	0.102	2.489	2.591
α	0°	15°	0°	15°

21-7000A

24-PIN POWER-TAB PLASTIC DUAL-IN-LINE PACKAGE WITHOUT HEAT SINK