

LM032L·LM032XMBL

- 20 character x 2 lines
- Controller LSI HD44780 is built-in (See page 79).
- +5V single power supply
- Display color: LM032L : Gray
LM032XMBL : New-gray

MECHANICAL DATA (Nominal dimensions)

Module size116W x 39H (max.) x 10.5T (max.) mm
 Effective display area 83W x 18.6H mm
 Character size (5 x 7 dots) 3.2W x 4.85H mm
 Character pitch 3.7 mm
 Dot size 0.6W x 0.65H mm
 Weight about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (V_i)	V_{SS}	V_{DD} V
Operating temperature (T_a)	0	50 40*°C
Storage temperature (T_{stg})	-20	70 60*°C

* Shows the value of type LM032XMBL.

ELECTRICAL CHARACTERISTICS

$T_a = 25^\circ\text{C}$, $V_{DD} = 5.0 \text{ V} \pm 0.25 \text{ V}$
 Input "high" voltage (V_{IH}) 2.2 V min.
 Input "low" voltage (V_{IL}) 0.6 V max.
 Output "high" voltage (V_{OH}) ($-I_{OH} = 0.2 \text{ mA}$) . . 2.4V min.
 Output "low" voltage (V_{OL}) ($I_{OL} = 1.2 \text{ mA}$) . . 0.4V max.
 Power supply current (I_{DD}) ($V_{DD} = 5.0 \text{ V}$) . . 2.0 mA typ.
 3.0 mA max.

POWER SUPPLY FOR LCD DRIVE (Recommended) ($V_{DD}-V_O$)

Duty = 1/16
 Range of $V_{DD}-V_O$ 1.5~5.25 V
 $T_a = 0^\circ\text{C}$ 4.6 V typ.
 $T_a = 25^\circ\text{C}$ 4.2 V typ.
 $T_a = 50^\circ\text{C}$ 3.5 V typ.

OPTICAL DATA See page 7

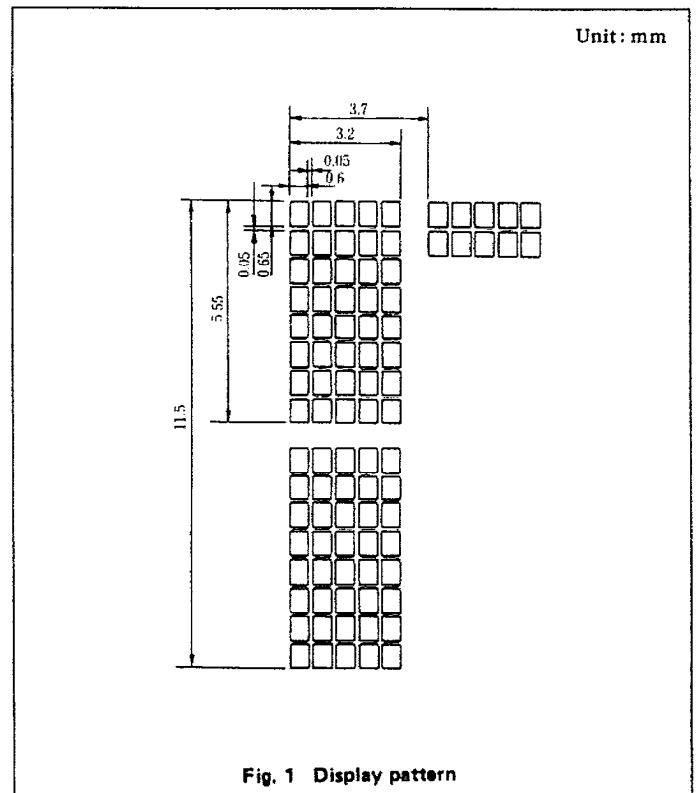
INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	—	0V
2	V_{DD}	—	+5V
3	V_O	—	—
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

- (1) When interface data is 4 bits long, data is transferred using only 4 buses of $DB_4 \sim DB_7$, and $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$, when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of $DB_0 \sim DB_3$, when interface data is 8 bits long).
- (2) When interface data is 8 bits long, data is transferred using 8 data buses of $DB_0 \sim DB_7$.



Unit: mm

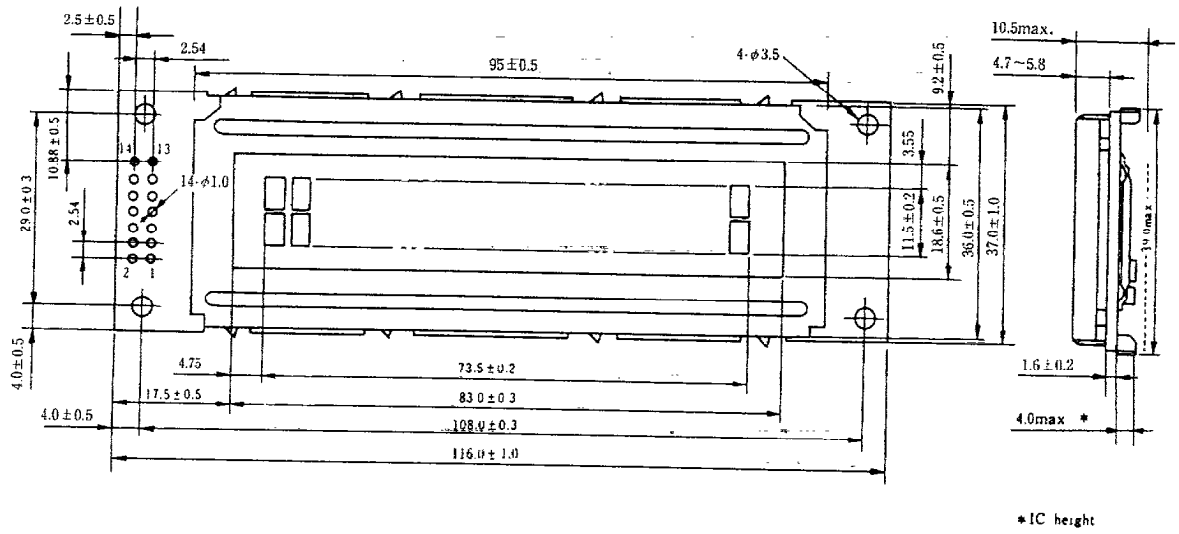


Fig. 2 External dimensions

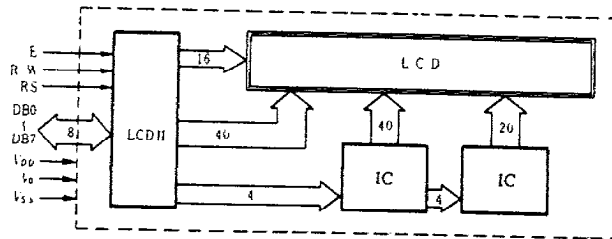


Fig. 3 Block diagram

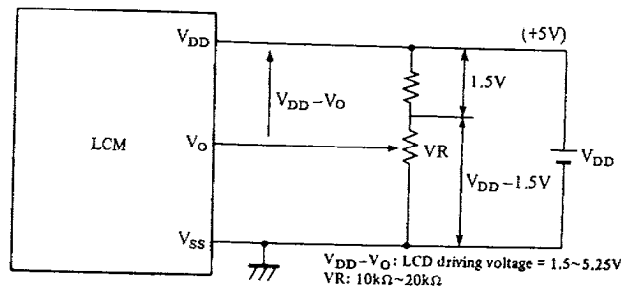


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	—	—	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	—	—	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	—	—	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	—	—	ns
Data delay time	t_{DDR}	Fig. 6	—	—	320	ns
Data set up time	t_{DSW}	Fig. 5	195	—	—	ns
Hold time	t_H	Fig. 5, Fig. 6	20	—	—	ns

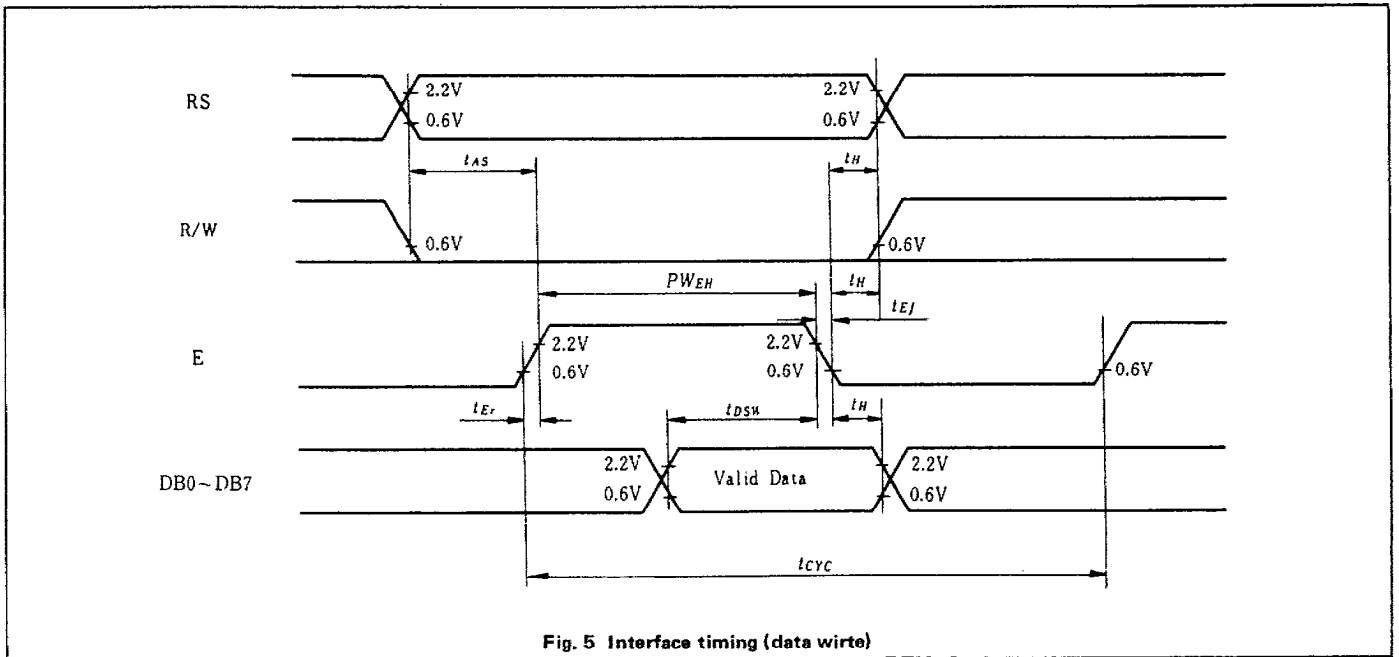


Fig. 5 Interface timing (data write)

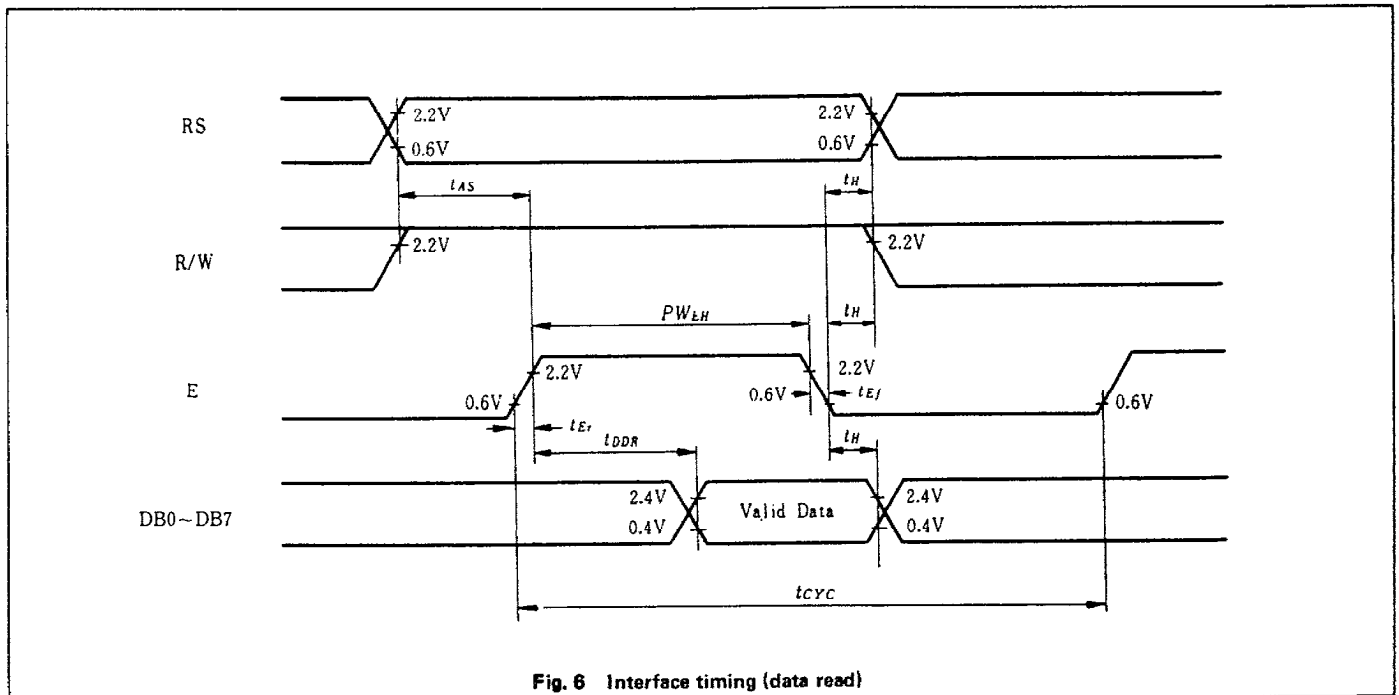


Fig. 6 Interface timing (data read)