19-1284; Rev 0; 10/97

MAXIM

Low-Cost, High-Speed, Single-Supply, Gain of +2 Buffers with Rail-to-Rail Outputs in SOT23

MAX4014/MAX4017/MAX4019/MAX4022

General Description

The MAX4014/MAX4017/MAX4019/MAX4022 are precision, closed-loop, gain of +2 (or -1) buffers featuring high slew rates, high output current drive, and low differential gain and phase errors. These single-supply devices operate from +3.15V to +11V, or from ±1.575V to ±5.5V dual supplies. The input voltage range extends 100mV beyond the negative supply rail and the outputs swing Rail-to-Rail®.

These devices require only 5.5mA of quiescent supply current while achieving a 200MHz -3dB bandwidth and a 600V/µs slew rate. In addition, the MAX4019 has a disable feature that reduces the supply current to 400µA. Input voltage noise for these parts is only 10nV/√Hz and input current noise is only 1.3pA/√Hz. This buffer family is ideal for low-power/low-voltage applications that require wide bandwidth, such as video, communications, and instrumentation systems. For space-sensitive applications, the MAX4014 comes in a tiny 5-pin SOT23 package.

Features

- **Internal Precision Resistors for Closed-Loop Gains of +2 or -1**
- **High Speed:**
  - **200MHz -3dB Bandwidth**
  - **30MHz 0.1dB Gain Flatness (6MHz min)**
  - **600V/µs Slew Rate**
- **Single 3.3V/5.0V Operation**
- **Outputs Swing Rail-to-Rail**
- **Input Voltage Range Extends Beyond V_{EE}**
- **Low Differential Gain/Phase: 0.04%/0.02°**
- **Low Distortion at 5MHz:**
  - **-78dBc Spurious-Free Dynamic Range**
  - **-75dB Total Harmonic Distortion**
- **High Output Drive: ±120mA**
- **Low, 5.5mA Supply Current**
- **400µA Shutdown Supply Current**
- **Space-Saving SOT23-5, µMAX, or QSOP Packages**

Selector Guide

PART	NO. OF AMPS	ENABLE	PIN-PACKAGE
MAX4014	1	No	5-Pin SOT23
MAX4017	2	No	8-Pin SO/µMAX
MAX4019	3	Yes	14-Pin SO, 16-Pin QSOP
MAX4022	4	No	14-Pin SO, 16-Pin QSOP

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4014EUK	-40°C to +85°C	5 SOT23-5	ABZQ
MAX4017ESA	-40°C to +85°C	8 SO	—
MAX4017EUA	-40°C to +85°C	8 µMAX	—
MAX4019ESD	-40°C to +85°C	14 SO	—
MAX4019EEE	-40°C to +85°C	16 QSOP	—
MAX4022ESD	-40°C to +85°C	14 SO	—
MAX4022EEE	-40°C to +85°C	16 QSOP	—

Applications

Portable/Battery-Powered Instruments

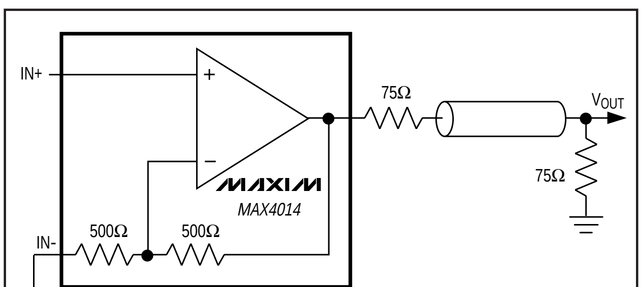
Video Line Driver

Analog-to-Digital Converter Interface

CCD Imaging Systems

Video Routing and Switching Systems

Typical Operating Circuit



GAIN OF +2 VIDEO/RF CABLE DRIVER

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})..12V
IN_-, IN_+, OUT_, EN_ ....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration to V_{CC} or V_{EE}.............Continuous
Continuous Power Dissipation (T_A = +70°C)
5-pin SOT23 (derate 7.1mW/°C above+70°C).............571mW
8-pin SO (derate 5.9mW/°C above +70°C)..................471mW
8-pin µMAX (derate 4.1mW/°C above +70°C).............330mW
14-pin SO (derate 8.3mW/°C above +70°C)................667mW
16-pin QSOP (derate 8.3mW/°C above +70°C)...........667mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or at any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, IN_- =0V, EN_ = 5V, R_L = ∞ to ground, V_{OUT} = V_{CC} / 2, noninverting configuration, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	IN_+		V_{EE} - 0.1		V_{CC} - 2.25	V
		IN_-		V_{EE} - 0.1		V_{CC} + 0.1	
Input Offset Voltage	V_{OS}	R_L = 50Ω			4	20	mV
Input Offset Voltage Drift	TC_{VOS}				8		µV/°C
Input Offset Voltage Matching		Any channels for MAX4017/MAX4019/MAX4022			±1		mV
Input Bias Current	I_B	IN_+ (Note 2)			5.4	20	µA
Input Resistance	R_{IN}	IN_+, over input voltage range			3		MΩ
Voltage Gain	A_V	R_L ≥ 50Ω, (V_{EE} + 0.5V) ≤ V_{OUT} ≤ (V_{CC} - 2.0V)		1.9	2	2.1	V/V
Output Resistance	R_{OUT}	f = DC			25		mΩ
Output Current	I_{OUT}	R_L = 20Ω to V_{CC} or V_{EE}		±80	±120		mA
Short-Circuit Output Current	I_{SC}	Sinking or sourcing			±150		mA
Output Voltage Swing	V_{OUT}	R_L = 50Ω	V_{CC} - V_{OH}		1.60	2.00	V
			V_{OL} - V_{EE}		0.04	0.50	
		R_L =150Ω	V_{CC} - V_{OH}		0.75	1.50	
			V_{OL} - V_{EE}		0.04	0.50	
		R_L = 2kΩ	V_{CC} - V_{OH}		0.06		
			V_{OL} - V_{EE}		0.06		
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{CC} = 5V, V_{EE} = 0V, V_{OUT} = 2V		46	57		dB
		V_{CC} = 5V, V_{EE} = -5V, V_{OUT} = 0V		54	66		
		V_{CC} = 3.3V, V_{EE} = 0V, V_{OUT} = 0.9V			45		
Operating Supply-Voltage Range		V_{CC} to V_{EE}		3.15		11.0	V
Disabled Output Resistance	$R_{OUT(OFF)}$	MAX4019, EN_ = 0V, 0V ≤ V_{OUT} ≤ 5V			1		kΩ
EN_ Logic-Low Threshold	V_{IL}	MAX4019				V_{CC} - 2.6	V
EN_ Logic-High Threshold	V_{IH}	MAX4019		V_{CC} - 1.5			V
EN_ Logic Input Low Current	I_{IL}	MAX4019	(V_{EE} + 0.2V) ≤ EN_ ≤ V_{CC}		0.5		µA
			EN_ = V_{EE}		200	550	
EN_ Logic Input High Current	I_{IH}	MAX4019, EN_ = V_{CC}			0.5	10	µA
Quiescent Supply Current (per Buffer)	I_{CC}	Enabled (EN_ = V_{CC})			5.5	8.0	mA
		MAX4019, disabled (EN_ = V_{EE})			0.4	0.7	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, IN_- = 0V, EN_ = 5V, R_L = 100Ω to ground, noninverting configuration, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 20mVp-p		200		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p		140		MHz
Bandwidth for 0.1dB Gain Flatness	$BW_{0.1dB}$	V_{OUT} = 20mVp-p (Note 4)	6	30		MHz
Slew Rate	SR	V_{OUT} = 2V step		600		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step		45		ns
Rise/Fall Time	t_R, t_F	V_{OUT} = 100mVp-p		1		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p		-78		dBc
Harmonic Distortion	HD	V_{OUT} = 2Vp-p, f_C = 5MHz: Second harmonic		-78		dBc
		Third harmonic		-82		
		Total harmonic distortion		-75		
Third-Order Intercept	IP3	f = 10.0MHz		35		dBm
Input 1dB Compression Point		f_C = 10MHz, A_{VCL} = +2V/V		11		dBm
Differential Phase Error	DP	NTSC, R_L = 150Ω		0.02		degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω		0.04		%
Input Noise Voltage Density	e_n	f = 10kHz		10		$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f = 10kHz		1.3		$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}			1		pF
Disabled Output Capacitance	$C_{OUT(OFF)}$	MAX4019, EN_ = 0V		2		pF
Output Impedance	Z_{OUT}	f = 10MHz		6		Ω
Buffer Enable Time	t_{ON}	MAX4019		100		ns
Buffer Disable Time	t_{OFF}	MAX4019		1		µs
Buffer Gain Matching		MAX4017/MAX4019/MAX4022, f = 10MHz, V_{OUT} = 20mVp-p		0.1		dB
Buffer Crosstalk	X_{TALK}	MAX4017/MAX4019/MAX4022, f = 10MHz, V_{OUT} = 2Vp-p		-95		dB

Note 1: The MAX4014EUK is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 2: Tested with V_{OUT} = +2.5V.

Note 3: PSRR for single +5V supply tested with V_{EE} = 0V, V_{CC} = +4.5V to +5.5V; for dual ±5V supply with V_{EE} = -4.5V to -5.5V, V_{CC} = +4.5V to +5.5V; and for single +3V supply with V_{EE} = 0V, V_{CC} = +3.15V to +3.45V.

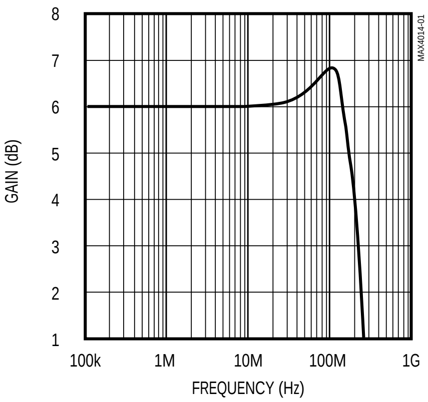
Note 4: Guaranteed by design.

Low-Cost, High-Speed, Single-Supply, Gain of +2 Buffers with Rail-to-Rail Outputs in SOT23

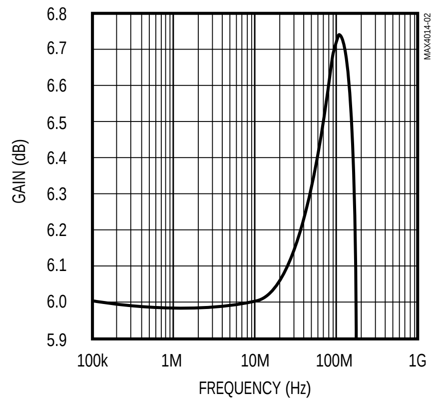
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +2, R_L = 150Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

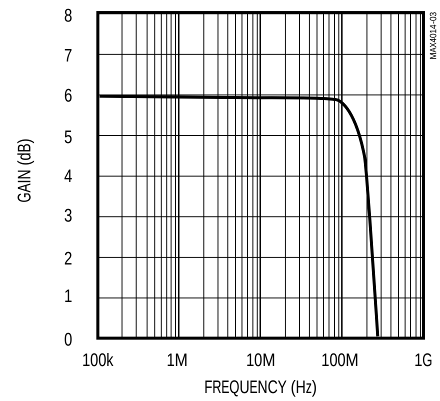
SMALL-SIGNAL GAIN vs. FREQUENCY



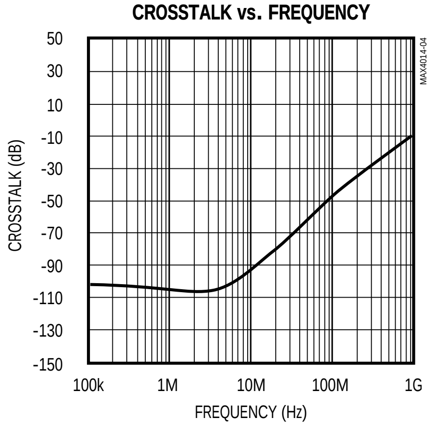
GAIN FLATNESS vs. FREQUENCY



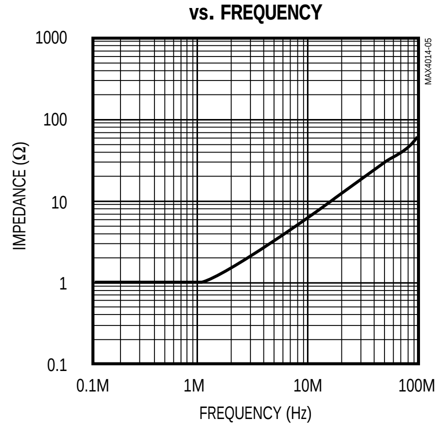
LARGE-SIGNAL GAIN vs. FREQUENCY



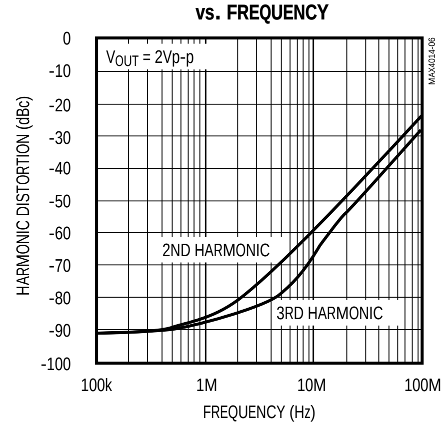
MAX4017/19/22 CROSSTALK vs. FREQUENCY



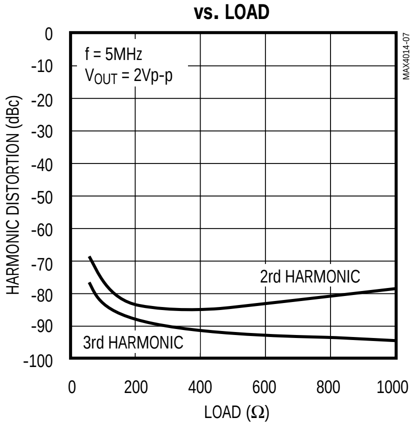
CLOSED-LOOP OUTPUT IMPEDANCE vs. FREQUENCY



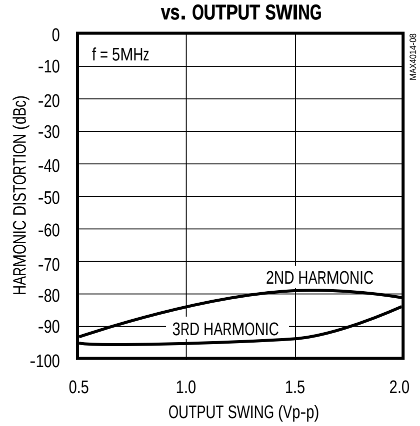
HARMONIC DISTORTION vs. FREQUENCY



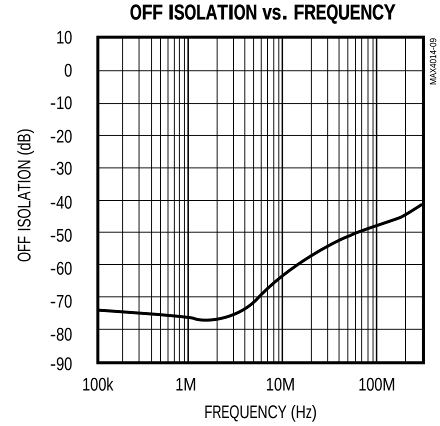
HARMONIC DISTORTION vs. LOAD



HARMONIC DISTORTION vs. OUTPUT SWING



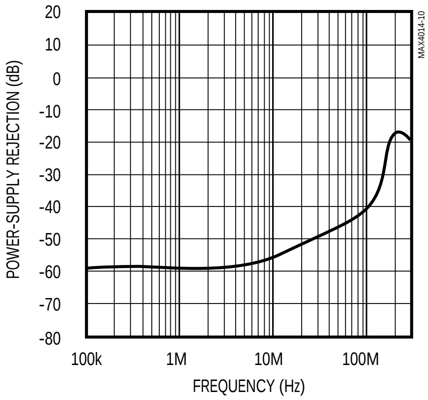
MAX4019 OFF ISOLATION vs. FREQUENCY



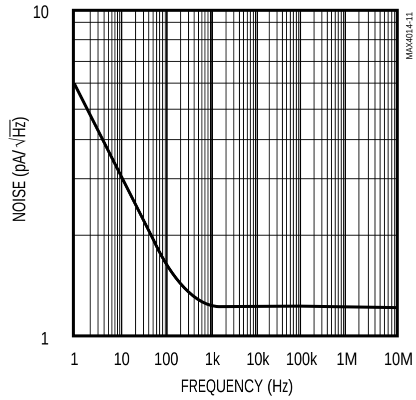
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +2, R_L = 150Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

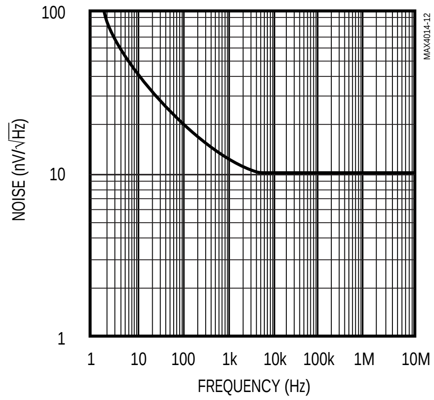
POWER-SUPPLY REJECTION vs. FREQUENCY



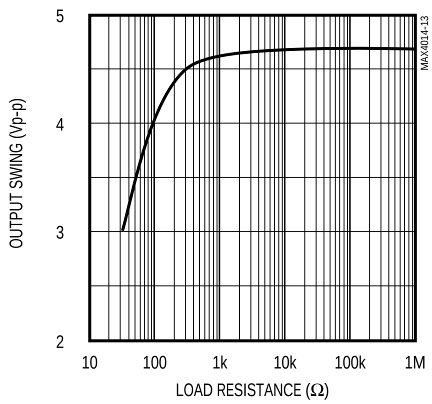
CURRENT NOISE DENSITY vs. FREQUENCY



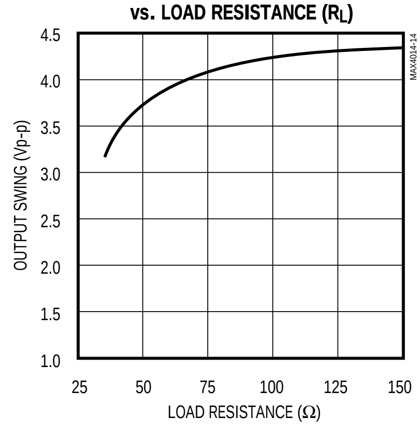
VOLTAGE NOISE DENSITY vs. FREQUENCY



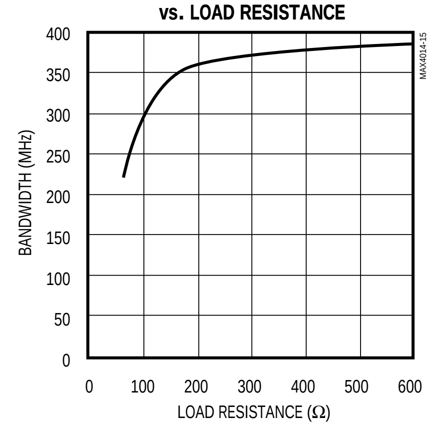
OUTPUT SWING vs. LOAD RESISTANCE



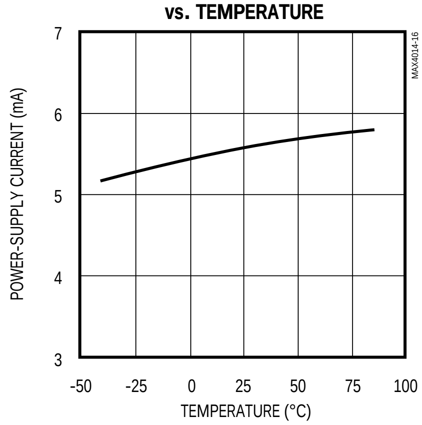
OUTPUT SWING vs. LOAD RESISTANCE (R_L)



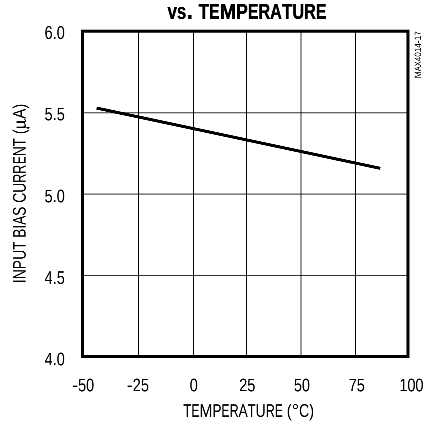
BANDWIDTH vs. LOAD RESISTANCE



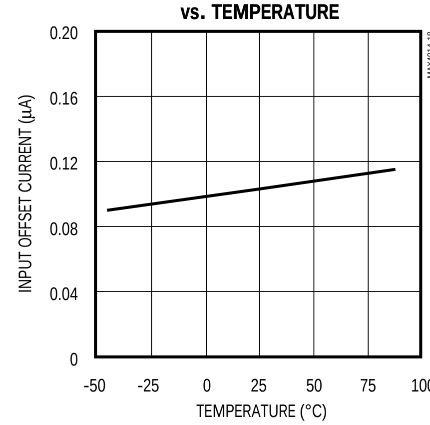
POWER-SUPPLY CURRENT (PER AMPLIFIER) vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



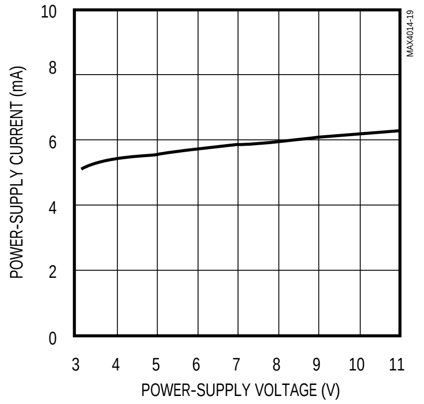
INPUT OFFSET CURRENT vs. TEMPERATURE



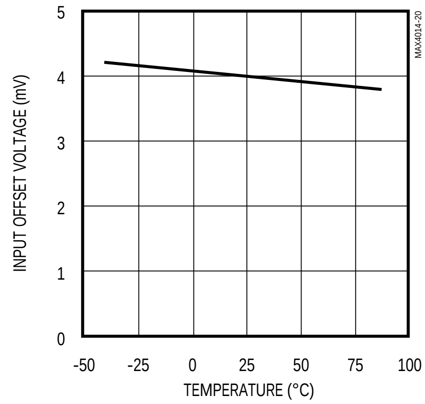
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +2, R_L = 150Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

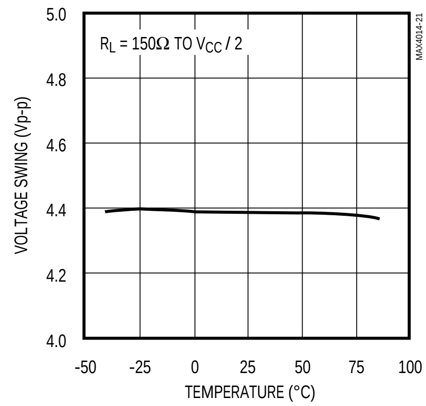
POWER-SUPPLY CURRENT (PER AMPLIFIER) vs. POWER-SUPPLY VOLTAGE



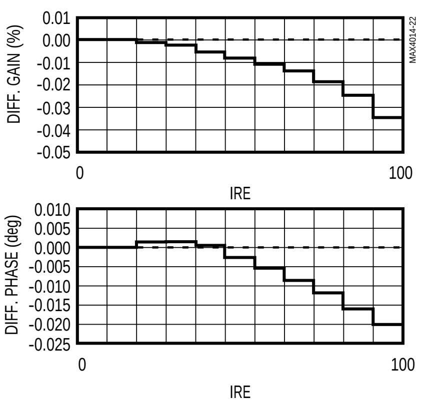
INPUT OFFSET VOLTAGE vs. TEMPERATURE



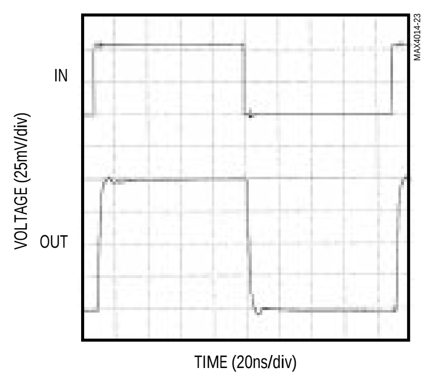
VOLTAGE SWING vs. TEMPERATURE



DIFFERENTIAL GAIN AND PHASE

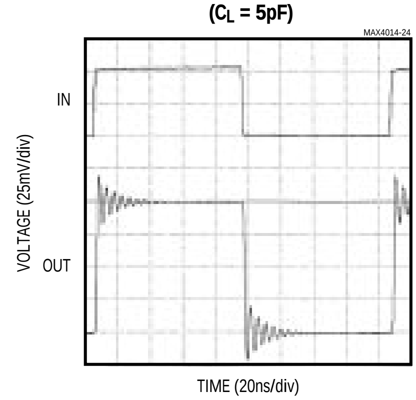


SMALL-SIGNAL PULSE RESPONSE

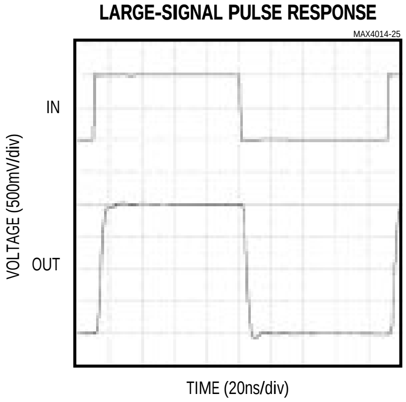


V_{CM} = 1.25V, R_L = 100Ω to GROUND

SMALL-SIGNAL PULSE RESPONSE (C_L = 5pF)

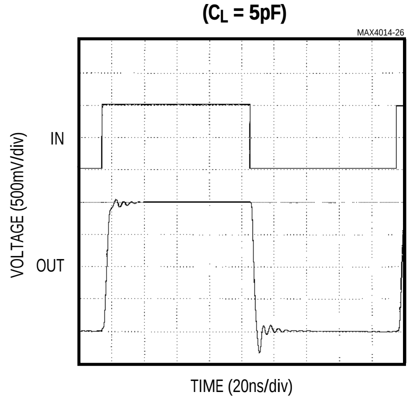


LARGE-SIGNAL PULSE RESPONSE



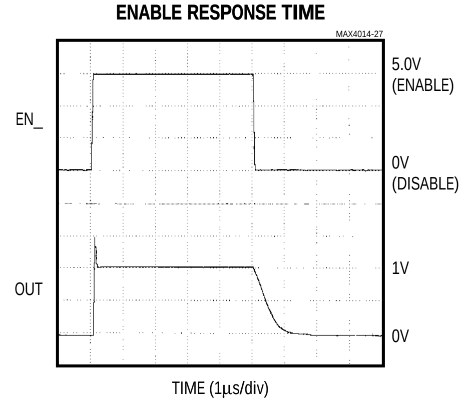
V_{CM} = 0.9V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE (C_L = 5pF)



V_{CM} = 1.75V, R_L = 100Ω to GROUND

ENABLE RESPONSE TIME



V_{IN} = 0.5V

Pin Description

PIN						NAME	FUNCTION
MAX4014	MAX4017	MAX4019		MAX4022			
SOT23-5	SO/µMAX	SO	QSOP	SO	QSOP		
—	—	—	8, 9	—	8, 9	N.C.	No Connect. Not internally connected. Tie to ground or leave open.
1	—	—	—	—	—	OUT	Amplifier Output
2	4	11	13	11	13	V_{EE}	Negative Power Supply or Ground (in single-supply operation)
3	—	—	—	—	—	IN+	Noninverting Input
4	—	—	—	—	—	IN-	Inverting Input
5	8	4	4	4	4	V_{CC}	Positive Power Supply
—	1	7	7	1	1	OUTA	Amplifier A Output
—	2	6	6	2	2	INA-	Amplifier A Inverting Input
—	3	5	5	3	3	INA+	Amplifier A Noninverting Input
—	7	8	10	7	7	OUTB	Amplifier B Output
—	6	9	11	6	6	INB-	Amplifier B Inverting Input
—	5	10	12	5	5	INB+	Amplifier B Noninverting Input
—	—	14	16	8	10	OUTC	Amplifier C Output
—	—	13	15	9	11	INC-	Amplifier C Inverting Input
—	—	12	14	10	12	INC+	Amplifier C Noninverting Input
—	—	—	—	14	16	OUTD	Amplifier D Output
—	—	—	—	13	15	IND-	Amplifier D Inverting Input
—	—	—	—	12	14	IND+	Amplifier D Noninverting Input
—	—	1	1	—	—	ENA	Enable Input for Amplifier A
—	—	3	3	—	—	ENB	Enable Input for Amplifier B
—	—	2	2	—	—	ENC	Enable Input for Amplifier C

Detailed Description

The MAX4014/MAX4017/MAX4019/MAX4022 are single-supply, rail-to-rail output, voltage-feedback, closed-loop buffers that employ current-feedback techniques to achieve 600V/µs slew rates and 200MHz bandwidths. These buffers use internal 500Ω resistors to provide a preset closed-loop gain of +2V/V in the noninverting configuration or -1V/V in the inverting configuration. Excellent harmonic distortion and differential gain/phase performance make these buffers an ideal choice for a wide variety of video and RF signal-processing applications.

Local feedback around the buffer's output stage ensures low output impedance, which reduces gain sensitivity to load variations. This feedback also produces demand-driven current bias to the output transistors for ±120mA drive capability, while constraining total supply current to less than 7mA.

Applications Information

Power Supplies

These devices operate from a single +3.15V to +11V power supply or from dual supplies of ±1.575V to ±5.5V. For single-supply operation, bypass the V_{CC} pin to ground with a 0.1µF capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1µF capacitor.

Selecting Gain Configuration

Each buffer in the MAX4014 family can be configured for a voltage gain of +2V/V or -1V/V. For a gain of +2V/V, ground the inverting terminal. Use the noninverting terminal as the signal input of the buffer (Figure 1a). Grounding the noninverting terminal and using the inverting terminal as the signal input configures the buffer for a gain of -1V/V (Figure 1b).

Since the inverting input exhibits a 500Ω input impedance, terminate the input with a 56Ω resistor when the device is configured for an inverting gain in 50Ω applications (terminate with 88Ω in 75Ω applications). Terminate the input with a 49.9Ω resistor in the noninverting case. Output terminating resistors should directly match cable impedances in either configuration.

Layout Techniques

Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the buffer's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following guidelines when designing the board:

- Don't use wire-wrapped boards. They are too inductive.
- Don't use IC sockets. They increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

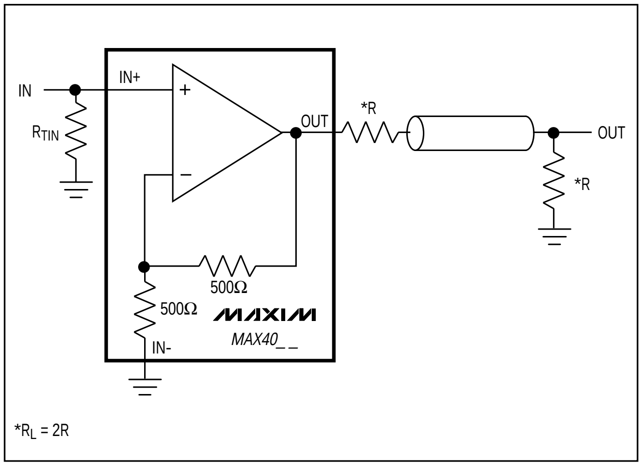


Figure 1a. Noninverting Gain Configuration (A_V = +2V/V)

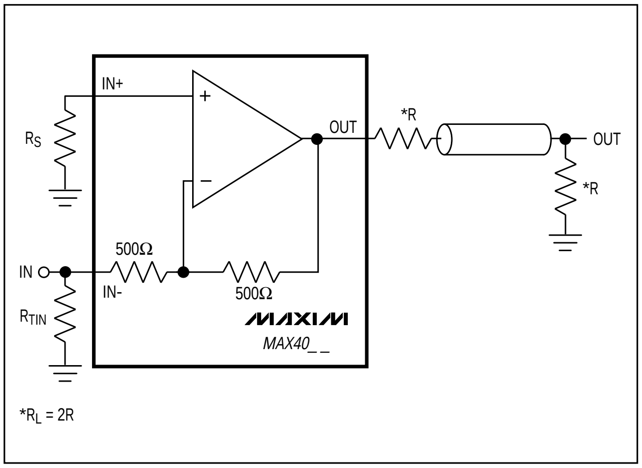


Figure 1b. Inverting Gain Configuration (A_V = -1V/V)

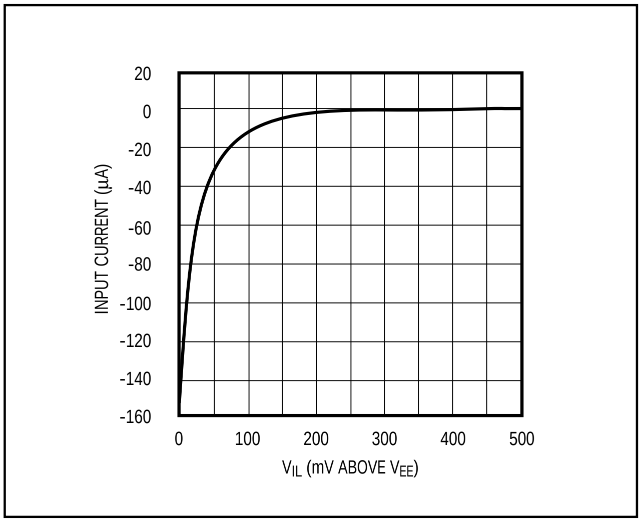


Figure 2. Enable Logic-Low Input Current vs. Enable Logic-Low Threshold

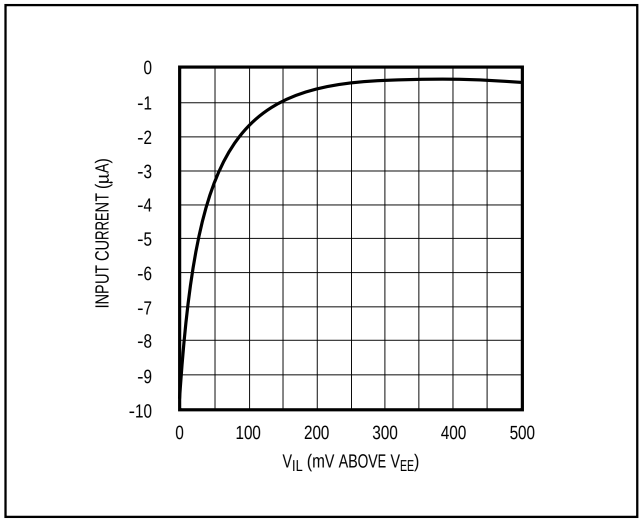


Figure 4. Enable Logic-Low Input Current vs. Enable Logic-Low Threshold with 10kΩ Series Resistor

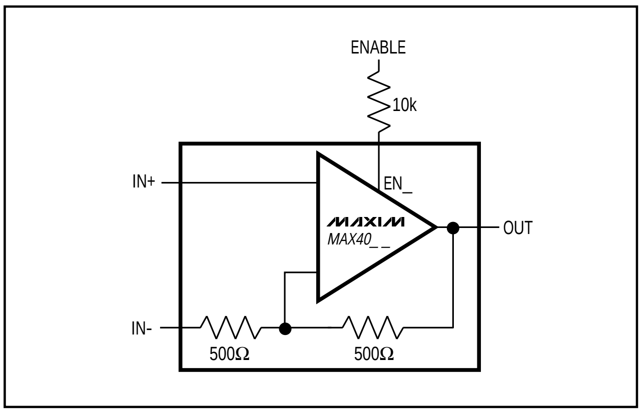


Figure 3. Circuit to Reduce Enable Logic-Low Input Current

Input Voltage Range and Output Swing

The input range for the MAX4014 family extends from (V_{EE} - 100mV) to (V_{CC} - 2.25V). Input ground sensing increases the dynamic range for single-supply applications. The outputs drive a 2kΩ load to within 60mV of the power-suply rails. With heavier loads, the output swing is reduced as shown in the *Electrical Characteristics* and the *Typical Operating Characteristics*. As the load increases, the input range is effectively limited by the output-drive capability, since the buffers have a fixed voltage gain of +2 or -1.

For example, a 50Ω load can typically be driven from 40mV above V_{EE} to 1.6V below V_{CC}, or 40mV to 3.4V when operating from a single +5V supply. If the buffer is operated in the noninverting, gain of +2 configuration with the inverting input grounded, the effective input voltage range becomes 20mV to 1.7V, instead of the -100mV to 2.75V indicated by the *Electrical Characteristics*. Beyond the effective input range, the buffer output is a nonlinear function of the input, but it will not undergo phase reversal or latchup.

Enable

The MAX4019 has an enable feature (EN_) that allows the buffer to be placed in a low-power state. When the buffers are disabled, the supply current will not exceed 550µA per buffer.

As the voltage at the EN_ pin approaches the negative supply rail, the EN_ input current rises. Figure 2 shows a graph of EN_ input current versus EN_ pin voltage. Figure 3 shows the addition of an optional resistor in series with the EN pin, to limit the magnitude of the current increase. Figure 4 displays the resulting EN pin input current to voltage relationship.

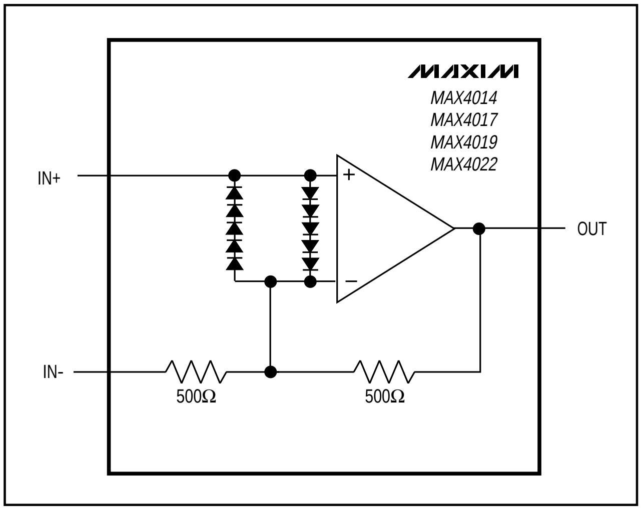


Figure 5. Input Protection Circuit

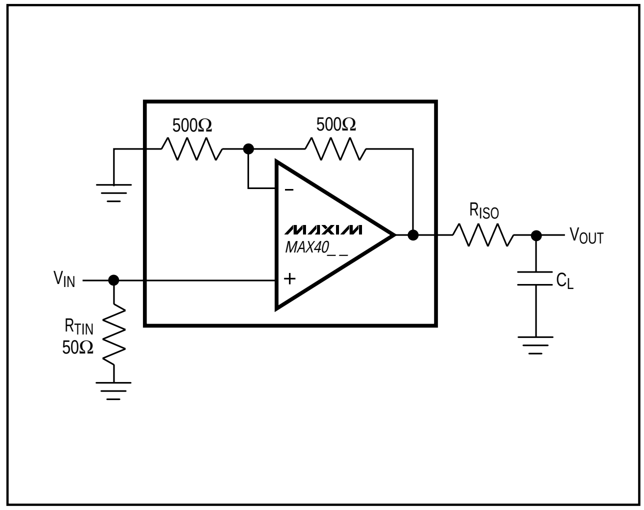


Figure 7. Driving a Capacitive Load through an Isolation Resistor

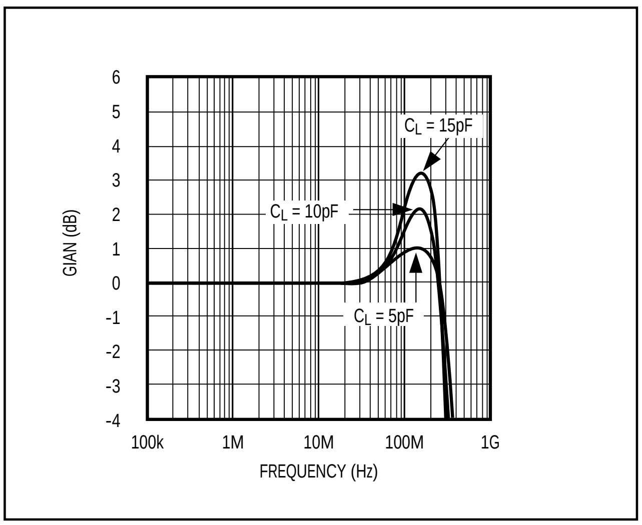


Figure 6. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

Disabled Output Resistance

The MAX4014/MAX4017/MAX4019/MAX4022 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages, as shown in Figure 5. This protection circuitry consists of five back-to-back Schottky diodes between IN_+ and IN_-. These diodes lower the disabled output resistance from 1kΩ to 500Ω when the output voltage is 3V greater or less than the voltage at IN_+. Under these conditions, the input protection diodes will be forward biased, lowering the disabled output resistance to 500Ω.

Output Capacitive Loading and Stability

The MAX4014/MAX4017/MAX4019/MAX4022 provide maximum AC performance with no load capacitance. This is the case when the load is a properly terminated transmission line. However, they are designed to drive up 25pF of load capacitance without oscillating, but with reduced AC performance.

Driving large capacitive loads increases the chance of oscillations occurring in most amplifier circuits. This is especially true for circuits with high loop gains, such as voltage followers. The buffer's output resistance and the load capacitor combine to add a pole and excess phase to the loop response. If the frequency of this pole is low enough to interfere with the loop response and degrade phase margin sufficiently, oscillations can occur.

A second problem when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier's gain margin.

Figure 6 shows the frequency response of the MAX4014/MAX4017/MAX4019/MAX4022 under different capacitive loads. To drive loads with greater than 25pF of capacitance or to settle out some of the peaking, the output requires an isolation resistor like the one shown in

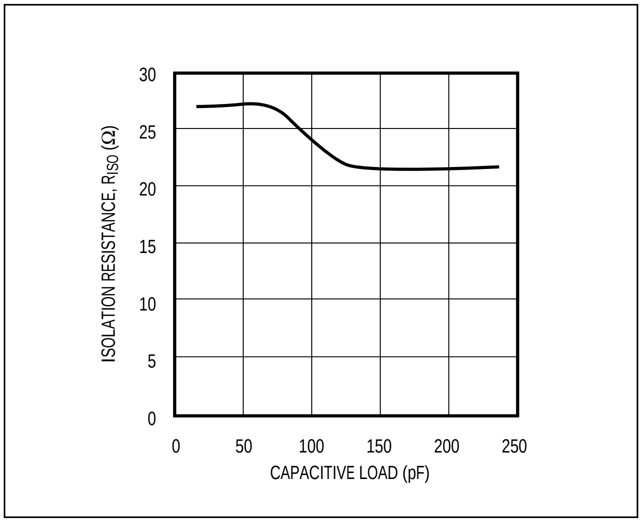


Figure 8. Capacitive Load vs. Isolation Resistance

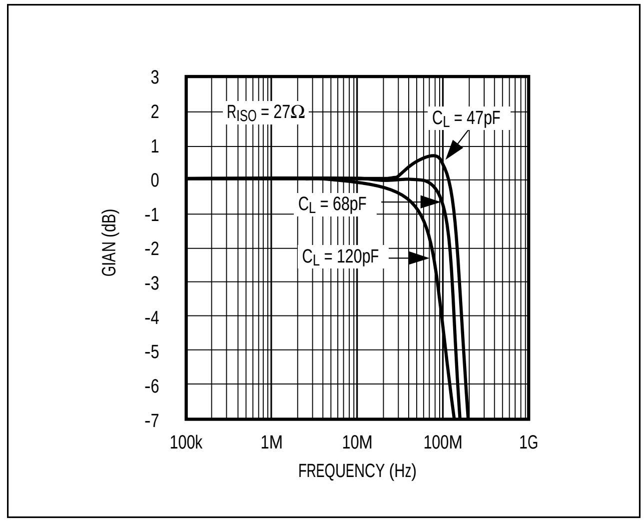


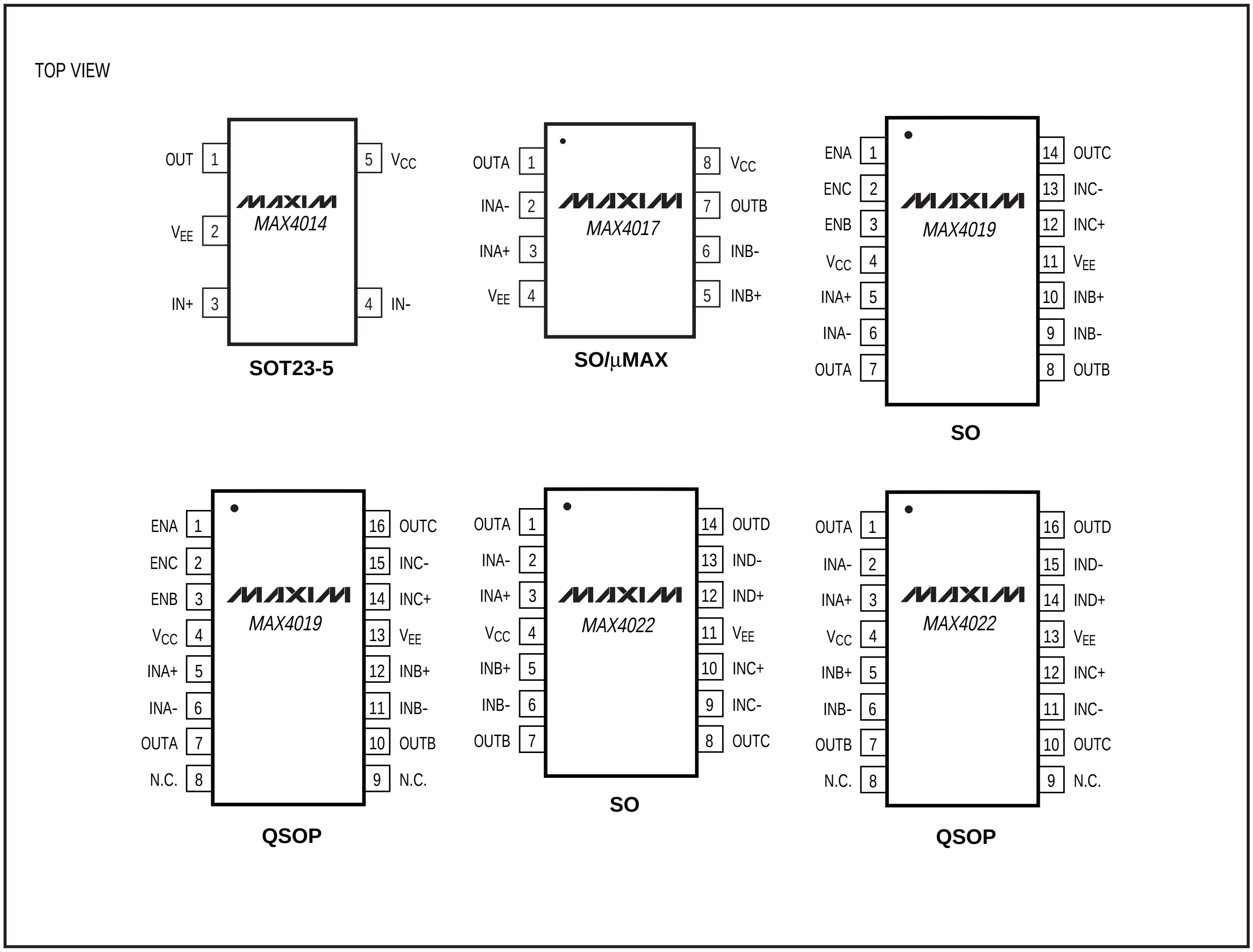
Figure 9. Small-Signal Gain vs. Frequency with Load Capacitance and 27Ω Isolation Resistor

Figure 7. Figure 8 is a graph of the optimal isolation resistor versus load capacitance. Figure 9 shows the frequency response of the MAX4014/MAX4017/MAX4019/MAX4022 when driving capacitive loads with a 27Ω isolation resistor.

Coaxial cables and other transmission lines are easily driven when properly terminated at both ends with their characteristic impedance. Driving back-terminated transmission lines essentially eliminates the lines' capacitance.

Low-Cost, High-Speed, Single-Supply, Gain of +2 Buffers with Rail-to-Rail Outputs in SOT23

Pin Configurations



Chip Information

PART NUMBER	NO. OF TRANSISTORS
MAX4014	95
MAX4017	190
MAX4019	299
MAX4022	362

SUBSTRATE CONNECTED TO V_{EE}

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