

EM128V16 Family

128Kx16 bit Ultra-Low Power Asynchronous Static RAM

Overview

The EM128V16 is an integrated memory device containing a low power 2 Mbit Static Random Access Memory organized as 131,072 words by 16 bits. The design is identical to NanoAmp's EM128Q16 with the exception of a single Chip Enable pin for compatibility with certain competitor devices. The device is fabricated using NanoAmp's advanced CMOS process and high-speed/ultra low-power/low-voltage circuit technology.

These designs are unique in their combination of fast access time and very low power making them very suitable for high performance battery powered applications such as cellular phones and hand held GPS navigation devices.

Features

- **Wide Voltage Range:**
2.3 to 3.0 Volts
- **Extended Temperature Range:**
-40 to +85 °C
- **Fast Cycle Time:**
 $T_{ACC} < 55 \text{ ns @ } 2.3\text{V}$
 $T_{ACC} < 35 \text{ ns @ } 2.7\text{V}$
- **Very Low Operating Current:**
 $I_{CC} < 2.0 \text{ mA typical at } 2.5\text{V, } 1 \text{ Mhz}$
- **Very Low Standby Current:**
 $I_{SB} < 10 \mu\text{A @ } 55 \text{ °C}$
- **44-Pin TSOP, 48-Pin BGA Available**

FIGURE 1: Pin Configurations

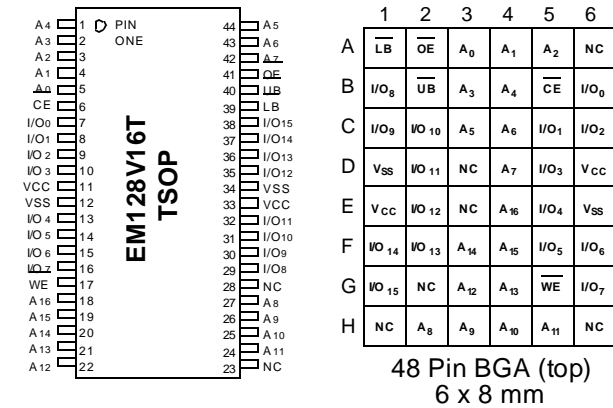


TABLE 1: Pin Descriptions

Pin Name	Pin Function
A ₀ -A ₁₆	Address Inputs
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{LB}}$	Lower Byte Enable Input
$\overline{\text{UB}}$	Upper Byte Enable Input
I/O ₀ -I/O ₁₅	Data Inputs/Outputs
NC	Not Connected
V _{CC}	Power
V _{SS}	Ground

FIGURE 2: Typical Operating Envelope (R/W Mix)

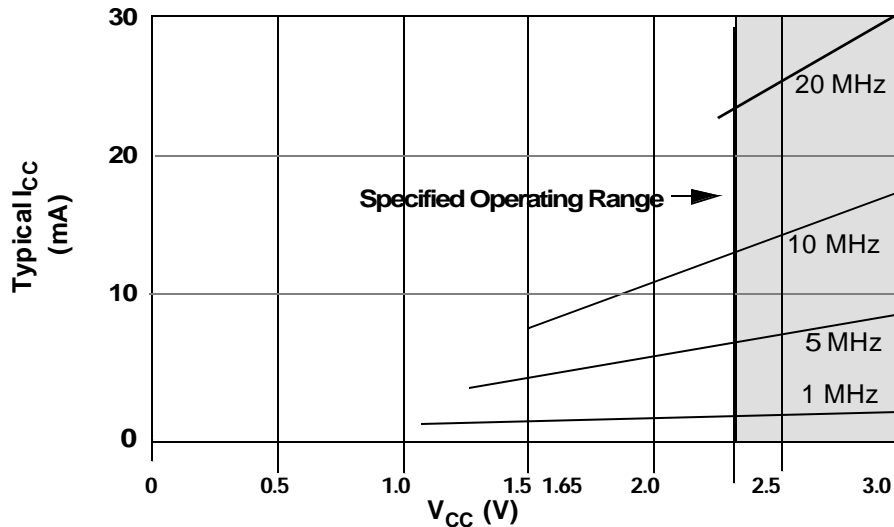


FIGURE 3: Functional Block Diagram

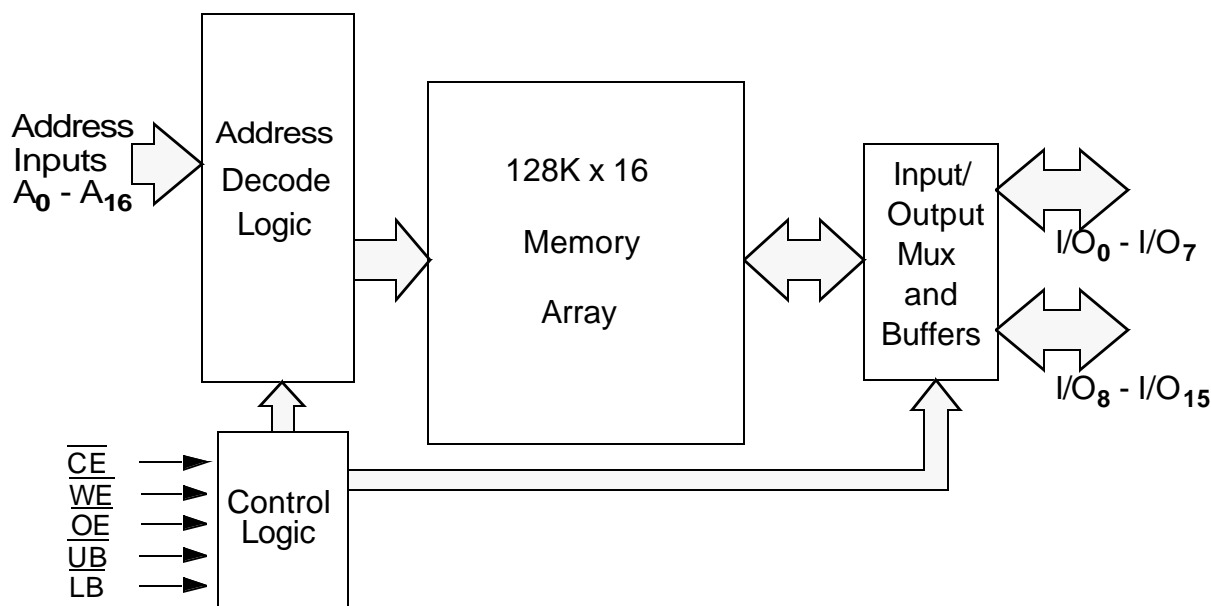


TABLE 2: Functional Description

\overline{CE}	\overline{WE}	\overline{OE}	\overline{UB}	\overline{LB}	I/O ₀ - I/O ₁₅ ¹	MODE	POWER
H	X	X	X	X	High Z	Standby ²	Standby
L	X	X	H	H	High Z	Active	Standby ⁴
L	L	X ³	L ¹	L ¹	Data In	Write ³	Active -> Standby ⁴
L	H	L	L ¹	L ¹	Data Out	Read	Active -> Standby ⁴
L	H	H	L ¹	L ¹	High Z	Active	Standby ⁴

1. When \overline{UB} and \overline{LB} are in select mode (low), I/O₀ - I/O₁₅ are affected as shown. When \overline{LB} only is in the select mode only I/O₀ - I/O₇ are affected as shown. When \overline{UB} is in the select mode only I/O₈ - I/O₁₅ are affected as shown.
2. When the device is in standby mode, control inputs (\overline{WE} , \overline{OE} , \overline{UB} , and \overline{LB}), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When \overline{WE} is invoked, the \overline{OE} input is internally disabled and has no effect on the circuit.
4. The device will consume active power in this mode whenever addresses are changed. Data inputs are internally isolated from any external influence.

TABLE 3: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF
I/O Capacitance	C _{I/O}	V _{IN} = 0V, f = 1 MHz, T _A = 25°C		8	pF

Note: These parameters are verified in device characterization and are not 100% tested

TABLE 4: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	-0.3 to $V_{CC}+0.3$	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.3 to 4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260 °C, 10sec(Lead only)	°C

* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: Operating Characteristics (Over specified Temperature Range)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		2.3		3.0	V
Data Retention Voltage	V_{DR}	Chip Disabled (Note 3)	1.2			V
Input High Voltage	V_{IH}		$0.7V_{CC}$		$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}		-0.5		$0.3V_{CC}$	V
Output High Voltage	V_{OH}	$I_{OH} = 0.2mA$	$V_{CC}-0.3$			V
Output Low Voltage	V_{OL}	$I_{OL} = -0.2mA$			0.3	V
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}			0.5	μA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ or Chip Disabled			0.5	μA
Read/Write Operating Supply Current (Note 1)	I_{CC1}	$V_{IN} = V_{IH}$ or V_{IL} Chip Enabled, $I_{out} = 0$			0.5fV	mA
Read/Write Quiescent Operating Supply Current (Note 2)	I_{CC3}	$V_{IN} = V_{CC}$ or 0V Chip Enabled, $I_{out} = 0$ $f = 0$, $t_A = 55^\circ C$			10	μA
Operating Standby Current (Note 2)	I_{SB1}	$V_{IN} = V_{CC}$ or 0V Chip Disabled, $t_A = 55^\circ C$			10	μA
Maximum Standby Current (Note 2)	I_{SB2}	$V_{IN} = V_{CC}$ or 0V, $V_{CC} = 3.0 V$ Chip Disabled, $t_A = 85^\circ C$			40	μA
Maximum Data Retention Current (Note 2)	I_{DR}	$V_{CC} = 1.2V$, $V_{IN} = V_{CC}$ or 0 Chip Disabled, $t_A = 55^\circ C$			1	μA

1. Operating current is a linear function of operating frequency and voltage. You may calculate operating current using the formula shown with operating frequency (f) expressed in MHz and operating voltage (V) in volts. Example: When operating at 2 MHz at 3.0 volts the device will draw a typical active current of $0.5 \times 2 \times 3 = 3.0$ mA in the page access mode. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
2. This device assumes a standby mode if the chip is disabled (\overline{CE} high). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) regardless of the state of \overline{CE} . In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.
3. The Chip is Disabled when \overline{CE} is high. The Chip is Enabled when \overline{CE} is low.

TABLE 6: Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5V_{CC}$
Output Load	CL = 30pF
Operating Temperature	-40 to +85°C

TABLE 7: Read Cycle Timing

Item	Symbol	2.3 - 3.0 V		2.7 - 3.0 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	55		35		ns
Address Access Time	t_{AA}		55		35	ns
Chip Enable to Valid Output	t_{CO}		55		35	ns
Output Enable to Valid Output	t_{OE}		20		15	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		20		15	ns
Chip Enable to Low-Z output	t_{LZ}	5		5		ns
Output Enable to Low-Z Output	t_{OLZ}	3		3		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	5		5		ns
Chip Enable to High-Z Output	t_{HZ}	5	15	5	15	ns
Output Disable to High-Z Output	t_{OHZ}	5	15	5	15	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	5	15	5	15	ns
Output Hold from Address Change	t_{OH}	5		5		ns

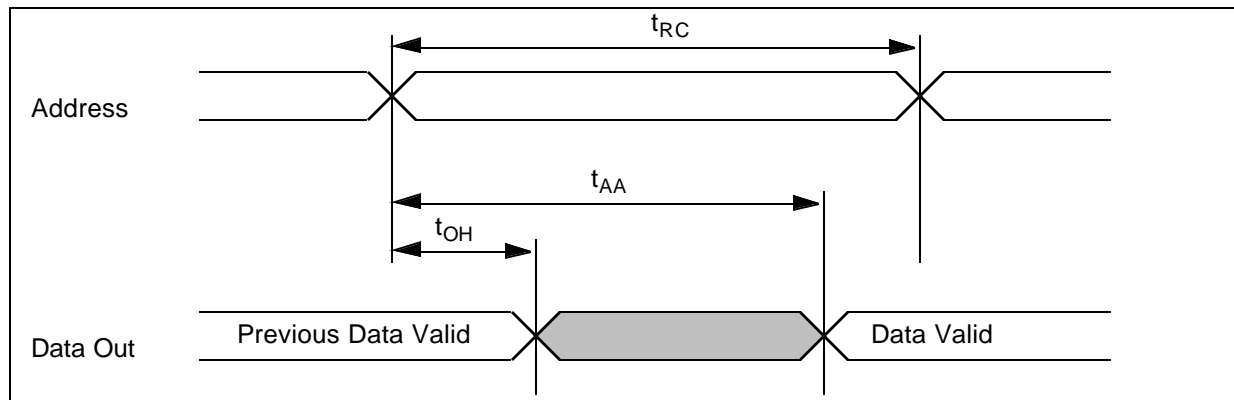
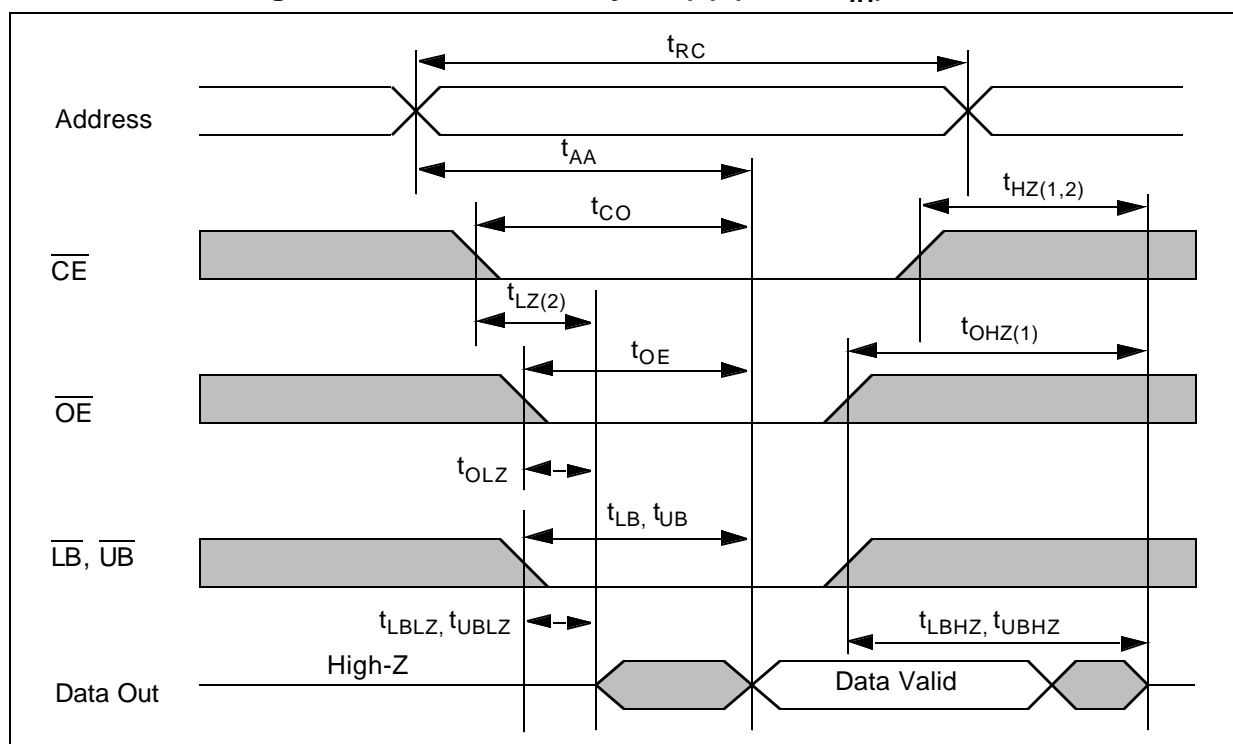
FIGURE 4: Timing of Read Cycle (1) ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)

FIGURE 5: Timing Waveform of Read Cycle (2) ($\overline{WE} = V_{IH}$)**TABLE 8: Write Cycle Timing**

Item	Symbol	2.3 - 3.0 V		2.7 - 3.0 V		Units
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	55		35		ns
Chip Enable to End of Write	t_{CW}	30		25		ns
Address Valid to End of Write	t_{AW}	30		25		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	30		25		ns
Address Set-up Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	30		25		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		15		10	ns
Data to Write Time Overlap	t_{DW}	20		15		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns

FIGURE 6: Timing Waveform of Write Cycle (1) (\overline{WE} control)

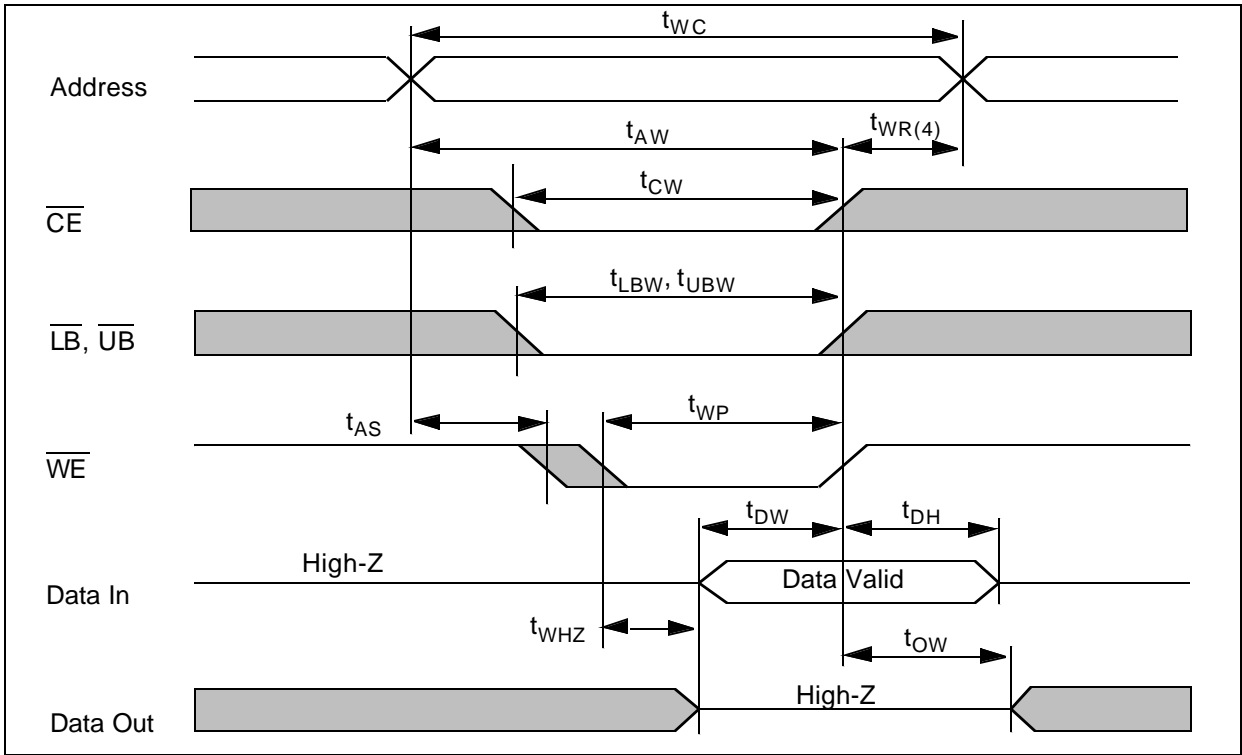


FIGURE 7: Timing Waveform of Write Cycle (2) (\overline{CE} Control)

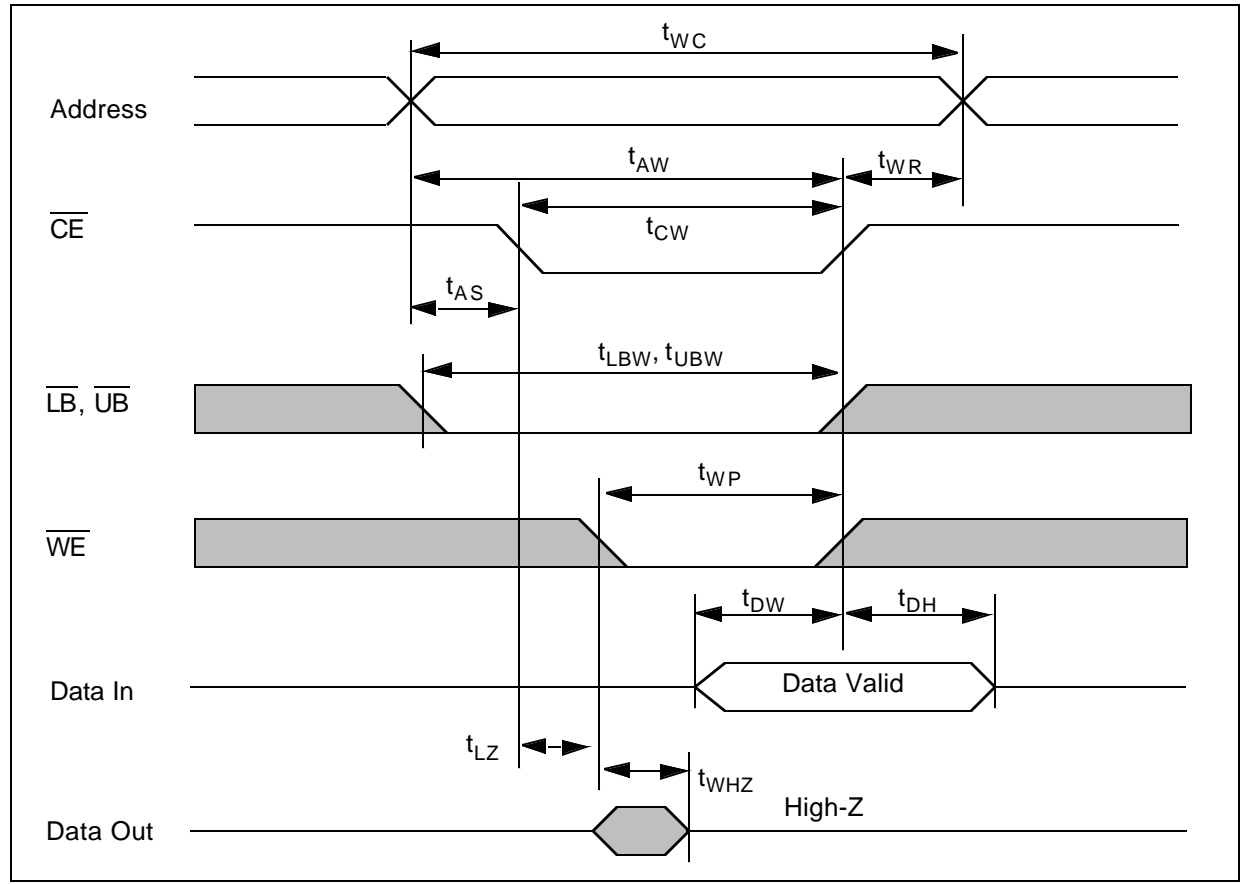
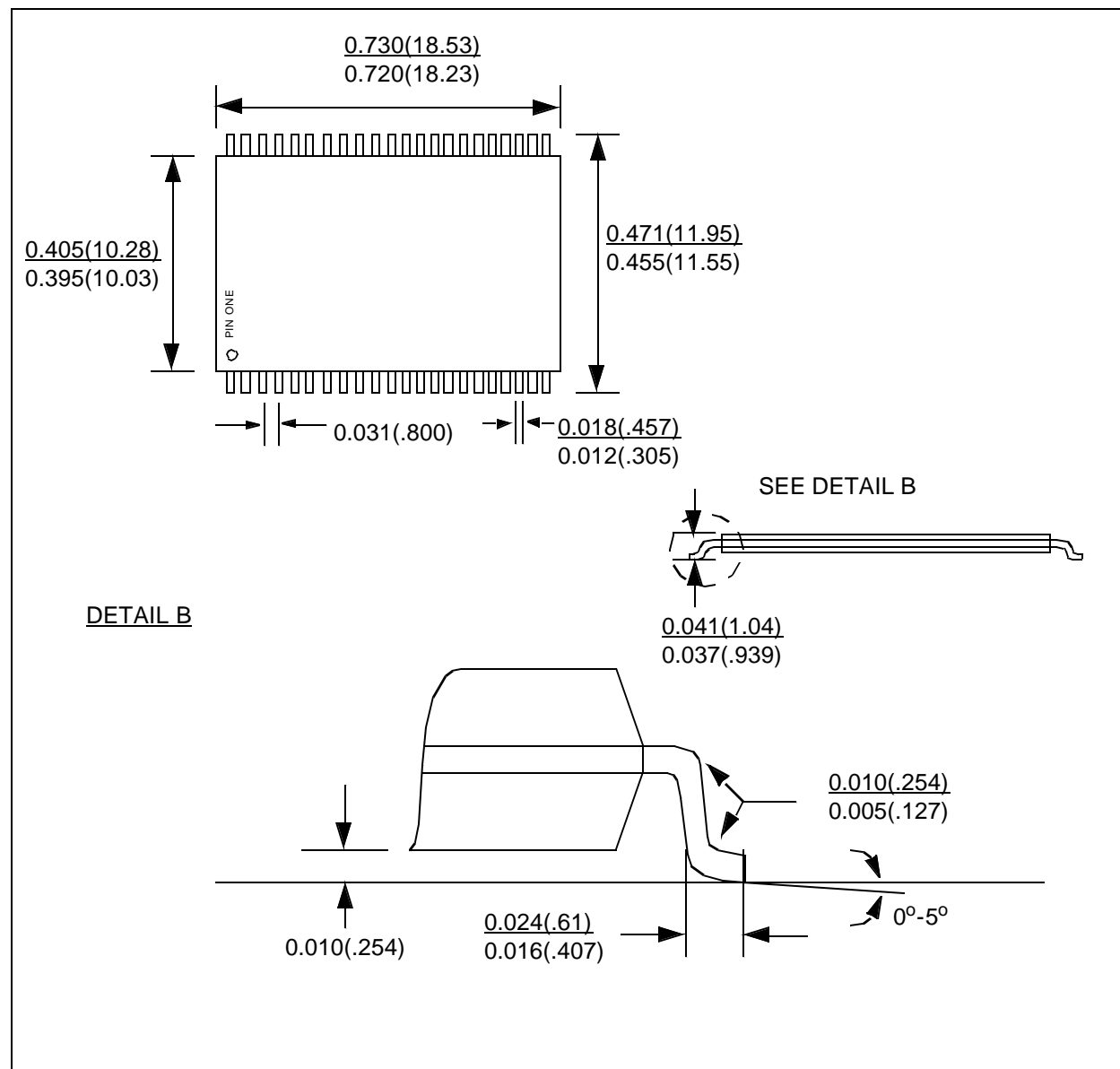
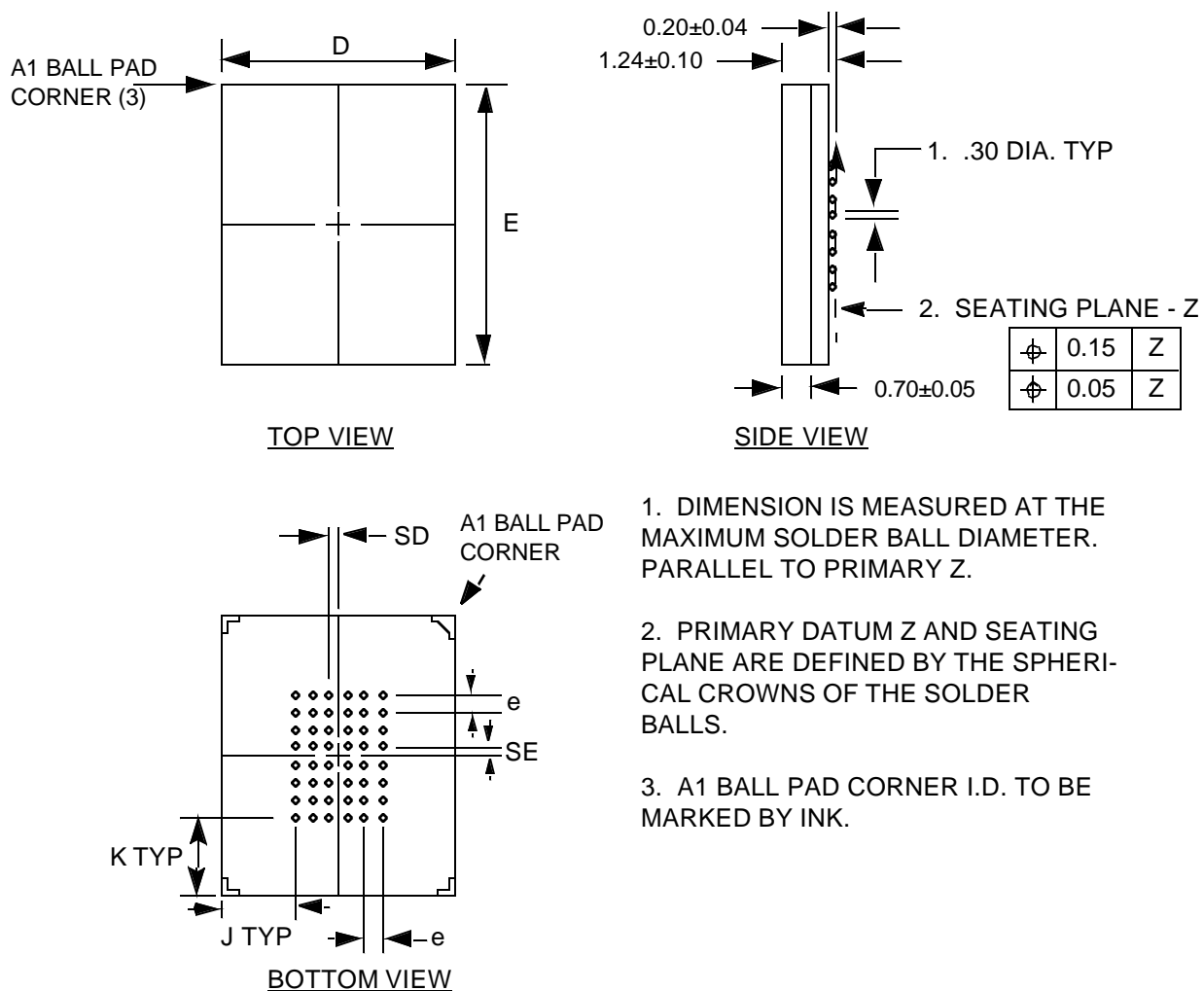


FIGURE 8: 44-LEAD TSOP PACKAGE (T44)



Note:

1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

FIGURE 9: BALL GRID ARRAY PACKAGING**TABLE 9: Dimensions (mm)**

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6	8	0.375	0.375	1.125	1.375	FULL

TABLE 10: Ordering Information

Part Number*	Package	Temperature Range	Voltage Range	Speed (@2.3V)
EM128V16B	48 pin BGA	-40 to +85°C	2.3 to 3.0 V	55 ns
EM128V16T	44 pin TSOP	-40 to +85°C	2.3 to 3.0 V	55 ns

* This part number must appear on your order.

TABLE 11: Revision History

Revision	Date	Change Description
01	Feb 2000	Initial Preliminary Release
02	Mar 27, 2000	Reversed I/O ₁ and I/O ₂ in figure 1: BGA pin configuration
03	May 1, 2000	Expanded voltage range to 2.3 to 3.0 volts
04	July 15, 2000	Added Specifications for 2.7 to 3.0 volts operation
05	Sept. 11, 2000	Final Release
06	Mar 2001	Minor errata changes

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