19-0798; Rev 0; 4/07

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

General Description

The MAX3845 is a TMDS® 2-to-4 fanout switch and cable driver for multimonitor distribution of DVI™ or HDMI™ signaling up to 1.65Gbps. Both inputs and outputs are standard TMDS signaling as per DVI and HDMI standards. Because TMDS links are "point-to-point," buffering is required for fanout applications.

Four DVI/HDMI TMDS outputs are provided for fanout distribution. Each TMDS output can be independently sourced from either input or can be turned off. Each TMDS input or output is composed of four differential channels that can be arbitrarily assigned to the three data signals and the 1/10th-rate clock. The data rate depends on resolution, but it can vary from 250Mbps (VGA) to 1.65Gbps (UXGA or 1080p/60).

Typical applications include multiroom display of the same video source or industrial/commercial signage applications such as airport monitors or trading room floor displays. The MAX3845 includes selectable output preemphasis that extends output cable reach up to an additional 7m.

For DDC switching, use the companion MAX4814E* 2:4 low-resistance CMOS crosspoint switch. DDC switching is not required for applications that connect DDC to one reference monitor only.

The MAX3845 can be configured to create a 2 x 8 or 4 x 4 switch (see the *Typical Operating Circuit* diagrams).

The MAX3845 is available in a 14mm × 14mm, 100-pin TQFP-EP package and operates over the -10°C to +85°C temperature range.

Applications

Digital Signage and Industrial Display

PC Monitor Distribution

Home A/V Receivers

DVI/HDMI Distribution Amplifiers

DVI/HDMI Crosspoint Switches

Pin Configuration appears at end of data sheet.

TMDS is a registered trademark of Silicon Image, Inc.

DVI is a trademark of Digital Display Working Group.

HDMI is a trademark of HDMI Licensing, LCC.

**Future product—contact factory for availability.*

Features

- **Two DVI/HDMI TMDS-Compatible Inputs and Four DVI/HDMI TMDS-Compatible Outputs**
- **Save Power by Turning Off Unused Outputs**
- **Each Output Independently Selects Input 1 or Input 2**
- **Three Preemphasis Settings Extend Cable Reach Up to 7m**
- **Operation Up to 1.65Gbps**
- **14mm x 14mm, 100-Pin TQFP Package with Exposed Paddle for Heat Sinking**
- **3.3V Power Supply**
- **TMDS Data (x3) and Clock (x1) Can Be Arbitrarily Assigned to the Four Identical Switched Paths (A, B, C, and D)**

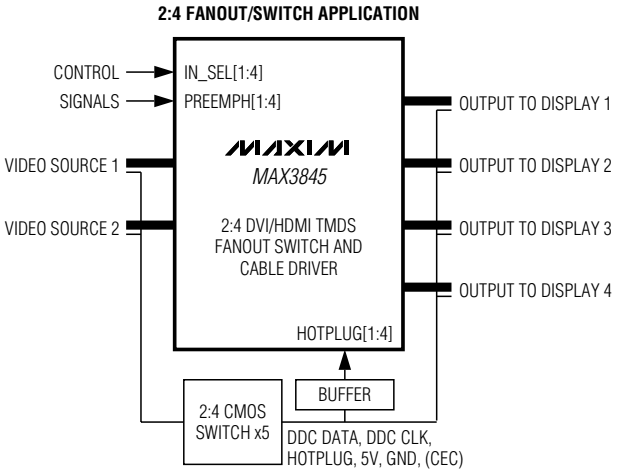
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3845UCQ+	-10°C to +85°C	100 TQFP-EP	C100E-3

+Denotes a lead-free package.

EP = Exposed pad.

Typical Operating Circuit



Typical Operating Circuits continued at end of data sheet.

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}) .....-0.3V to +5.5V
Voltage Range at HOTPLUGx Pins .....-0.3V to +6.0V
Voltage Range at LVTTL, LVCMOS, I/O Pins .....-0.3V to +5.5V
Voltage Range at CML Output Pins .....-0.3V to +5.5V
Voltage Range at CML Input Pins
(CML short to GND duration < 1s).....-0.3V to +4.0V
Voltage Between Any Input CML I/O
Complementary Pair .....±3.3V
Voltage Range at LOSMUTE_EN .....-0.3V to +5.5V
Voltage Between Any Output CML I/O
Complementary Pair.....±3.6V
Continuous Power Dissipation (T_A = +70°C)
100-Pin TQFP-EP (derate 45.5mW/°C
above +70°C) 3636mW
Operating Junction Temperature .....-55°C to +150°C
Storage Temperature Range .....-55°C to +150°C
Die Attach Temperature .....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to +3.6V, T_A = -10°C to +85°C. Typical values are at V_{CC} = +3.3V, external terminations = 50Ω ±1%, TMDS rate = 250Mbps to 1.65Gbps, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Current	I_{CC}	PREEMPH[1:4] = high, OUT_LEVEL = high, current into V_{CC} pins, 1200mV_{P-P} = V_{IN}			454	626	mA
Supply-Noise Tolerance		DC to 500kHz			50		mV_{P-P}
SKIN-EFFECT EQUALIZER PEAKING							
Fixed Rx Equalizer Compensation		Gain at 825MHz			1		dB
Settable Tx Preemphasis		PREEMPHx pin = low			0		
		PREEMPHx pin = open			3		
		PREEMPHx pin = high			6		
JITTER PERFORMANCE							
Residual Deterministic Jitter (Measured at end of cable having ideal skin-effect loss and connectors, e.g., Gore Twin Coax, Amphenol Skewclear Twinax, with SMA connectors) (Note 2)		200Ω back termination	0dB cable loss, no preemphasis		0.04	0.12	UI
			3dB cable loss, +3dB preemphasis		0.05	0.12	
			6dB cable loss, +6dB preemphasis		0.07	0.12	
		No back termination	0dB cable loss, no preemphasis		0.07	0.2	
			3dB cable loss, +3dB preemphasis		0.08	0.2	
			6dB cable loss, +6dB preemphasis		0.10	0.2	
Residual Random Jitter (Note 3)		Measured with source T_r/T_f = 250ps			1.5	2	ps_{RMS}
CML INPUTS (SOURCE SIDE)							
Differential-Input Voltage Swing	V_{ID}	At cable input		400		2000	mV_{P-P}
Common-Mode Input Voltage	V_{CM}			V_{CC} - 1000		V_{CC}	mV
Input Voltage When Disconnected				V_{CC} - 10		V_{CC} + 10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to +3.6V, T_A = -10°C to +85°C. Typical values are at V_{CC} = +3.3V, external terminations = 50Ω ±1%, TMDS rate = 250Mbps to 1.65Gbps, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Resistance	R_{IN}	Single-ended	45	50	55	Ω
Input LOS/Mute Threshold		Differential peak-peak		150		mV
Input LOS/Mute Response Time		Deassert mute		1.2		µs
		Assert mute		0.6		
Input Return Loss		Differential, ≤ 1.6GHz		19		dB
CML OUTPUTS (CABLE SIDE)						
Differential-Output Voltage Swing	V_{OD}	No preemphasis, no back termination, OUT_LEVEL = low	900	1050	1200	mV_{P-P}
		No preemphasis, 200Ω back termination, OUT_LEVEL = high	825	925	1050	
Output-Voltage High	V_{OH}	Single-ended, no back termination	V_{CC} - 10		V_{CC} + 10	mV
Output Voltage During Power-Down	V_{OFF}	Single-ended, PWRDWN_x = low or V_{CC} = 0V	V_{CC} - 10		V_{CC} + 10	
Rise/Fall Time		20% to 80% (T_A = 0°C to +85°C)	75	90	140	ps
Intrapair Skew				12	40	
Interpair Skew		Worst case among A, B, C, and D of an output		35	60	
CONTROL INTERFACE						
LVTTL Input High Voltage	V_{IH}		2.0			V
LVTTL Input Low Voltage	V_{IL}	All except IN_SELx pins			1.0	
		IN_SELx pins			0.8	
LVTTL Input High Current		$V_{IH(MIN)} < V_{IN} < V_{IH(MAX)}$			100	µA
LVTTL Input Low Current		$V_{IL(MIN)} < V_{IN} < V_{IL(MAX)}$, All except OUT_LEVEL pin			150	
		$V_{IL(MIN)} < V_{IN} < V_{IL(MAX)}$, OUT_LEVEL pin			500	
HOTPLUGx Input High Voltage		Typical input 30kΩ to GND	V_{CC} - 0.2		5.5	V
HOTPLUGx Input Low Voltage					1.5	

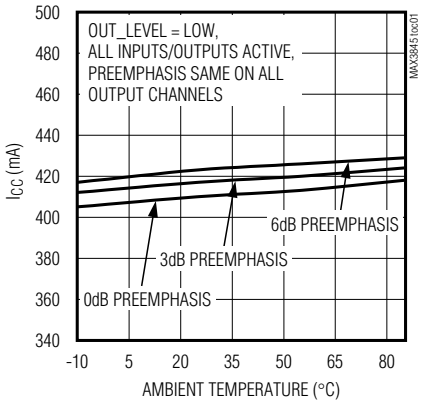
Note 1: AC specifications are guaranteed by design and characterization.
Note 2: Test pattern is a 2^{10} - 1 PRBS + 20 ones + 2^{10} - 1 PRBS (inverted) + 20 zeros.
Note 3: Test pattern is a 1111 0000 pattern at 1.65Gbps.

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

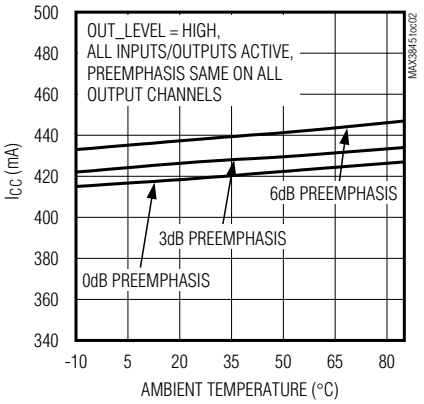
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^{10} - 1 PRBS + 20 ones + 2^{10} - 1 PRBS (inverted) + 20 zeros, unless otherwise noted.)

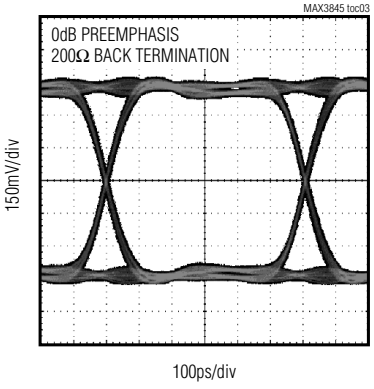
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



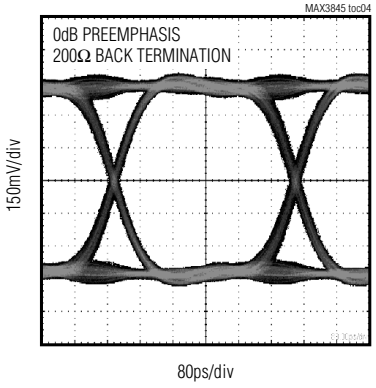
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



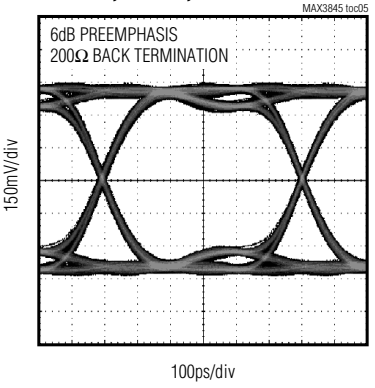
OUTPUT EYE DIAGRAM AT 1.65Gbps SHORT LOW-LOSS SMA CABLE



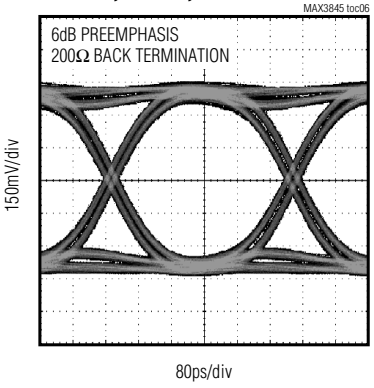
OUTPUT EYE DIAGRAM AT 2.25Gbps SHORT LOW-LOSS SMA CABLE



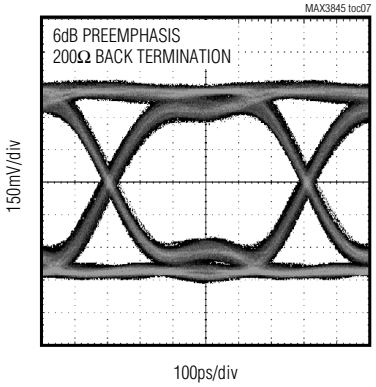
OUTPUT EYE DIAGRAM AT 1.65Gbps 6dB LOSS, 24AWG, 25ft TWIN-AX CABLE



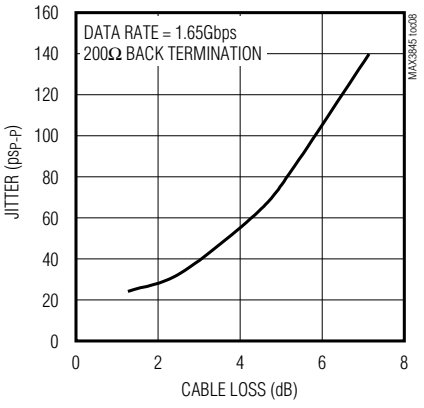
OUTPUT EYE DIAGRAM AT 2.25Gbps 6dB LOSS, 24AWG, 25ft TWIN-AX CABLE



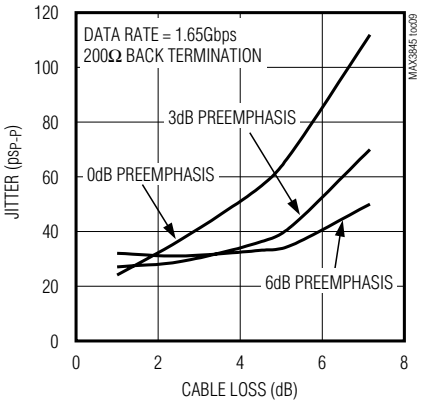
OUTPUT EYE DIAGRAM AT 1.65Gbps THROUGH 2m DVI TO HDMI CABLE



JITTER vs. INPUT-SIDE CABLE LOSS AT 825 MHz



JITTER vs. OUTPUT-SIDE CABLE LOSS AT 825 MHz

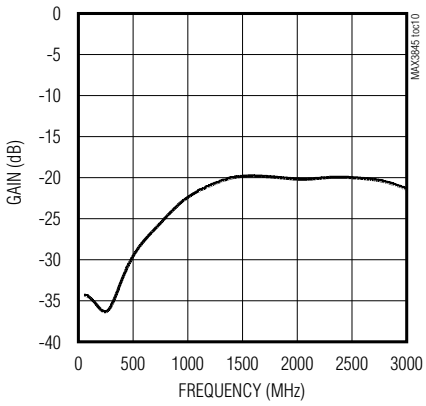


DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

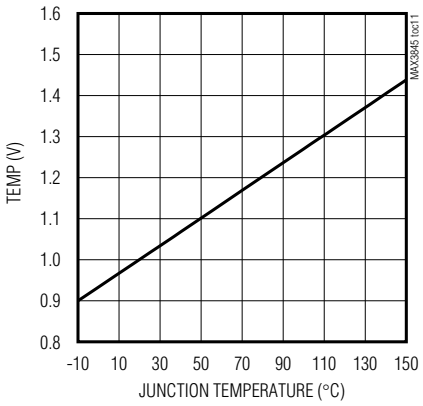
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = +3.3V, T_A = +25°C, data pattern = 2^{10} - 1 PRBS + 20 ones + 2^{10} - 1 PRBS (inverted) + 20 zeros, unless otherwise noted.)

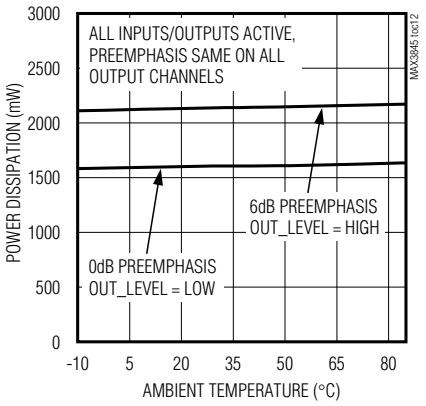
DIFFERENTIAL-INPUT RETURN LOSS vs. FREQUENCY



TEMP VOLTAGE vs. JUNCTION TEMPERATURE



POWER DISSIPATION vs. AMBIENT TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 4, 7, 10, 97, 100	V_{CC1}	Positive Power-Supply Connection. Powers input channel 1 and output channels 1 and 2.
2, 5, 8, 98	IN1_B+, IN1_C+, IN1_D+, IN1_A+	Noninverting TMDS CML Input, Channel 1
3, 6, 9, 99	IN1_B-, IN1_C-, IN1_D-, IN1_A-	Inverting TMDS CML Input, Channel 1
11	PWRDWN_1	Power-Down, LVTTL/LVCMOS Input. Force high or leave open to power down input channel 1. Force low to enable input channel 1. The MAX3845 powers down if both PWRDWN_1 and PWRDWN_2 are forced high or left open.
12	V_{CC3}	Positive Power-Supply Connection. Powers the temp-sense circuitry.
13	LOSMUTE_EN	LOS MUTE Enable Input. Connect to V_{CC} for typical operation. Connect to GND to disable the LOS MUTE function.
14	TEMP	Junction Temperature Sensor. Attach a ground-referenced voltage DMM to this pin to measure the die's junction temperature (see the V_{CC3} pin description). Leave open if not used.
15	PWRDWN_2	Power-Down, LVTTL/LVCMOS Input. Force high or leave open to power down input channel 2. Force low to enable input channel 2. The MAX3845 powers down if both PWRDWN_1 and PWRDWN_2 are forced high or left open.
16, 19, 22, 25, 26, 29	V_{CC2}	Positive Power-Supply Connection. Powers input channel 2 and output channels 3 and 4.

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

Pin Description (continued)

PIN	NAME	FUNCTION
17, 20, 23, 27	IN2_A+, IN2_B+, IN2_C+, IN2_D+	Noninverting TMDS, CML Input, Channel 2
18, 21, 24, 28	IN2_A-, IN2_B-, IN2_C-, IN2_D-	Inverting TMDS, CML Input, Channel 2
30, 61, 65, 96	IN_SEL4, IN_SEL3, IN_SEL2, IN_SEL1	Input Select, LVTTL Input. Force high to select input channel 1. Force low to select input channel 2. Leave open to disable the output channel.
31, 62, 64, 95	PREEMPH4, PREEMPH3, PREEMPH2, PREEMPH1	Preemphasis Select, LVTTL/LVCMOS Input. Force high for 6dB of output preemphasis. Leave open for 3dB of output preemphasis. Force low for 0dB of output preemphasis (normal).
32, 46, 80, 94	HOTPLUG4, HOTPLUG3, HOTPLUG2, HOTPLUG1	Hotplug Sense Input. Connect this pin to the display's HOTPLUGx signal (buffered) to allow automatic power-down of the associated output when the display is disconnected. A low-cost quad 5V, noninverting CMOS gate (74ACT32 series) is recommended to buffer the MAX3845 from the HOTPLUGx pin to match HOTPLUG level specifications. If this feature is not used, connect to V_{CC}.
33, 36, 39, 42, 45, 47, 50, 51, 54, 57, 60	GND2	Supply Ground. Ground connection for input channel 2 and output channels 3 and 4.
34, 37, 40, 43	OUT4_D-, OUT4_C-, OUT4_B-, OUT4_A-	Inverting TMDS, CML Output, Channel 4
35, 38, 41, 44	OUT4_D+, OUT4_C+, OUT4_B+, OUT4_A+	Noninverting TMDS, CML Output, Channel 4
48, 52, 55, 58	OUT3_D-, OUT3_C-, OUT3_B-, OUT3_A-,	Inverting TMDS, CML Output, Channel 3
49, 53, 56, 59	OUT3_D+, OUT3_C+, OUT3_B+, OUT3_A+,	Noninverting TMDS, CML Output, Channel 3

Pin Description (continued)

PIN	NAME	FUNCTION
63	OUT_LEVEL	Output Level Select, LVTTL/LVCMOS Input. Force pin low when no back termination is used (11mA of tail current). Force pin high when 200Ω back termination resistors are used (14mA of tail current).
66, 69, 72, 75, 76, 79, 81, 84, 87, 90, 93	GND1	Supply Ground. Ground connection for input channel 1 and output channels 1 and 2.
67, 70, 73, 77	OUT2_D-, OUT2_C-, OUT2_B-, OUT2_A-	Inverting TMDS, CML Output, Channel 2
68, 71, 74, 78	OUT2_D+, OUT2_C+, OUT2_B+, OUT2_A+	Noninverting TMDS, CML Output, Channel 2
82, 85, 88, 91	OUT1_D-, OUT1_C-, OUT1_B-, OUT1_A-	Inverting TMDS, CML Output, Channel 1
83, 86, 89, 92	OUT1_D+, OUT1_C+, OUT1_B+, OUT1_A+	Noninverting TMDS, CML Output, Channel 1
—	EP	Ground. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical operation.

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

Detailed Description

The MAX3845 2:4 DVI/HDMI fanout switch and cable driver accept differential CML input data at rates of 250Mbps up to 1.65Gbps (individual channel data rate). The input portion of the device consists of two independent TMDS inputs, each having four fixed-level equalizers, four limiting amplifiers, a loss-of-signal (LOS) detector, and power-down control. The output portion of the device consists of four independent TMDS outputs, each having four multiplexers, four output buffers with selectable preemphasis, HOTPLUG detection, and channel selection control (Figure 1).

Fixed Input Equalization

All four differential pairs on the MAX3845's TMDS inputs have fixed-level equalizers to compensate for 0in to 6in of FR4 PCB losses. The signal boost is approximately 1dB at 825MHz. If more equalization is desired, use the MAX3814 or MAX3815 in front of the MAX3845 to accommodate long cable lengths.

Limiting Amplifiers

Limiting amplifiers follow the equalizer block to ensure proper signal levels are achieved for the multiplexers.

Loss-of-Signal (LOS) Detectors

Input channel 1 has an LOS detector attached to the IN1_B pair. For input channel 2 the LOS detector is attached to the IN2_C pair. If the received-signal amplitude is smaller than $150mV_{P-P}$ (typical) at IN1_B, all output channels selected to input 1 are muted. Likewise, if a signal smaller than $150mV_{P-P}$ (typical) is at IN2_C, all output channels selected to input 2 are muted.

Multiplexers

Each MAX3845 output has four multiplexers, one for each signal pair contained in the TMDS channel. These connect the output to either input 1 or input 2. The IN_SELx pins control the multiplexers.

Preemphasis Drivers

The preemphasis drivers have three selectable levels of preemphasis: 0dB, 3dB, and 6dB. The preemphasis drivers provide a precompensated signal that allows for extended length cables to be used at the output.

Applications Information

MAX3845 in HDMI 1.3 Systems

The MAX3845 is designed and characterized to operate from 250Mbps to 1.65Gbps. HDMI 1.3 specifies up to 2.25Gbps for 1080p "deep color" and allows a maximum data rate of 3.4Gbps on each of the three data pairs. The MAX3845 operates normally in an HDMI 1.3 system up to 1.65Gbps. The MAX3845 operates at data rates above 1.65Gbps with reduced jitter performance. See the *Typical Operating Characteristics* section for more information.

MAX3845 in HDCP Systems

High-bandwidth digital content protection (HDCP) is a copy protection system employed in some DVI and most HDMI interfaces. Video data is encrypted at the transmitter and decrypted at the receiver. The data scrambling is dependent upon shared keys established during the authentication protocol that occurs over the DDC channel (between the video source and the display). The MAX3845 does not decrypt or reencrypt data. Therefore, HDCP-encrypted video routed through the MAX3845 is only viewable on the display to which the DDC channel is connected. For applications that employ HDCP, the MAX3845 acts as a dual 1:4 switch and not as a fanout device. This means that one video source can be selected to drive any one of four displays, but the video source cannot be replicated on more than one display at the time. Fanout is possible in non-HDCP applications, allowing one video source to simultaneously drive up to four displays.

Output Level Control, Back Termination, and AC-Coupling

The OUT_LEVEL pin is an LVTTL input that allows the user to select between standard output drive current (11mA) or increased output drive current (14mA). The increased output current setting allows back termination resistors to be used on the outputs. The use of back terminations is highly recommended for best signal integrity (see Figures 2 and 3).

If OUT_LEVEL is set low, the standard output drive current (11mA) is consistent with DVI/HDMI architecture and common-mode levels. As per standard, no back termination is used so no reflected energy can be absorbed.

If OUT_LEVEL is set high, the output drive current is increased to 14mA and allows the use of back termination resistors. Two options are available: a differential back termination resistor or two single-ended pullup resistors (see Figures 2 and 3).

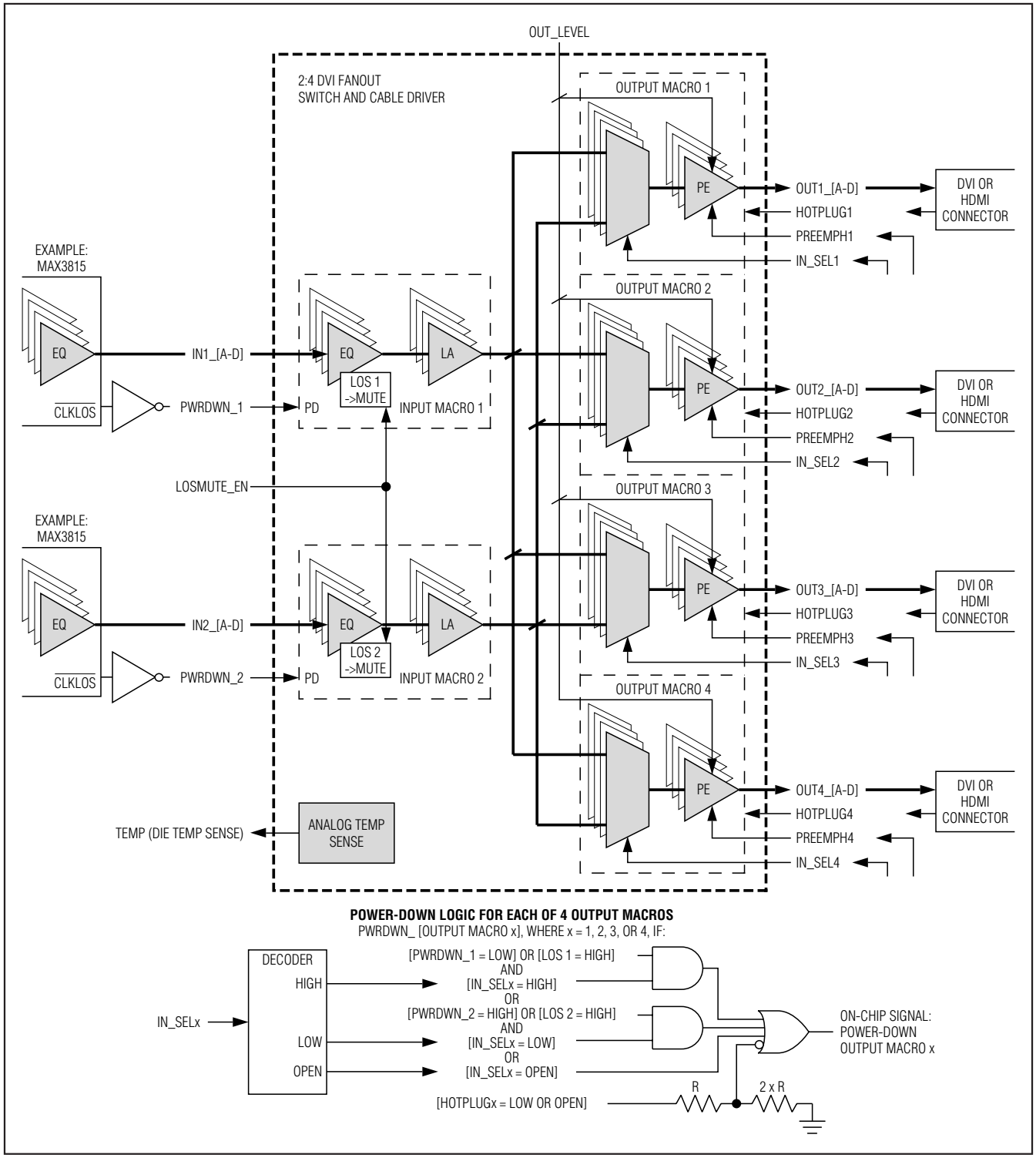


Figure 1. Functional Diagram

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

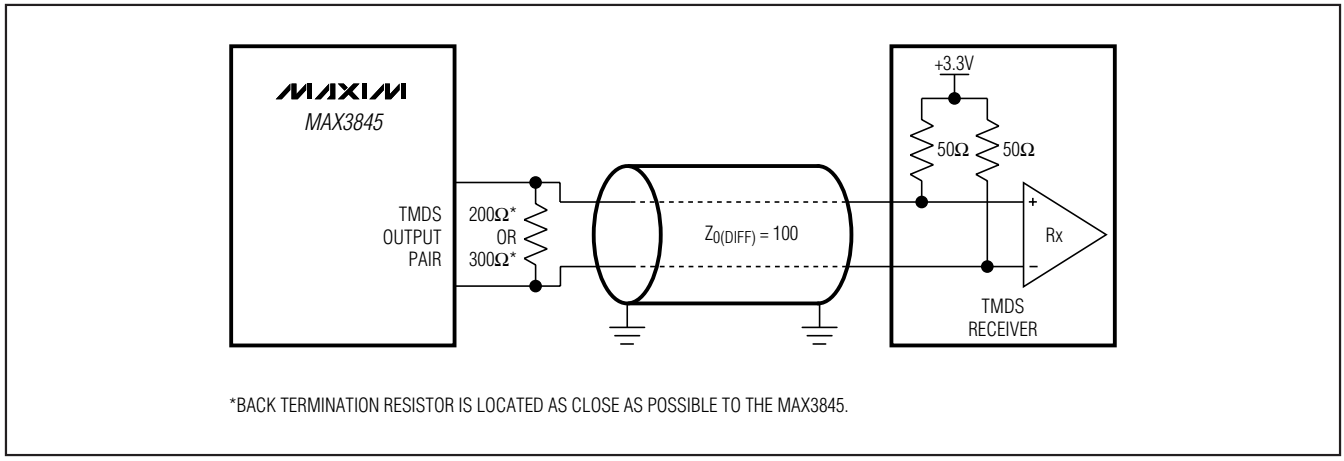


Figure 2. DC-Coupled Differential Back Termination

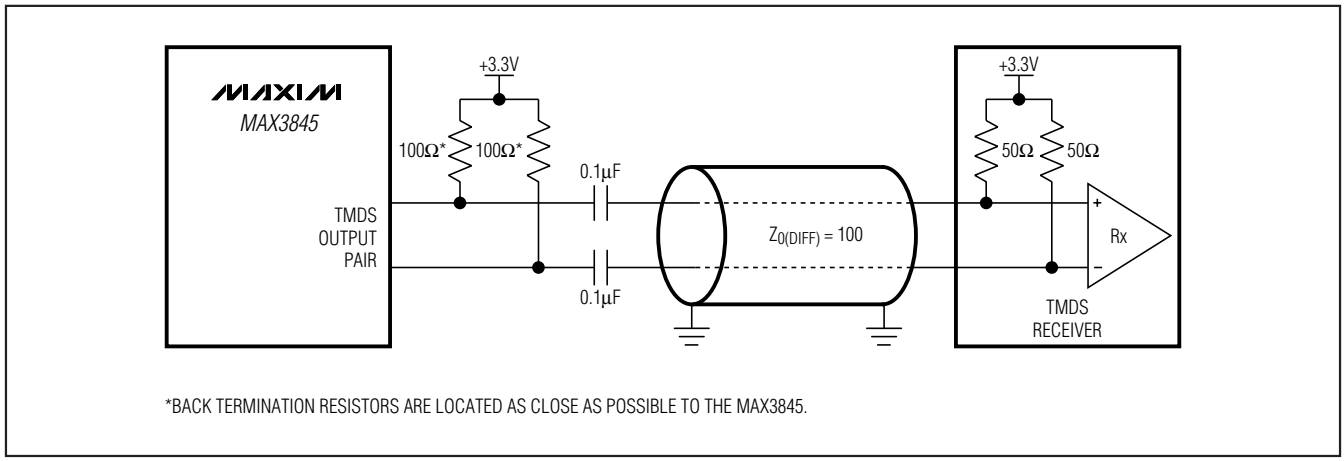


Figure 3. AC-Coupled Single-Ended Back Termination

Back termination greatly reduces signal degradation caused by reflections coming off DVI/HDMI connectors and any other transmission line discontinuities. Much of the reflected energy off a DVI connector, for example, is absorbed by the back termination resistance rather than reflected forward, causing eye closure. For the cases shown in Figures 2 and 3, the return loss is approximately 9.5dB. In other words, about 90% of the reflected energy is absorbed by the back termination resistors. Maxim strongly recommends using back termination to maximize the MAX3845's performance.

The differential back termination options reduce the common-mode output voltage seen by the TMDS receiver to approximately V_{CC} - 350mV (Table 1).

The single-ended back termination option allows for AC-coupling between the MAX3845 and a TMDS receiver, so long as the TMDS receiver is tolerant of an input common-mode voltage equal to V_{CC} (HDMI 1.2 or later).

Table 1. Output Levels With and Without Back Termination

CONDITIONS	VOLTAGES AT THE INPUT OF THE TMDS RECEIVER (TYPICAL)			
	V_{DIFF}	V_{CM}	V_H	V_L
PREEMPHx = LOW, OUT_LEVEL = LOW (Output Drive Current = 11mA)				
No back termination	$1100mV_{P-P}$	V_{CC} - 275mV	V_{CC}	V_{CC} - 550mV
PREEMPHx = LOW, OUT_LEVEL = HIGH (Output Drive Current = 14mA)				
Differential 200Ω back terminations (DC-coupled)	$950mV_{P-P}$	V_{CC} - 350mV	V_{CC} - 120mV	V_{CC} - 585mV
Differential 300Ω back terminations (DC-coupled)	$1050mV_{P-P}$	V_{CC} - 350mV	V_{CC} - 90mV	V_{CC} - 615mV
Single-ended, 2x 100Ω back terminations (AC-coupled)	$950mV_{P-P}$	V_{CC}	V_{CC} + 240mV	V_{CC} - 240mV

Temperature Sense

Pin 14, TEMP, allows the on-die temperature to be sensed as an analog voltage output. To sense the die temperature, measure the DC voltage at TEMP. The approximate die temperature can be determined using the following equation:

$$T_J = (V_{TEMP} - 0.93) \times 297$$

Also see the *Typical Operating Characteristics* section for more information.

Power-Down

The power-down inputs (PWRDWN_1 and PWRDWN_2) reduce power consumption by powering down the chosen input and all outputs that are selected to that input. For example, when output channels 1 and 4 are selected to transmit input channel 2, and channel 2 is powered down, both outputs 1 and 4 are also powered down.

Hotplug Detect

Each output channel has a HOTPLUGx detection pin associated with it. This pin is designed to detect whether a monitor's hotplug connection is attached. If HOTPLUGx is low (less than 1.5V), the associated output is powered down. If HOTPLUGx is higher than V_{CC} - 0.2V, up to 5.5V, the associated output is powered down.

Activating an Output

Several things must occur for an output to be active. Table 2 lists the required inputs to enable an output.

Cable Selection

Good quality cable is recommended for good performance. Deterministic jitter (DJ) can be caused by differential-to-common-mode conversion (or vice versa) within a twisted pair (STP or UTP), usually a result of cable twist or dielectric imbalance. Refer to Application Note *HFAN-4.5.4: 'Jitter Happens' when a Twisted Pair is Unbalanced* for more information.

Table 2. Output Enable Requirements

OUTPUT x STATE	IN_SELx CONDITION	HOTPLUGx CONDITION	PWRDWN_1 CONDITION	PWRDWN_2 CONDITION	LOS 1 CONDITION	LOS 2 CONDITION
INPUT 1	HIGH	HIGH	LOW	Don't care	LOW	Don't care
INPUT 2	LOW	HIGH	Don't care	LOW	Don't care	LOW

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

Interface Models

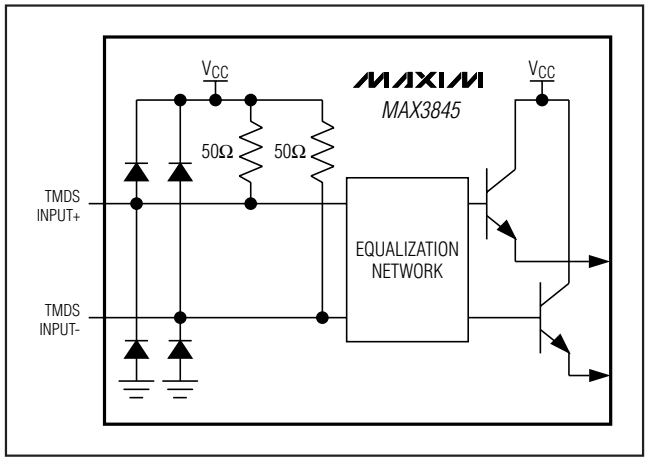


Figure 4. Simplified Input Circuit Schematic

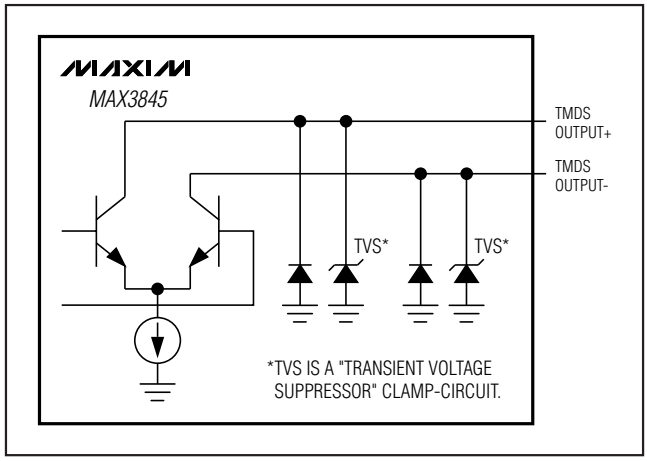


Figure 5. Simplified Output Circuit Schematic

Layout Considerations

The data inputs and outputs are the MAX3845's most critical paths, and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the MAX3845:

- Maintain 100Ω differential transmission line impedance into and out of the MAX3845.
- The data and clock inputs should be wired directly between the cable connector and IC without stubs.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground path vias should be placed close to the IC and the input/output interfaces to allow a return current path to the IC and the DVI/HDMI cable.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

For more information, refer to the schematic and board layers of the Maxim evaluation kit, *MAX3845EVKIT*.

Exposed-Pad Package and Thermal Considerations

The exposed pad on the 100-pin TQFP-EP provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3845 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Because the MAX3845 is a high-power device, it is important to ensure that good heat dissipation is incorporated into the PCB design. The device's temperature-sense pin (TEMP) allows estimation of the junction temperature to be made while the MAX3845 is operating. This information can be used to determine if the PCB layout is dissipating heat properly.

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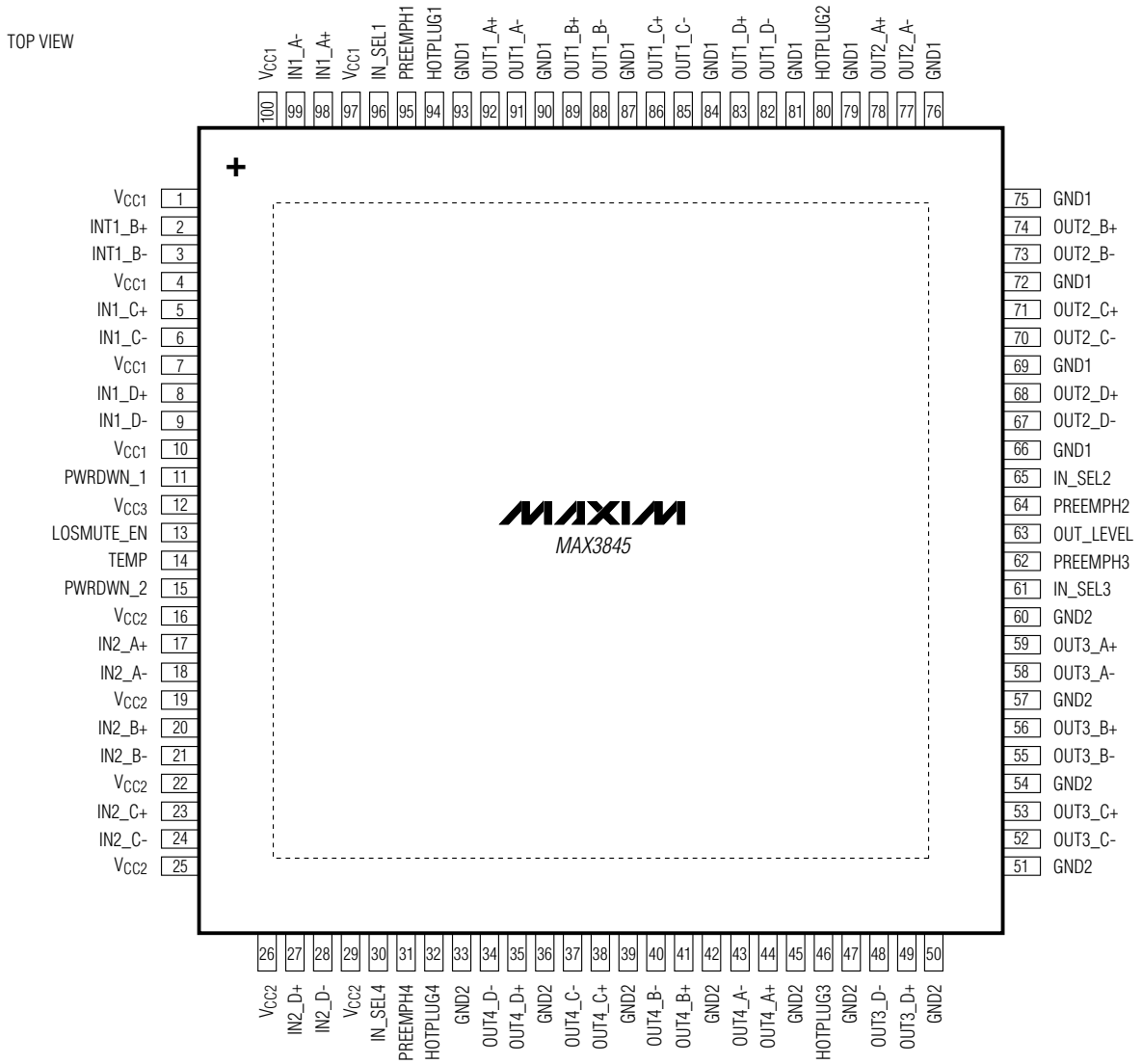
Pin Configuration

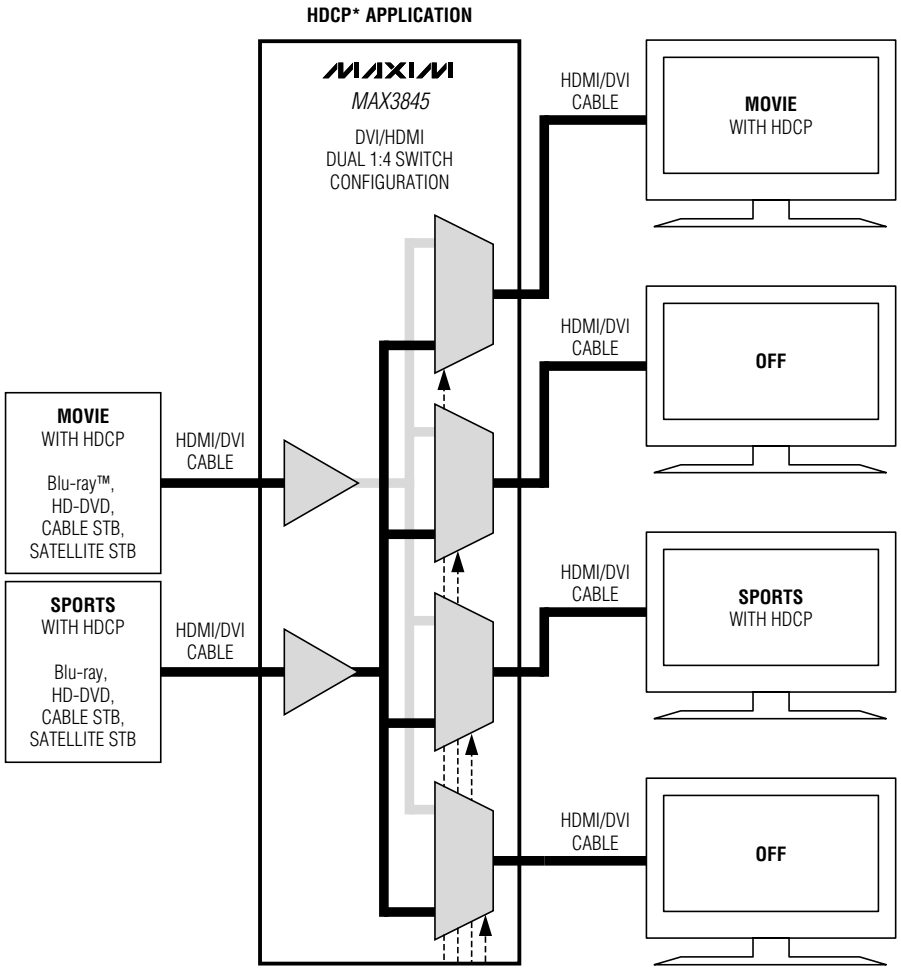


TQFP-EP*

*EXPOSED PAD MUST BE CONNECTED TO GROUND.

DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

Typical Operating Circuits (continued)



* BECAUSE THE MAX3845 IS A TRANSPARENT SWITCH, HDCP SOURCES CAN ONLY BE CONNECTED TO ONE HDCP-COMPLIANT DISPLAY AT A TIME AND CANNOT BE FANNED OUT THROUGH THE MAX3845.

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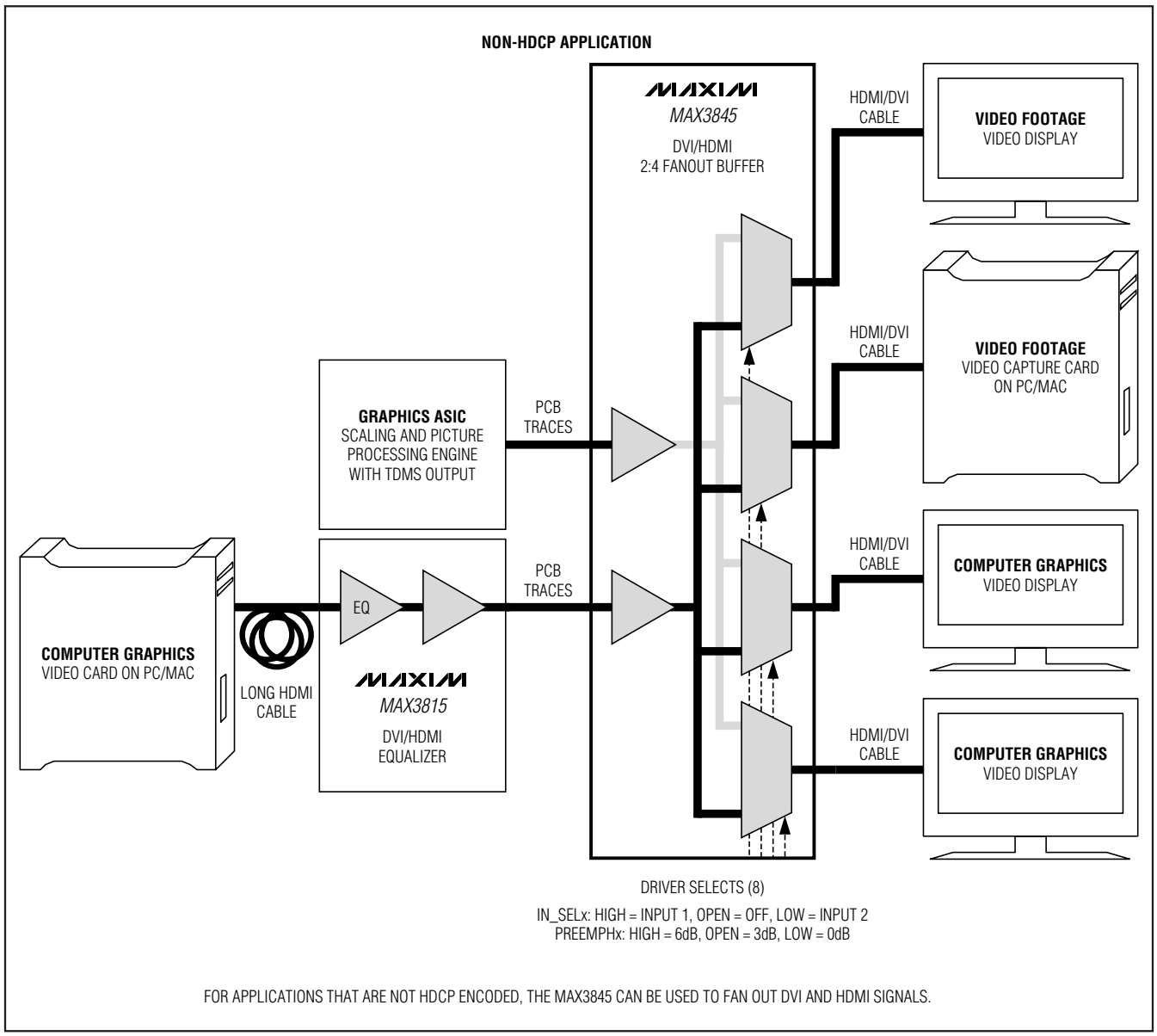
DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

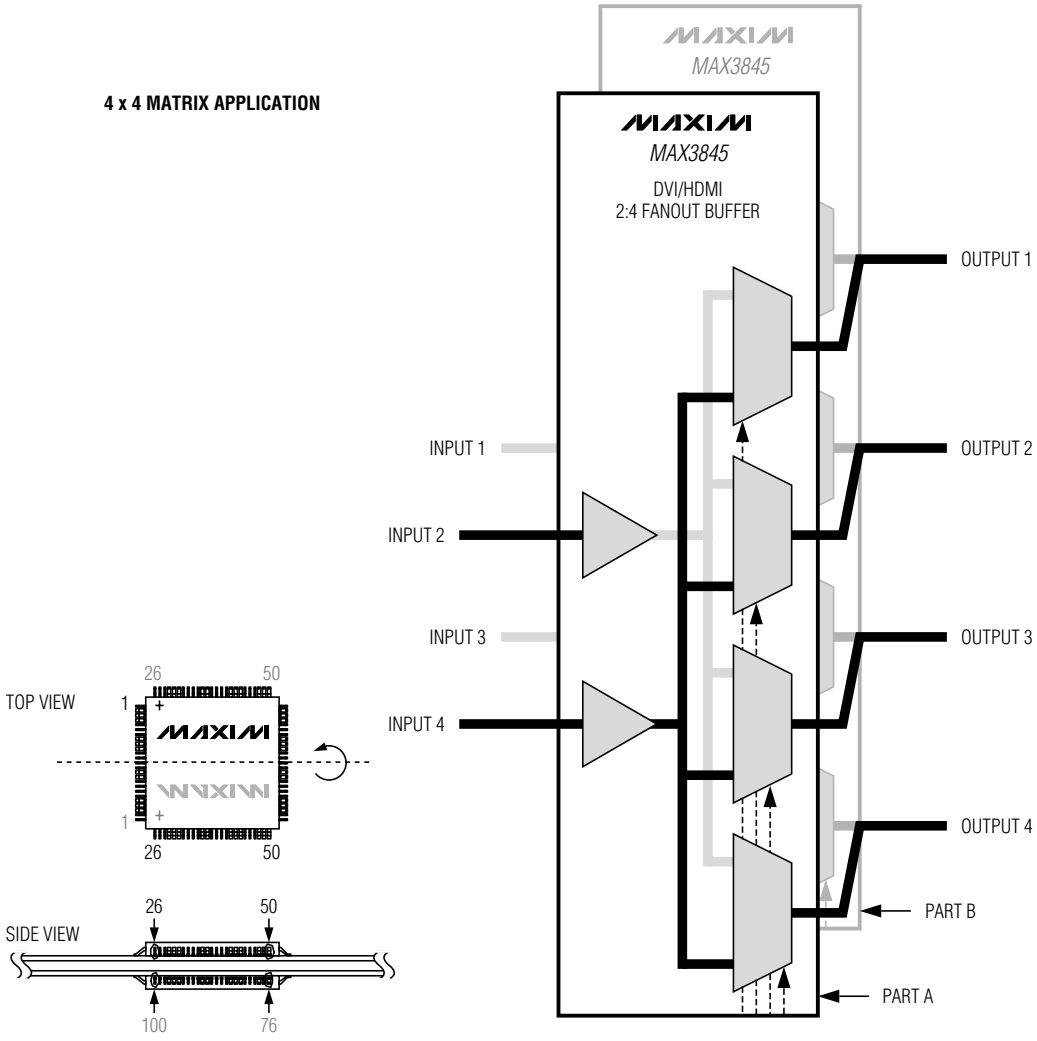
Typical Operating Circuits (continued)



DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

Typical Operating Circuits (continued)

4 x 4 MATRIX APPLICATION

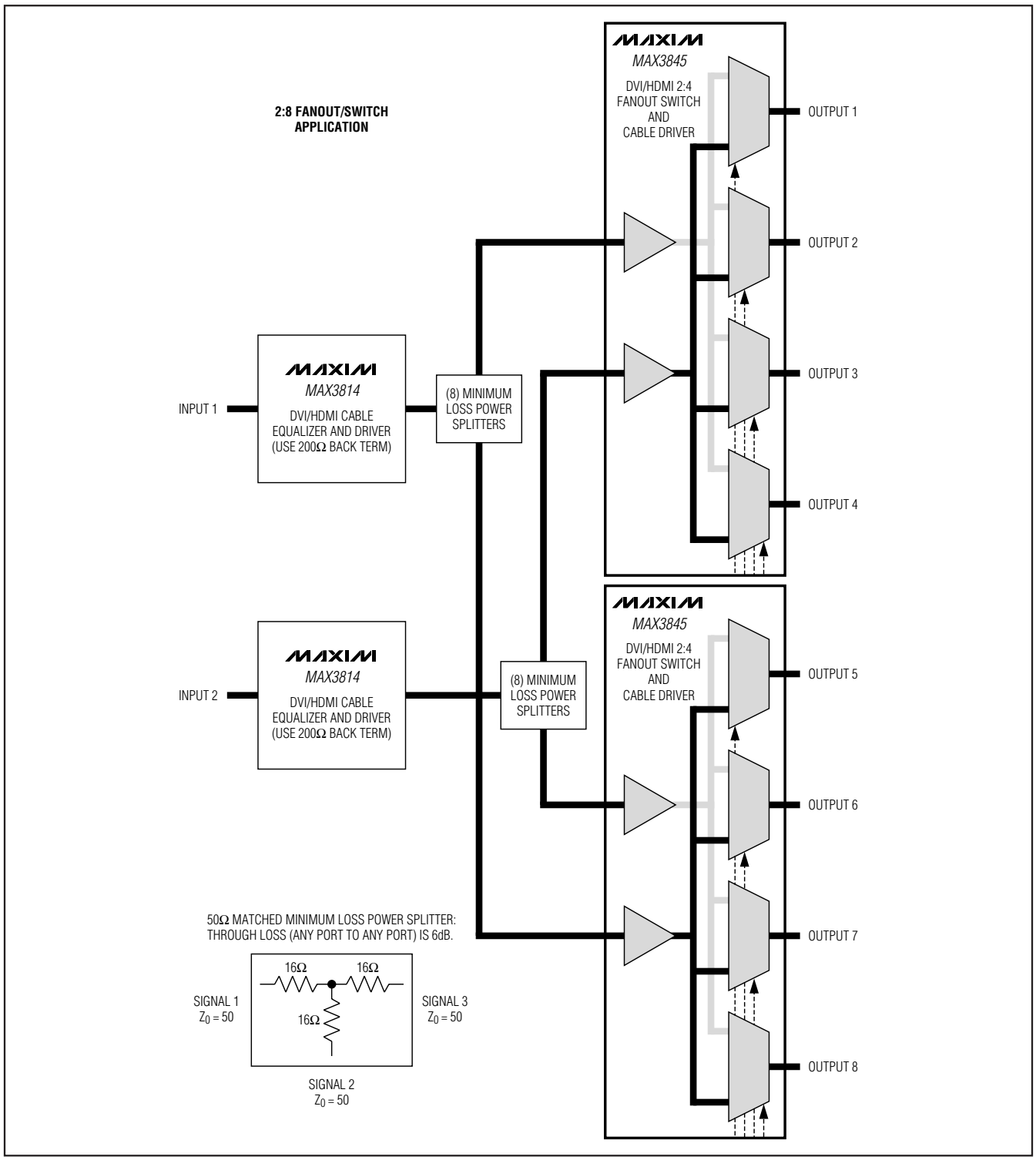


DRIVER SELECTS 2x(8)

IN_SELx (PART A): HIGH = INPUT 2, OPEN = OFF, LOW = INPUT 4
IN_SELx (PART B): HIGH = INPUT 1, OPEN = OFF, LOW = INPUT 3
PREEMPHx: HIGH = 6dB, OPEN = 3dB, LOW = 0dB

FOR 4 x 4 MATRIX OPERATION, TWO MAX3845 PARTS ARE LOCATED ON EITHER SIDE OF THE BOARD WITH THE AXIS OF ROTATION ABOUT PINS 13 AND 63.

Typical Operating Circuits (continued)

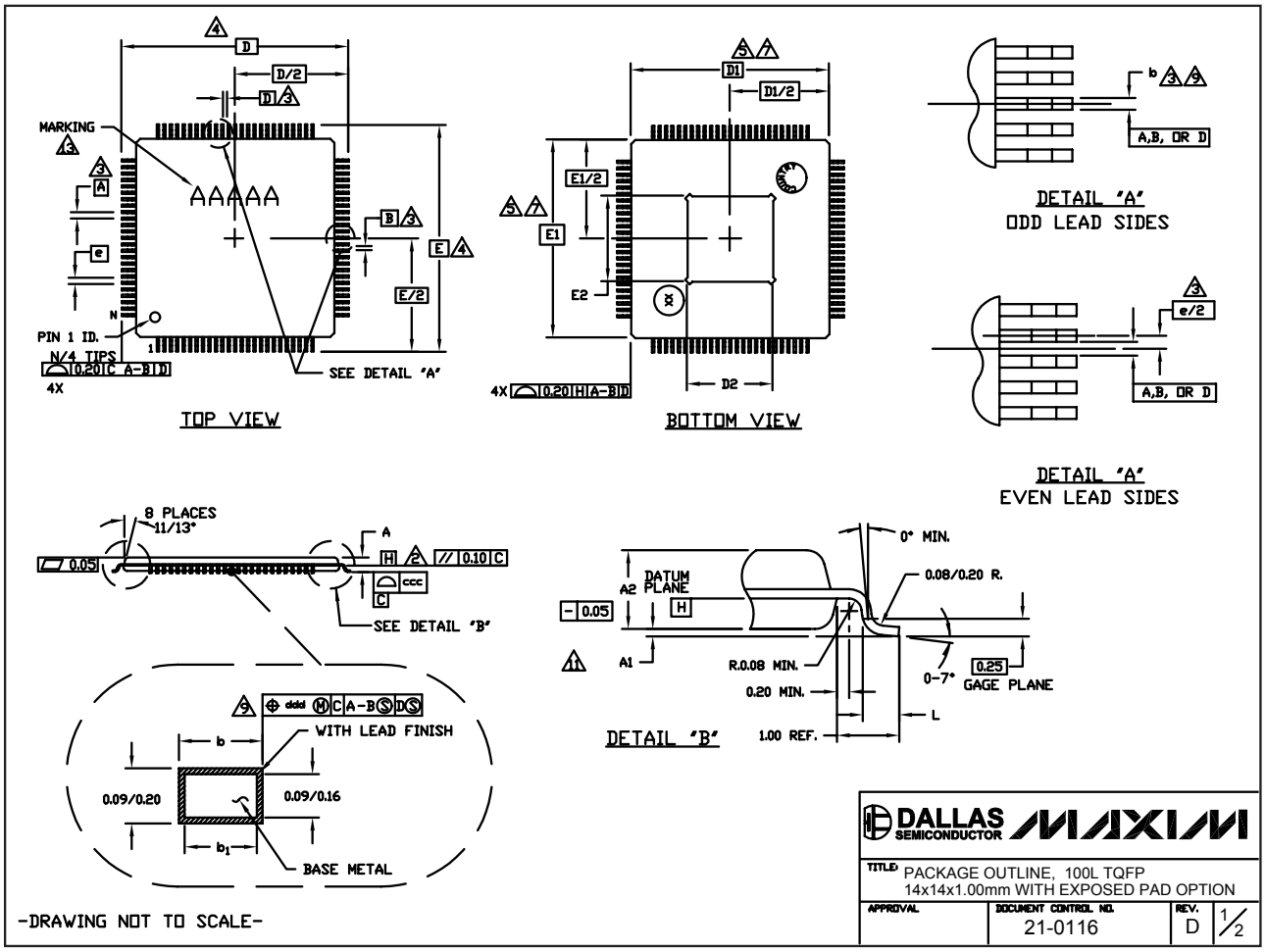


DVI/HDMI 2:4 TMDS Fanout Switch and Cable Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

14x14x1.00L TQPF, EXP. PAD.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SYMBOL	ALL DIMENSIONS ARE IN MILLIMETERS			
	MIN.	NOM.	MAX.	NOTES
A	~	~	1.20	
A_1	0.05	~	0.15	11
A_2	0.95	1.00	1.05	
D		16.00 BSC.		4
D_1		14.00 BSC.		7,8
E		16.00 BSC.		4
E_1		14.00 BSC.		7,8
L	0.45	0.60	0.75	
N		100		
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	~	~	0.08	
ddd	~	~	0.08	

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG. CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C100E-2	7.7	8.0	8.3	7.7	8.0	8.3
C100E-3	6.2	6.5	6.8	6.2	6.5	6.8
C100E-6	4.7	5.0	5.3	4.7	5.0	5.3
C100E-11	3.3	3.6	3.9	5.5	5.8	5.9

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. DATUM PLANE [H] LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUM [A–B] AND [D] TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXITS PLASTIC BODY AT DATUM PLANE [H].
4. TO BE DETERMINED AT SEATING PLANE [C].
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254mm ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [H].
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
9. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. THIS OUTLINE CONFROMS TO JEDEC MS-026.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
12. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05mm.
13. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 100L TQFP
14x14x1.00mm WITH EXPOSED PAD OPTION

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