19-2713; Rev 1; 11/03

EVALUATION KIT AVAILABLE

12.5Gbps Settable Receive Equalizer

General Description

The MAX3804 driver with integrated analog equalizer compensates up to 20dB of loss at 5GHz. It is designed to ensure PC board signal integrity up to 12.5Gbps, where frequency-dependent skin effect and dielectric losses typically produce unacceptable amounts of intersymbol interference. The MAX3804 can extend the practical chip-to-chip transmission distance for 10Gbps NRZ serial data up to 30in (0.75m) on FR-4, and it significantly decreases deterministic jitter. Residual jitter after equalization for 10.7Gbps signals is typically 24ps$_{P-P}$ on the maximum path length.

The MAX3804 is ideal for 10Gbps chip-to-chip serial interconnections on inexpensive FR-4 material. Its 3mm × 3mm package affords optimal placement and routing flexibility. It has separate V_{CC} connections for internal logic and current-mode logic (CML) I/O. This allows the CML input and output to be referenced to isolated supplies, providing independent DC-coupled interfacing to 1.8V, 2.5V, or 3.3V ICs. Eight discrete levels of input equalization can be selected through a digital control input, enabling the equalizer to be matched to a range of transmission line path loss. When correctly set to match the path loss, the MAX3804 provides optimal performance over a wide range of data rates and formats.

Applications

OC-192 and 10Gb Ethernet Switches and Routers

OC-192 and 10Gb Ethernet Serial Modules

High-Speed Signal Distribution

Features

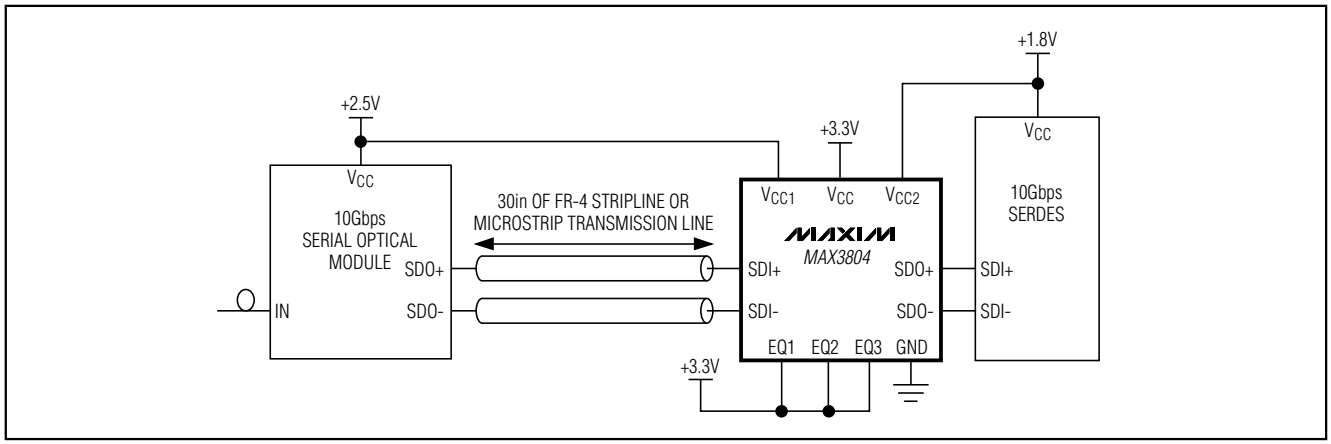
- **Compensates Up to 30in (0.75m) of 6-mil FR-4 Transmission Line Loss**
- **115mW Operating Power**
- **Up to 12.5Gbps Data Rate**
- **Compatible with 8B10B, 64B66B, and PRBS Data**
- **Less than 30ps$_{P-P}$ Residual Jitter After Equalization**
- **3-Bit Equalization Level Select Input**
- **3mm x 3mm Thin QFN Package**
- **DC-Coupling to 1.8V, 2.5V, or 3.3V CML I/O**
- **-40°C to +85°C Operation**
- **+3.3V Core Supply Voltage**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3804ETE	-40°C to +85°C	16 Thin QFN (3mm x 3mm)	T1633F-3

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

12.5Gbps Settable Receive Equalizer

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....-0.5V to +4.0V
CML Supply Voltage (V_{CC1}, V_{CC2}) .....-0.5V to (V_{CC} + 0.5V)
Current at Serial Output (SDO+, SDO-) .....±25mA
Input Voltage (SDI+, SDI-, EQ1, EQ2, EQ3) .....-0.5V to (V_{CC} + 0.5V)

Continuous Power Dissipation (T_A = +85°C)
16-Lead Thin QFN-EP (derate 17.5mW/°C above +85°C) 1398mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, V_{CC1} = V_{CC2} = +1.65V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = V_{CC1} = V_{CC2} = +3.3V, and T_A = +25°C, unless otherwise noted.)

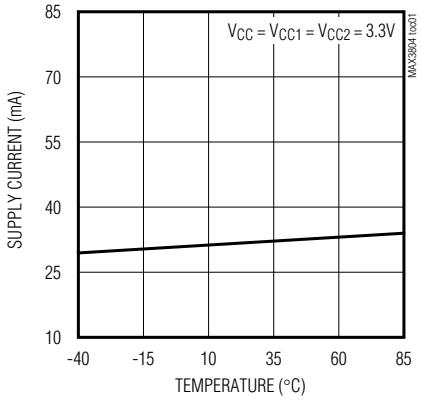
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			35	50	mA
CML Input Differential	V_{IN}	AC-coupled or DC-coupled (Note 1)	400		1200	mV_{P-P}
CML Input Common Mode		DC-coupled	V_{CC1} - 0.4		V_{CC1} + 0.1	V
CML Input Termination		Single ended	42.5	50	57.5	Ω
CML Input Return Loss		Up to 5GHz		10		dB
CML Output Differential	V_{OUT}		400	500	600	mV_{P-P}
CML Output Impedance		Single ended	42.5	50	57.5	Ω
CML Output Transition Time	t_R, t_F	20% to 80% (Notes 2, 6)			35	ps
Residual Jitter Output (Total RJ, PWD, and PDJ)		At 10.7Gbps (Notes 3, 4, 5, 6)		24	30	ps_{P-P}
		At 12.5Gbps (Notes 3, 4, 5, 6)		17	30	
LVTTL Input Current	I_{IH}, I_{IL}		-30		+30	µA
LVTTL Input Low	V_{IL}				0.8	V
LVTTL Input High	V_{IH}		2.0			V

Note 1: Differential Input Sensitivity is defined at the input to a transmission line. The transmission line is differential Z_0 = 100Ω, 6-mil microstrip in FR-4, ε_r = 4.5, and tan δ = 0.02, V_{IN} = (SDI+ - SDI-).
Note 2: Measured with 0000011111 pattern at 12.5Gbps.
Note 3: Residual jitter is the difference in total jitter (RJ, PWD, and PDJ) between the transmitted signal (at the input to the transmission line) and equalizer output. Total residual jitter is DJ_{P-P} + 14.2 x RJ_{RMS}.
Note 4: Measured at 10.7Gbps using a pattern of 100 ones, 2^7PRBS, 100 zeros, 2^7PRBS, and at 12.5Gbps using a K28.5 pattern. Deterministic jitter at the input is from frequency-dependent, media-induced loss only.
Note 5: V_{IN} = 400mV_{P-P} to 1200mV_{P-P}, input path is 0 to 30in, 6-mil microstrip in FR-4, ε_r = 4.5, and tan δ = 0.02.
Note 6: Guaranteed by design and characterization.

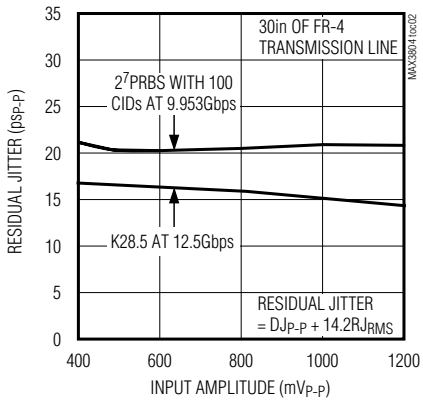
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

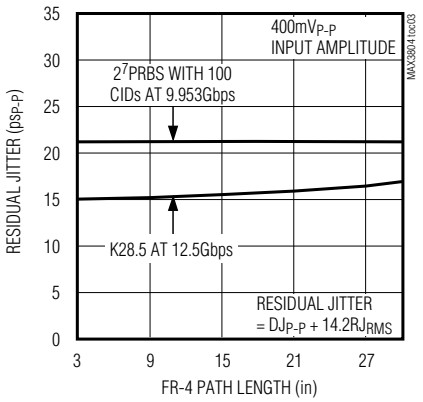
SUPPLY CURRENT vs. TEMPERATURE



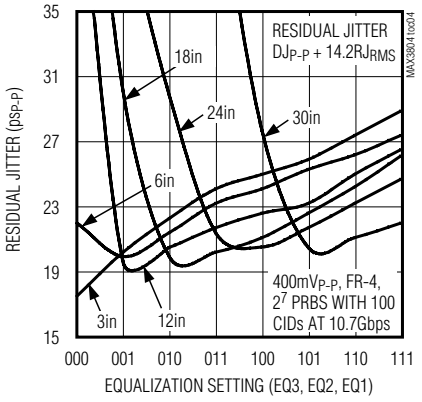
RESIDUAL JITTER vs. INPUT AMPLITUDE



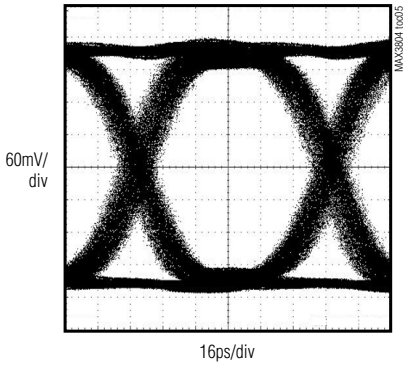
RESIDUAL JITTER vs. FR-4 PATH LENGTH



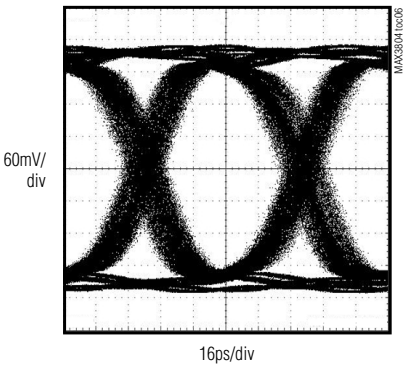
RESIDUAL JITTER vs. EQUALIZATION SETTING



EQUALIZER OUTPUT EYE AFTER 18in OF FR-4 (2^7PRBS WITH 100 CIDs AT 10.7Gbps)



EQUALIZER OUTPUT EYE AFTER 18in OF FR-4 (K28.5 AT 12.5Gbps)

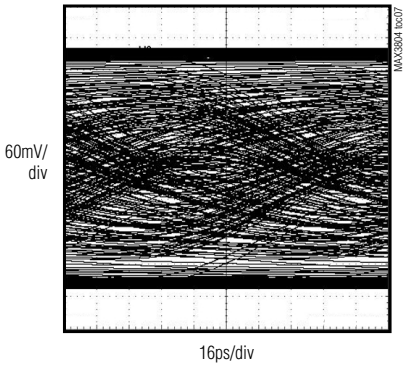


12.5Gbps Settable Receive Equalizer

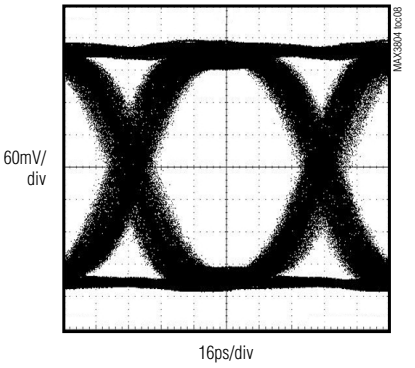
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

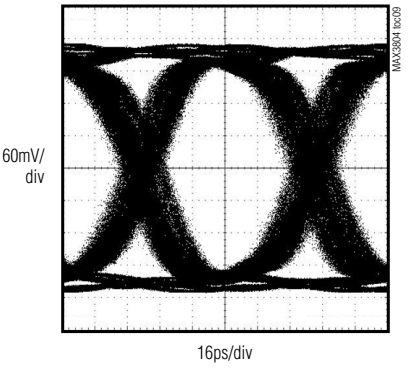
EQUALIZER INPUT EYE AFTER 30in OF FR-4 (2^7PRBS WITH 100 CIDs AT 10.7Gbps)



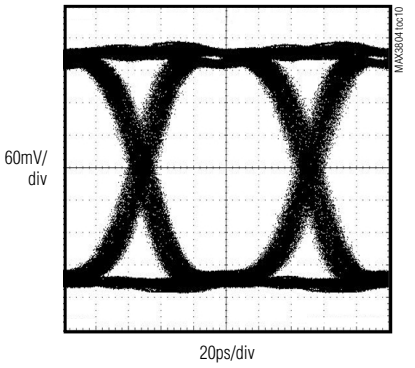
EQUALIZER OUTPUT EYE AFTER 30in OF FR-4 (2^7PRBS WITH 100 CIDs AT 10.7Gbps)



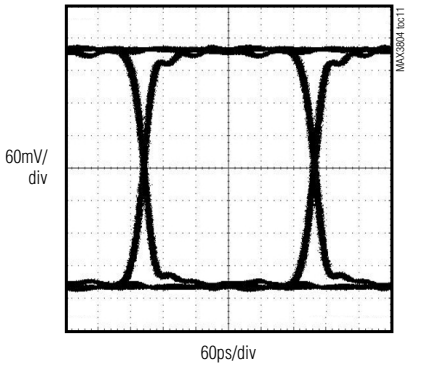
EQUALIZER OUTPUT EYE AFTER 30in OF FR-4 (K28.5 AT 12.5Gbps)



EQUALIZER OUTPUT EYE AFTER 24ft OF RG-188/U COAXIAL CABLE, SINGLE ENDED (2^7PRBS WITH 100 CIDs, 9.953Gbps)



EQUALIZER OUTPUT EYE AFTER 30in OF FR-4 (2^7PRBS WITH 100 CIDs AT 3.2Gbps)



Pin Description

PIN	NAME	FUNCTION
1, 4	V_{CC1}	CML Input Supply Voltage. Connect to +1.8V to +3.3V for DC-coupled CML. Input can also be AC-coupled.
2	SDI+	Positive Serial Data Input, CML
3	SDI-	Negative Serial Data Input, CML
5	EQ1	Equalizer Boost Control Logic Input LSB, LVTTL. See Table 1.
6	EQ2	Equalizer Boost Control Logic Input, LVTTL. See Table 1.
7	EQ3	Equalizer Boost Control Logic Input MSB, LVTTL. See Table 1.
8, 16	GND	Supply Ground
9, 12	V_{CC2}	CML Output Supply Voltage. Connect to +1.8V to +3.3V for DC-coupled CML. Output can also be AC-coupled.
10	SDO-	Negative Serial Data Output, CML
11	SDO+	Positive Serial Data Output, CML
13, 14	N.C.	No Connection. Leave unconnected.
15	V_{CC}	+3.3V Core Supply Voltage
EP	Exposed Pad	Ground. Must be soldered to the circuit board ground for proper thermal and electrical performance (see the *Package and Layout Considerations* section).

Detailed Description

General Theory of Operation

The MAX3804's low-noise linear input stage includes two amplifiers, one with flat-frequency response, and one with response that compensates for the loss characteristic of an FR-4 PC board transmission line. A current-steering network allows the designer to control the amount of equalization to match the path loss for specific applications. This network consists of a pair of variable attenuators feeding into a summing node. Equalization is set by a 3-bit LVTTL-compatible input (EQ3, EQ2, and EQ1). By employing fixed control of the equalization level, the MAX3804 provides optimal performance for a specific path loss. A high-speed limiting amplifier follows the equalizer circuitry to shape the output signal (see Figure 1).

CML Input and Output Buffers

The MAX3804 input and output CML buffers are terminated with 50Ω to V_{CC1} and V_{CC2}, respectively. The equivalent circuit for the output is shown in Figure 2. Separate supply voltage connections are provided for the core (V_{CC}), input (V_{CC1}), and output (V_{CC2}) circuitry to control noise coupling, and to allow DC-coupling to +1.8V, +2.5V, or +3.3V CML ICs. The CML inputs and outputs can also be AC-coupled.

Use AC-coupling for single-ended cable applications. The unused CML input must be connected through an AC-coupling capacitor to a 50Ω termination.

The low-frequency cutoff of the input-stage offset-cancellation circuit is nominally 21kHz.

12.5Gbps Settable Receive Equalizer

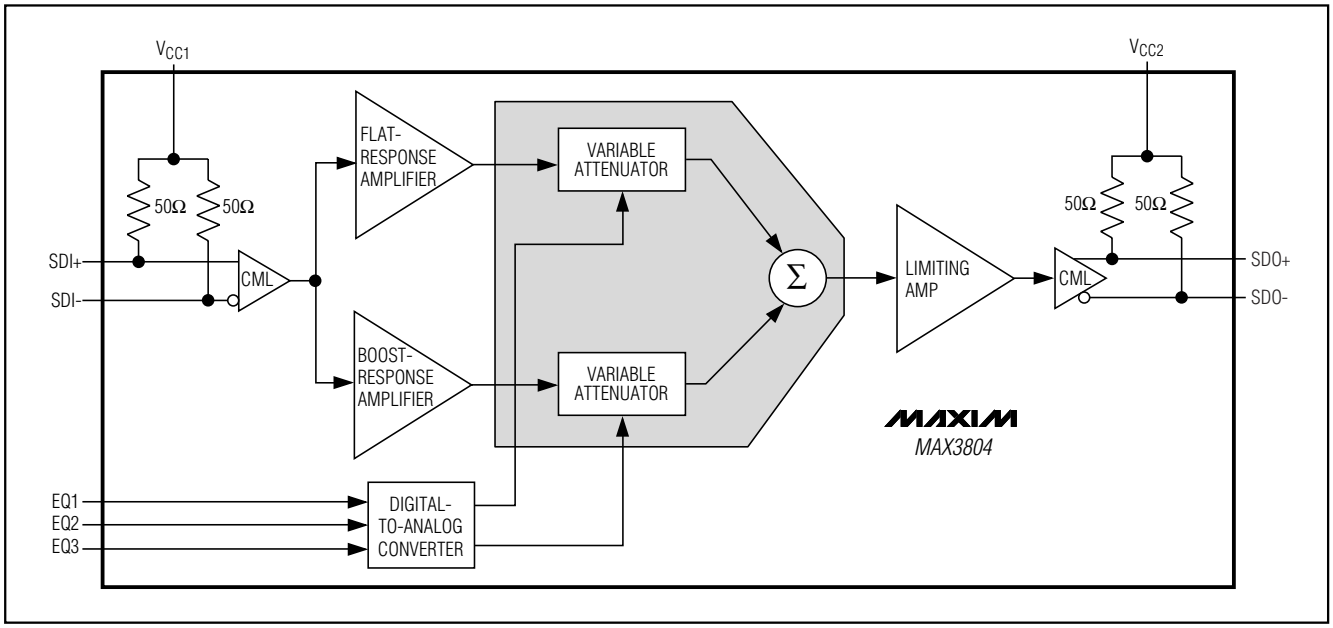


Figure 1. Functional Diagram

Applications Information

Equalizer Boost Level Control

The MAX3804 equalizer is intended for use at the receive end of an FR-4 PC board transmission line, typically up to 30in of differential 6-mil stripline or microstrip. It is specifically designed to mitigate intersymbol interference caused by the frequency-dependent path loss of FR-4 transmission lines. It can also be used with a variety of other transmission-line materials and geometries, including coaxial cable, or PC board paths that include well-engineered connectors. Table 1 shows the relationship between nominal 6-mil FR-4 transmission line length and equalization setting.

Supply Voltage Connections

The CML input and output supplies (V_{CC1}, V_{CC2}) can be connected to +1.8V to +3.3V. V_{CC1} and V_{CC2} need not be connected to the same supply voltage; however, the core supply (V_{CC}) must be connected to +3.3V.

Package and Layout Considerations

The MAX3804 is packaged in a 3mm x 3mm plastic-encapsulated 16-lead thin QFN package. The package has an exposed pad that provides thermal and electrical connectivity to the IC and must be soldered to a high-frequency ground. Use good layout techniques for the SDI± and SDO± PC board transmission lines, and configure the trace geometry near the IC package to minimize impedance discontinuities. Power-supply decoupling capacitors should be as close as possible to the IC.

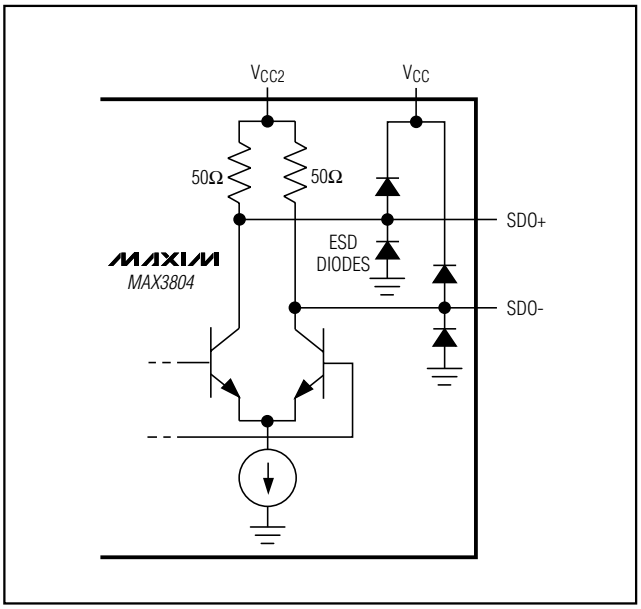
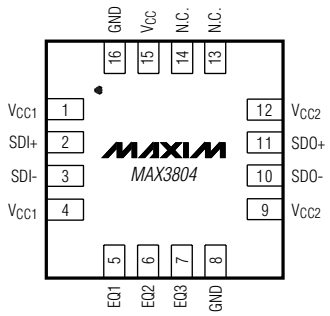


Figure 2. Simplified Output Structure

Table 1. Nominal 6-mil FR-4 Transmission Line Length and Equalization Settings

EQ3	EQ2	EQ1	NOMINAL 6-mil FR-4 MICROSTRIP LENGTH (in)
0	0	0	2
0	0	1	6
0	1	0	10
0	1	1	14
1	0	0	18
1	0	1	22
1	1	0	26
1	1	1	30

Pin Configuration



Thin QFN*
(3mm x 3mm)

*THE EXPOSED PAD MUST BE CONNECTED TO CIRCUIT BOARD GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

Chip Information

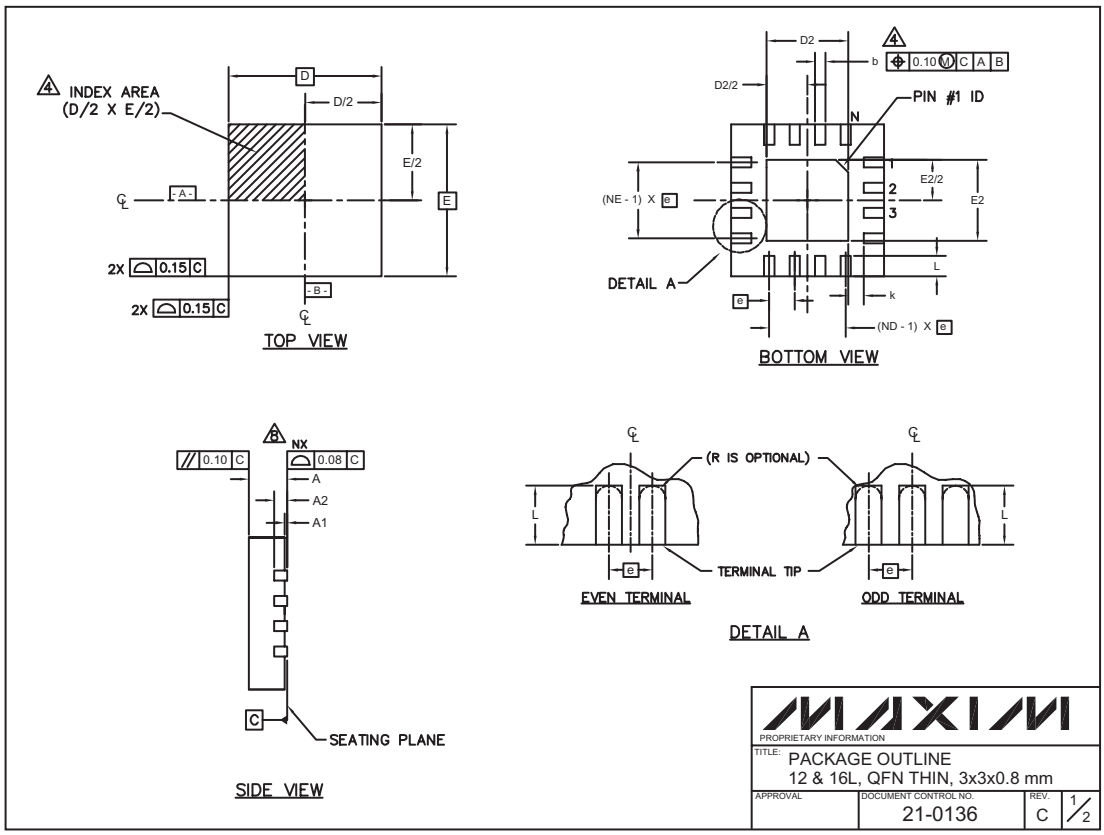
TRANSISTOR COUNT: 1007

PROCESS: SiGe bipolar

12.5Gbps Settable Receive Equalizer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	-

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 12 & 16L, QFN THIN, 3x3x0.8 mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. C	2/2