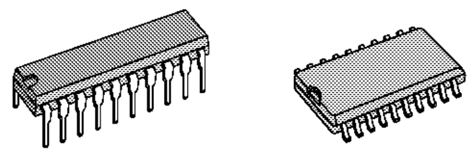
SGS-THOMSON MICROELECTRONICS

TEA7063

SPEECH CIRCUIT WITH POWER MANAGEMENT

PRELIMINARY DATA

- 2/4 WIRES INTERFACE WITH
  - double antisidetone network
  - AC impedance externally programmable
  - Rx output dynamic programmable
  - AGC attack-disconnect points programmable
- ANTI-CLIPPING/ANTI DISTORTION CIRCUIT PROGRAMMABLE
- DTMF INTERFACE
- 3.3 VOLTS SUPPLY FOR MICROPROCESSOR OR DIALER
- EXTRA CURRENT SUPPLY PROGRAMMABLE FOR LOUD SPEAKER
- DC CHARACTERISTIC PROGRAMMABLE FOR ALL SPECIFICATION
- LOW CURRENT OPERATION



DIP20 **SO20**

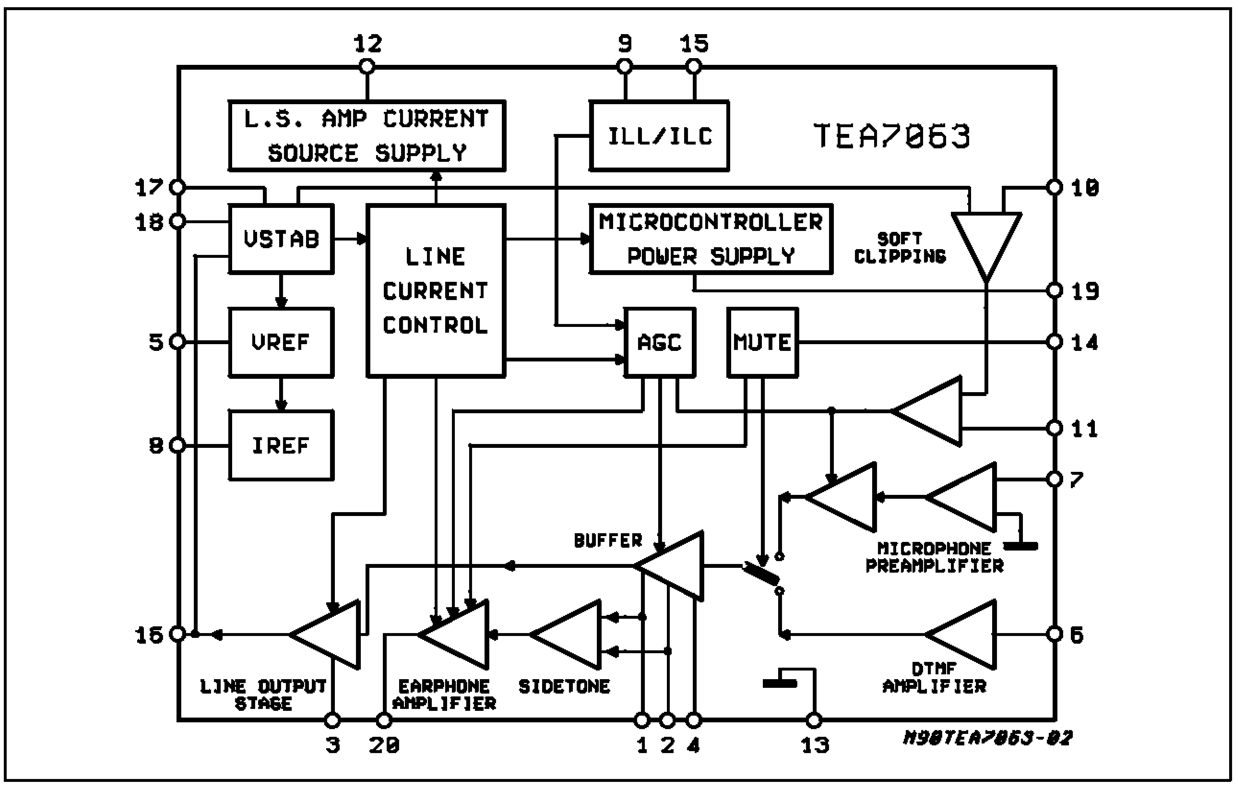
ORDERING NUMBERS:

TEA7063FP TEA7063DP

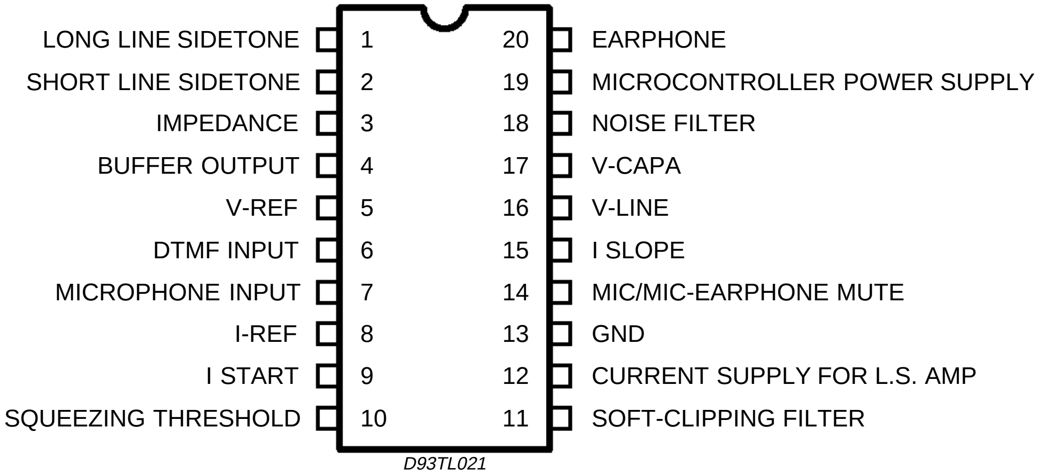
DESCRIPTION

The TEA7063 is designed to meet the different worldwide specifications for telephone set in medium and high range equipments.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



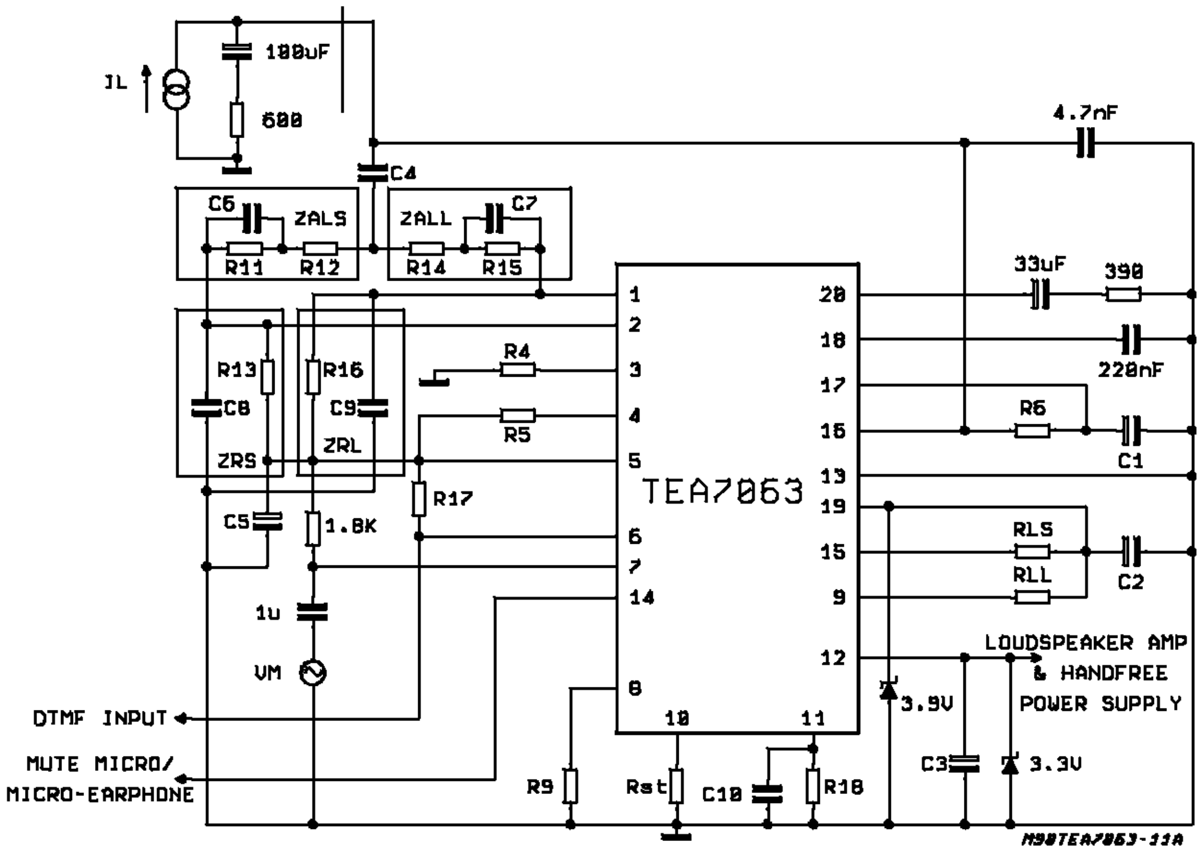
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Max. Current DC (steady)	150	mA
	Max. Voltage AC (steady)	7.5	V
	Max. Voltage AC + DC (steady)	9	V
	Max. Current (20ms) ONE SHOT	1	A
	Max. Voltage (20ms) ONE SHOT current < 1A	12	V
P_{tot}	Total Power Dissipation	1	W
T_J	Junction Temperature	130	°C

MAXIMUM OPERATING CONDITION

Symbol	Parameter	Value	Unit
V_{DC}	DC Voltage	7	V
V_{AC}	AC Voltage	2.2	Vp
I_{DC}	DC Current	110	mA
T_{OP}	Temperature Range	-20 to 70	°C

TEST CIRCUIT



R4 = 75	R13 = 2.7K	C1 = 47µF	C7 = 47pF	RLL = 150K
R5 = 5.1K	R14 = 0	C2 = 4.7µF	C8 = 2.2nF	RLS = 100K
R6 = 22K	R15 = 140K	C3 = 47µF	C9 = 2.2nF	RST = 330K
R9 = 100K	R16 = 2.7K	C4 = 470nF	C10 = 150nF	
R11 = 140K	R17 = 1.8K	C5 = 100µF		
R12 = 0	R18 = 560K	C6 = 47pF		

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ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; f = 1KHz; R9 = 100KΩ; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_C	Stabilized Voltage (pin 17)	I_L = 25mA; R9 = 100KΩ	2.25	2.5	2.75	V
Iint	Internal Bias Current (pin 17)	I_L = 25mA I_L = 25mA; R9 = 180K (V16 - R6*Iint +V_C)	120	140 105	160	µA µA
V_{ref}	Reference Voltage	I_L = 25mA	1.05	1.2	1.35	V
I_{ref}	Current at V_{ref}		-100		+10	µA
V_{mp}	Stabilized Supply at pin 19		3.1	3.3	3.5	V
I_{cmp}	Charging Current at Pin 19	Pin 17 = GND	0.6 X I_{line}			mA
I_{spm}	Static Current at Pin 19	I_L = 25mA; R9 = 100KΩ	1.1	1.5		mA
		I_L = 25mA; R9 = 180KΩ		0.85		mA
I_{imp}	Internal Consumption		80	110	150	µA
I_{ea}	Supply Current for Parallel Circuits (pin 12)	I_L = 25mA I_L = 75mA	10 50	12 57		mA mA
V_{mh} V_{mb}	Mute Microphone (pin 14)	ON OFF	1.6 0.25		 0.8	V V
V_{mh} V_{mb}	Mute Earphone (pin 14)	ON OFF	2.7 0.25		 2.1	V V
I_{mleak}	Mute Leakage Current (pin 14)	V_{14} = 5V			20	µA
G_S AGC_S	Tx Gain Long Line	I_L = 25mA	41.5 -7	42.5 -6	43.5 -5	dB dB
G_mf	DTMF Gain	Pin 14 > 1.6V	41.5	42.5	43.5	dB
THD_S	Tx Distortion	I_L = 25mA V_{mic} = -3dBm -GS V_{mic} = -3dBm -GS + 15dB			 3 10	 % %
Z_e	Microphone Impedance		20			KΩ
N_{Tx}	Tx Noise (psometric)	I_L = 25mA 2KΩ at Pins 5-7		-74		dBm psoph
R_S	Tx Attenuation in Mute Mode	I_L = 25mA Pin 14 > 1.6V	60			dB
G_r AGC_r	Rx Gain Long Line Line Lenght	I_L = 25mA	29 -7	30 -6	31 -5	dB dB
THD_r	Rx Distortion	I_L = 25mA Vro = 500mV Vro = 630mV			 3 10	 % %
N_{Rx}	Rx Noise	I_L = 25mA		-74		dBmp
R_r	Rx Attenuation in Mute Mode	I_L = 25mA Pin = 14 > 2.7V	50			dB
G_{as}	Antisidetone	I_L = 25mA	22			dB
Z_{ac}	AC Impedance	I_L = 25mA	500	650	800	Ω
G_{rs}	Confidence Level = V_{LINE}/V_{REC} (in DTMF)	Pin 14 > 2.7V	35.5	38.5	41.5	dB
I_{ST}	Soft Clipping Current Level Control (pin 10)	I_L = 25mA; R9 = 100KΩ I_L = 25mA; R9 = 180KΩ	2.30	2.55 1.4	2.80	mA µA
V_{ST}	Control Voltage Range (Pin 10)	$V_{ST} = R_{ST} \times I_{ST}$	0		1	V

CIRCUIT DESCRIPTION

1. DC CHARACTERISTICS

1.1 V_C (pin 17)

The stabilized voltage VC is connected to Vline (pin 16) through an internal shunt regulator T1, T2, which presents to the line a high AC impedance at frequecncies higher than 200Hz. At this purpose the value of C1 (at pin 17) must be not lower than 47µF (suggested value is 100µF).

The shunt regulator, T1 and T2, also controls the extra current source, or power management, at pin 12 (see also paragraph 6).

1.2 V_{LINE} (pin 16)

The line voltage (pin 16) is determined by the value of the external resistor R6 and by the internal current, I_{int}, flowing between V_C (pin 17) and Ground (see also paragr.: 1.1):

$V_{LINE} = V_C + R6 \times I_{int}$

V_C is fixed by design at about 2.5V.

I_{int} is reversely related to R9:

$I_{int} = 8\ Volt/R9 + 60\mu A$ at $I_L > 25mA$

$I_{int} = 4\ Volt/R9 + 60\mu A$ at $I_L = 6mA$

where I_L depends on I_{LB} (see supply management)

V_{LINE} must be externally adjusted (with R6) to guarantee both DC and AC characteristic in accordance to the specific standard of the different adminastrations.

Another adjustment of the DC characteristic is possible with R9. Increasing the value of R9 causes a decrease of I_{int} and consequently a reduction of the product I_{int} x R9. (see also Paragraph 7)

Figure 1

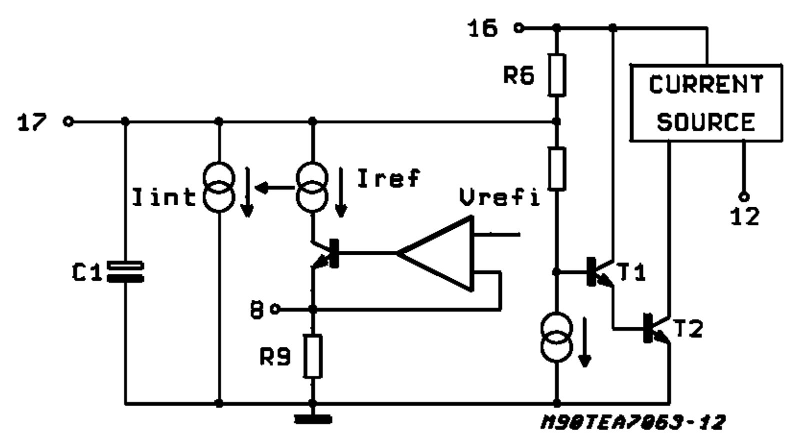
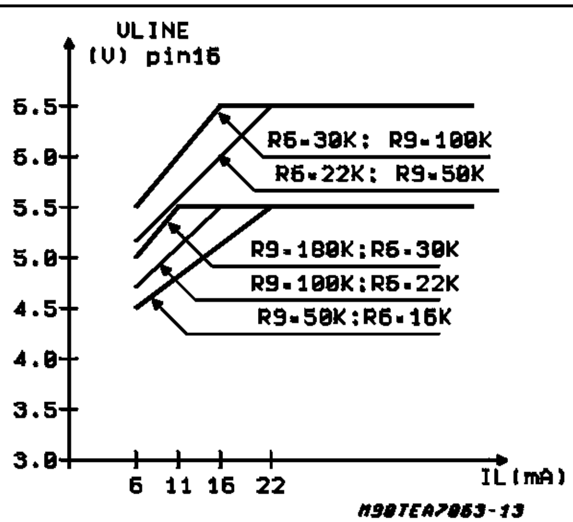


Figure 2



2. TRANSMISSION CHAIN

2.1 A.G.C. In Transmission

The transmission gain between Microphone Input (pin 7) and Vline (pin 16) is internally decreased of 6dB when the line current varies from ILL to ILS with a constant AC load of 600Ω.

The values of ILL (long line current) and ILS (short line current) are programmable through I-start (pin 9) and I-slope (pin 15) (see also paragr. 4).

2.2 Sending Impedance

The impedance of the Output Stage Amplifier, Z_{out}, is determined by the impedance Z4 (at pin 3).

$$Z_{out} = 10.65 \, x Z4$$

The total AC impedance shown to the line is the parallel

$Z_{par} = Z_{out} // Z_{int} // Z_{ext}$

where:

- Z_{int} = 10KΩ//8.5 nF (internal)
- Z_{ext} = R6//C4 (at pin 16)

2.3 Sending Mute

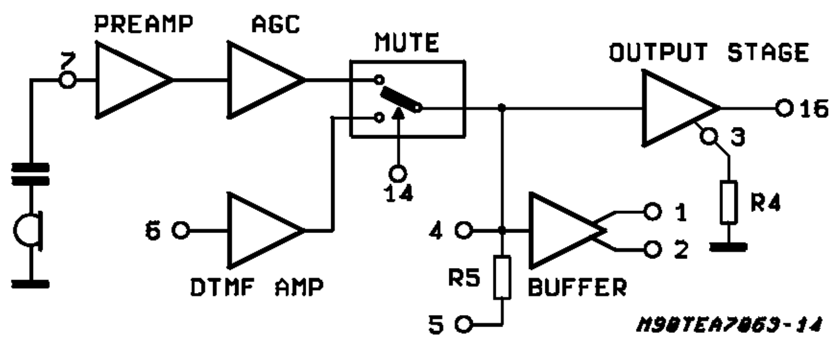
In normal speech operation (V_{mute} at pin 14 < 0.8V), the signal at Microphone Input (pin 7) is amplified to V_{line} (pin 16) with the gain Gs (long line) or 6dB lower (shorter lines) depending on AGC control (see paragr. 4).

In sending mute condition (V 14 > 1.6V) these gains are reduced of at least 60dB. In the same condition, DTMF input (pin 6) is activated, with gain Gmf to the line independent from I_{line} lenght.

2.4 Antisidetone Buffer

The signal coming from the sending preamplifier is internally presented at pin 4 and than buffered to pins 1 and 2 for sidetone cancellation (see paragraph 3.2).

Figure 3



2.5 Soft Clipping

To avoid distortion on line, the TEA7063 has a "soft clipping" on transmit channel.

The resistor (Rsoft) on pin 10 fixes the maximum AC peak dynamic on the line: V_{STL}

$$V_{STL}(Vp) = Vpin16(DC) - 1.44 \bullet \frac{R_{soft}\ (\text{pin } 10)}{R9\ (\text{pin } 8)}$$

where $Rsoft \leq \frac{1V}{I_{ST}}$ $I_{ST} = \frac{470mV}{2 \cdot R9\ (pin8)}$

The capacitor (C10) and the resistor (R10) connected on pin 11 fixe the constant time of the soft clipping.

Recommended values: C10 = 150nF;
R10 = 560KΩ

Figure 4

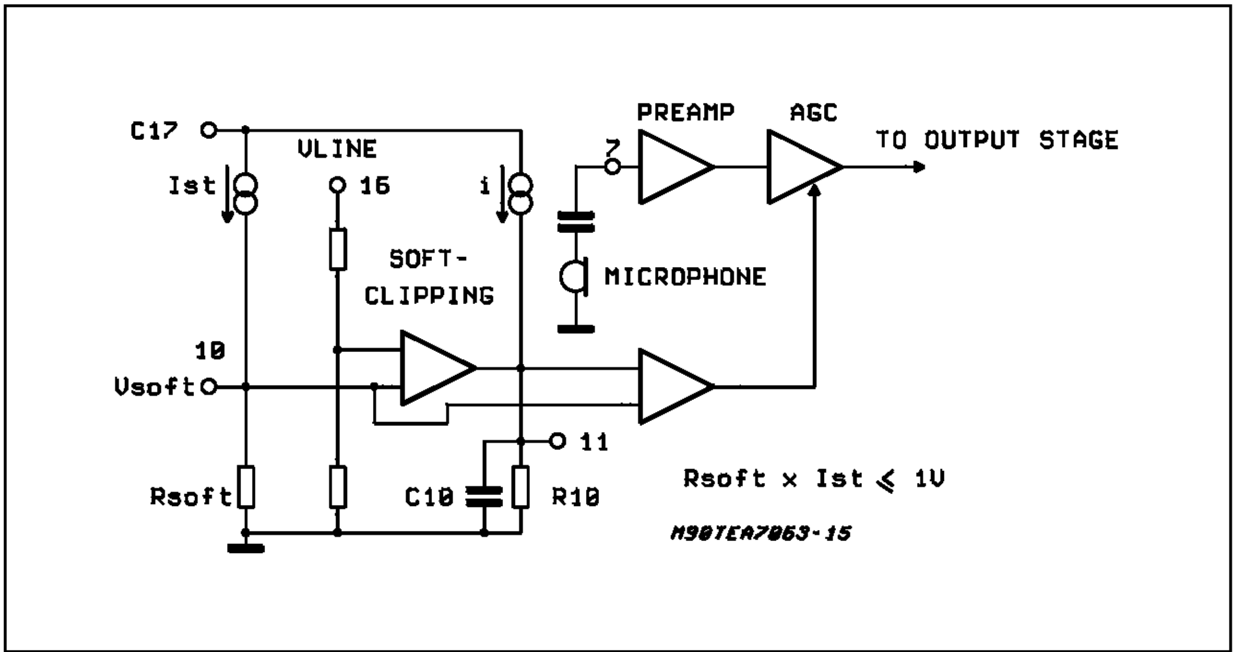
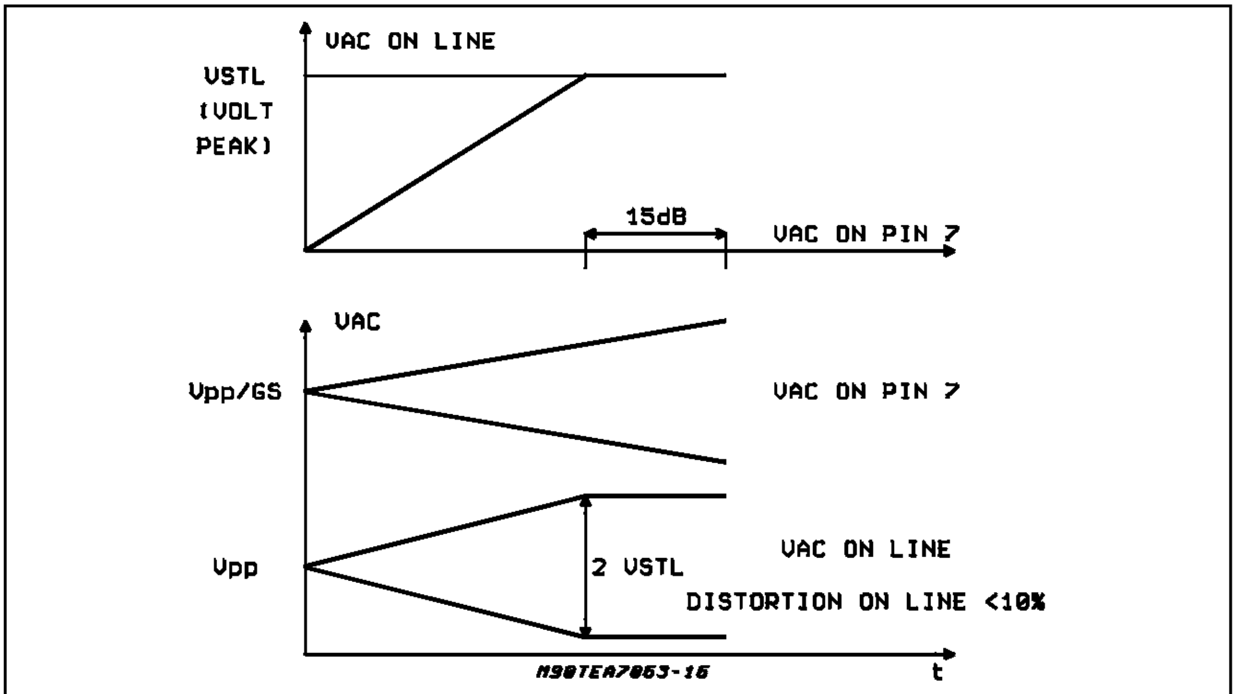


Figure 5: Transmit Curves



3. RECEIVE CHAIN

3.1 A.G.C. In Receive

As described for the transmission chain, also the receiving gains Gr, from pins 1 and 2 to pin 20, have a reduction of 6dB when Iline moves from ILL to ILS (see also paragr. 4).

3.2 Sidetone Compensation

The circuit is provided with a double anti-sidetone network to optimize both at long and short lines.

In case double antisidetone network is not requested by the application needs, pins 1 and 2 can be connected to each other and 5 external passive components can be saved (ZALL and ZRL).

Before entering pins 1 and 2, the received signal is areduced by the two attenating networks:

- ZALL/ZRL to pin 1 for long lines sidetone compensation,
- ZALS/ZRS to pin 2 for short lines sidetone compensation.

ZRL and ZRS define the total receive gains:

a) $\frac{V20}{V16} = G_r \bullet \frac{ZRL}{ZRL + ZALL}$ for long lines

b)

$\frac{V20}{V16} = (G_r - 6dB) \bullet \frac{ZRS}{ZRS + ZALS}$ for short lines

ZALL and ZALS define the sidetone compensation of the circuit.

The equivalent balancing impedance is given by the formula:

$ZAL = K \bullet ZALS + (1 - K) \bullet ZALL$

where:

-K = 0 at I_{LINE} = ILL or lower (long line)

-K varies linearly from 0 to 1 with Iline between ILL and ILS

-K = 1 at I_{LINE} = ILS or higher (short line)..

Calculations to define ZALL and ZALS are:

a)

$ZALL = 70 \bullet R5 \bullet \frac{Z_{line}(long) // Z_{ext} // Z_{int} // Z_{out}}{Z_{out}}$

b)

$ZALL = 70 \bullet R5 \bullet \frac{Z_{line}(short) // Z_{ext} // Z_{int} // Z_{out}}{Z_{out}}$

where:

- Z_{ext} = R6//C4//(Zelectret) (at pin 13)
- Z_{int} = 10KΩ//8.5nF (internal impedance)
- Z_{out} = 10.65 • Z4 (at pin 3; see paragr. 2.2)
- Zline (short) and (long) are the impedances of the line at minimum and naximum line lenght
- R5 = 5.1KΩ ±1% (typically)

3.3 AC Impedance

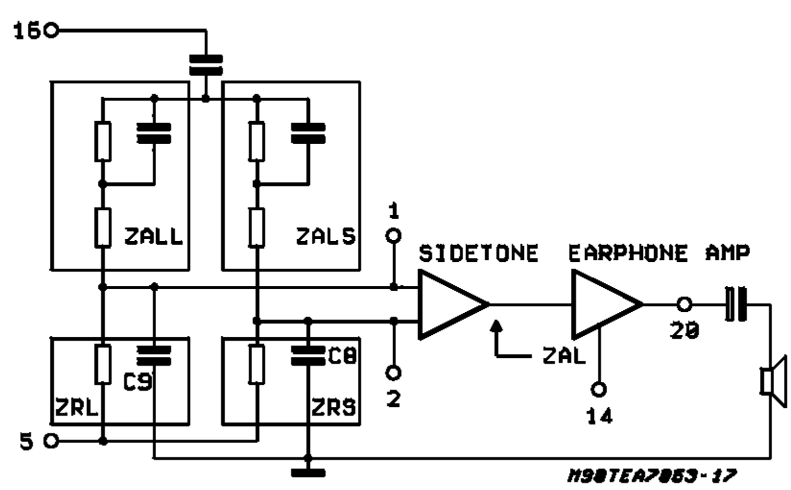
The total AC impedance of the circuit to the line is:

ZAC = Zout//Zint//Zext (ZALS, ZALL >>ZAC)

3.4 Receive Mute (and confidence level)

When the receive channel is muted (Vpin 14 > 2.7V) the receive gain is reduced of 60dB minimum.

Figure 6



In this condition an internal connection is activated from line DTMF output (pin 16) to Receive Output (pin 20) with an attenuation GRS = 38.5dB to provide acoustic feedback of the DTMF emission.

4. A.G.C AND SIDETONE PROGRAMMING

4.1 Programmable Controls

AGC and sidetone attack and disonnect points (or currents) are programmable externally through two independents pins, I-start (pin 9) and I-slope (pin 15).

4.2 I-Start (pin 9)

An external resistor RLL connected between I-start (pin 9) and Microprocessor Supply (pin 19) controls the attack point of AGC and ZAL (antisidetone Z).

ILL is the line current at which the control starts. Formulas for ILL and RLL with R9 = 100K are:

$$ILL = \frac{2880}{RLL} + 11mA$$

$$RLL = \frac{2880}{(ILL - 11mA)}$$

4.3 I-Slope (pin 15)

An external resistor RLS connected between I-slope (pin 15) and Microprocessor Supply (pin 19) controls the disconnected point of AGC and ZAS (antisidetone Z). ILS is the line current at which the control stops. Formulas for ILS and RLS with R9 = 100K are:

$$ILS = \frac{4680}{RLS} + ILL;$$

$$RLS = \frac{4680}{(ILS - ILL)}$$

4.4 A.G.C. OFF (pin 9 and 15)

Programming ILL and ILS respectively higher than 70mA and 450mA is forcing the IC in AGC OFF Condition.

Suggested external components are:
RLL = 51KΩ and RLS = 10KΩ

In this case sending, receiving gain and sidetone compensation are independent of the line lenght. Pins 1 and 2 can be connected to each other saving 5 passive external components at pin 2.

4.5 Secret Function for Private (pin 14)

The two separate thresholds for sending and Receiving Mute (pin 14) allow "Secret Function" (only microphone muted).

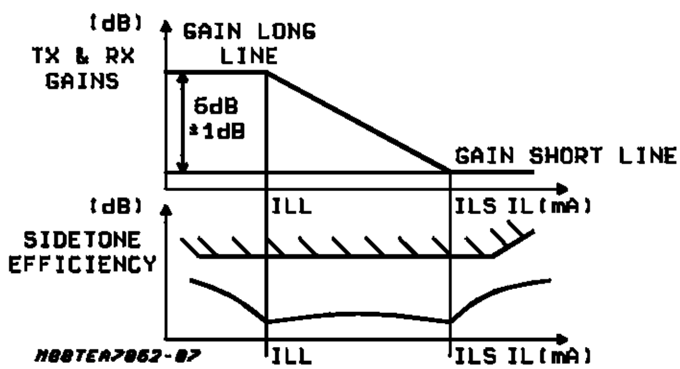
Pin 14 can be set:

a) between 0.25V and 0.8V for speech mode,

b) between 1.6V and 2.1V for "secret" mode (microphone muted),

c) between 2.7V and 3.3V for "all muted" mode

Figure 7



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5. MICROPROCESSOR INTERFACE

5.1 Microprocessor Supply (pin 19)

At "off-hook" the first priority of the circuit is to make some current available at the Microprocessor Supply (pin 19) to charge quickly the external capacitor C2.

This charging current is $I_{cpm} = 0.6 \bullet I_{LINE}$

T-charge of about 10ms is necessary, with C2 = 47/µF. to charge pin 19 at the specified value of 3.3V typical at I_{LINE} = 25mA:

$$\text{T-charge} = \frac{3.3V \bullet C2}{0.6 \bullet I_{LINE}} \text{ typically}$$

V_{mp} = 3.3V in normal operation and current increases linearly from 0.5mA min, at I_{LINE} = 6mA, to1.5mA, at I_{LINE} = 25mA, remaining stable for higher values of I_{LINE}. (with R9 = 100K)

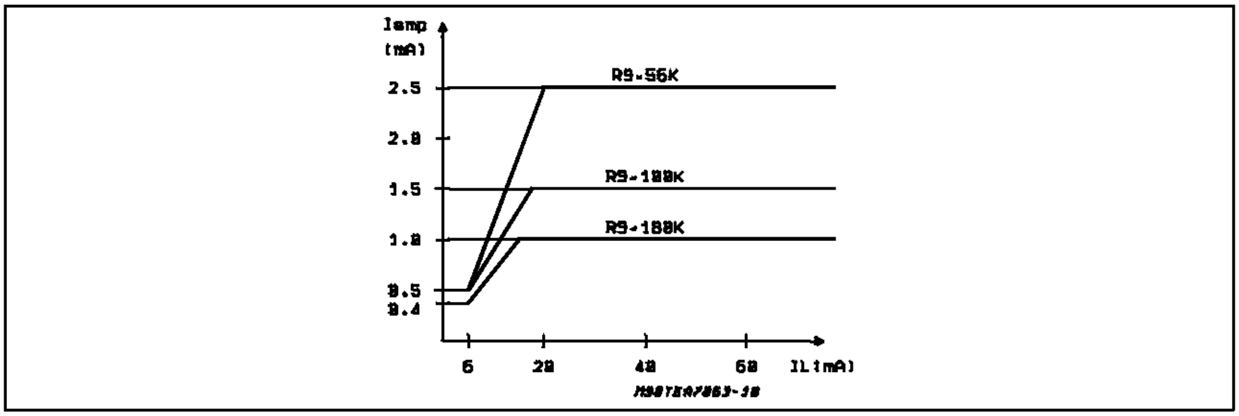
In general:

$$I_{mp} = \frac{130Volt}{R9} + 0.3mA \text{ at } I_L > 25mA$$

$$I_{mp} = \frac{11Volt}{R9} + 0.3mA \text{ at } I_L > 6mA$$

A zener of 3.9V typical is generally suggested to

Figure 8



6. CURRENT SOURCE FOR SPEAKERPHONE

6.1 Current Source (pin 12)

Most of the DC current available from the line is delivered by the speech circuit at the output I_{source} (pin 12) through an internal current generator.

Typical values of this current, I_{LS} with R9 = 100K, are:

$I_{LS} = (0.3 \bullet I_{LINE})$ for I_{LINE} < 16.5mA
$I_{LS} = (0.9 \bullet I_{LINE}$ -10mA) for I_{LINE} > 16.5mA

(ex: I_{LINE} = 16mA then I_{LS} = 5mA

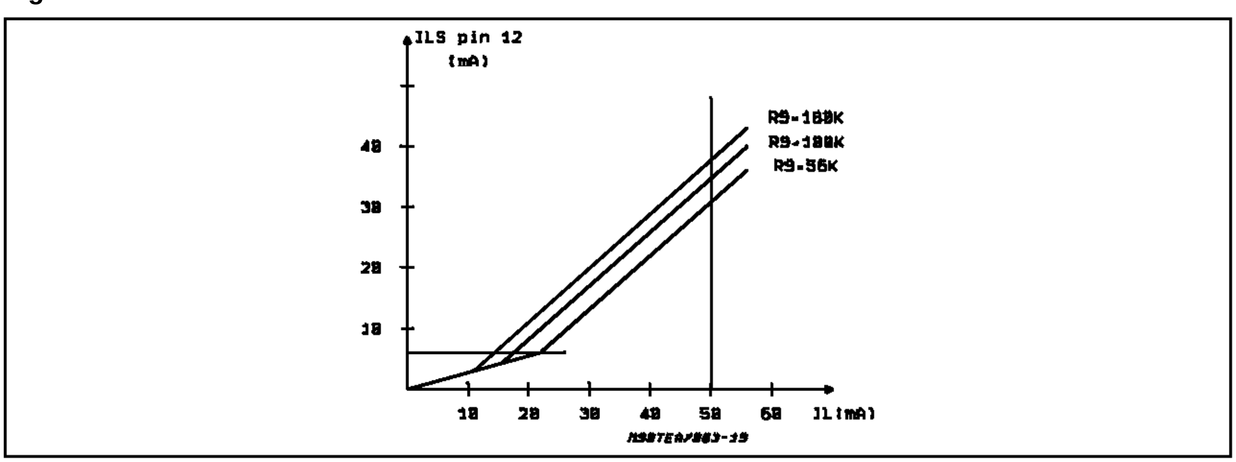
I_{LINE} = 30mA then I_{LS} = 17mA

I_{LINE} = 60mA then I_{LS} = 44mA).

The voltage level at pin 12 must be defined by an external regulator (i.e.: zener) and, if necessary, filtered with a capacitor (47 to 220µF).

In case V_{LINE} (at pin 16) approaches voltage at pin 12, then the internal current source switches off and its DC current is shunt to ground through and internal complementary generator, thus avoiding any negative effect on the AC and DC impedances of the telephone set application.

Figure 9



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7. INTERNAL DESCRIPTION OF CURRENT MANAGEMENT

7.1 Internal Power Supply Management

R9 fixes the line power supply management.
R9 fixes the values of: I_{ear}, I_{up}, I_{ref} and ILS.

A current line information is used to modifie the values of I_{ear}, I_{up}, I_{ref} and ILS between a minimum and a maximum values.

On Fig 10:
The transmit output stage is represented by a current source (I_{tr}). The I_{tr} value depends of the DC voltage on V_{LINE} (pin 16) and R_{ZAC} value.

The other internal stages connected to V_{LINE} (pin 16) are represented by a constant 1.3mA current source.

7.2 DC Characteristics (internal)

The DC characteristic is equals to:

$$V_{LINE}\ (\text{pin } 16) = V_C\ (\text{pin } 17) + R6 \bullet I_{int}$$

Iint is the sum of all the current sources connected on VC (pin 17):
$[I_p + I_{ref} + Vpin17 / (r7 + r8)]$

- I_p is the bias internal operational amplifiers power supply.
- $I_{ref} = 1 / 3 \bullet (V_{refi} / R9)$; with $V_{refi} = 470mV$
- $I_{ref} = 156 / R9$ mA

The current line information changes Iint value;

at low line current (6mA): $I_{int} = 4V / R9 + 60\mu A$

at low line current (IL = ILb): $I_{int} = 8V / R9 + 60\mu A$

7.3 Microcontroller Supply (internal)

$I_{up} = [(p2 / r2) \bullet I_{ref} + 0.3]$ mA $= [(p2 / r2) \bullet 156 / R9) + 0.3]$ mA

The current line information changes p2/r2 value;

at low line current (6mA): p2 / r2 = 70
at a line current (IL = ILb): p2 / r2 = 820

7.4 Earphone Current Supply (internal)

$I_{ear} = (p1 / r1) \bullet I_{ref}$ mA $= (p1 / r1) \bullet (156 / R9)$ mA

The current line information changes p1/r1 value;

at low line current (6mA): (p1 / r1) = 200
at a line current (IL = ILb): p1 / r1 = 2700

The maximum peak dynamic on the earphone is:
$V_{pear} = Z_{ear} \bullet I_{ear}$

7.5 Transmit Output Stage (internal)

The output stage bias current depends of the DC voltage on pin 16 and on R_{ZAC} impedance.

$I_{tr} = \dfrac{0.1425 \bullet V_{LINE} - 0.517}{R_Z}$ (R_Z is the resistor connected betwee pin3 and the ground)

7.6 Loudspeaker Current Source (internal)

The current source for external peripherals has two slopes:

- First slope; before I_{ear}, I_{up}, I_{tr} and I_{int} are stabilized at their maximum values: (IL = ILb)

$$ILS = 0.285 \bullet IL$$

- Second slope; after I_{ear}, I_{up}, I_{tr} and I_{int} are stabilized at their maximum values: (for IL > ILb)

$$\Delta\ (ILS) = 0.91 \bullet \Delta(I_{LINE}$$

I_{ear}, I_{up}, I_{tr} and I_{int} are stabilized at their maximum values between 16 and 26mA, the absolute IL value depends of R9 value. The line current (ILb) where I_{ear}, I_{up}, Itr, I_{int} are stabilized at their maximum values and where the slope of ILS change is:

$$ILb = \frac{I_{ear} + I_{up} + I_{tr} + I_{int} + 1.3}{0.715}$$

7.7 Numerical Example

1) R9 = 100KΩ; R6 = 25KΩ

♦ DC characteristic = 6V for I_{int} max:
= 5V for I_{int} min:

I_{int} min (IL = 6mA) = 4 /100K + 60 = 100µA
I_{int} min (IL = ILb) = 8 /100K + 60 = 140µA

Vpin17 = 2.5V ⇒ R6 = 25KΩ ⇒
Vpin16 min (IL = 6mA) = 2.5 + 25 • 100E - 3 = 5V
Vpin16 max (IL = ILb) = 2.5 + 25 • 140E - 3 = 6V

♦ Current Sources

I_{up} min (IL = 6mA) = 0.4mA
I_{up} max (IL = ILb) = 1.6mA

I_{ear} min (IL = 6mA) = 0.3mA
I_{ear} max (IL = ILb) = 4.2mA

with $R_Z = 75\Omega$

I_{tr} min (IL = 6mA) = 2.6mA
I_{tr} max (IL = ILb) = 4.5mA

ILS min (IL = 6mA) = 1.3mA

♦ ILb

$$ILb = \frac{1.6 + 4.2 + 4.5 + 0.14 + 1.3}{0.715}\ \text{mA}$$

ILb = 16.5mA

ILS (for IL = ILb) = 0.285 • ILb = 4.7mA

♦ at IL = 100mA:

Δ(ILS) = 0.91 • Δ(IL) = 0.91 • (100 - 16.5) = 76mA
ILS = 4.7 + 76 = 80.7mA

2) R9 = 56KΩ; R6 = 18KΩ

♦ DC characteristic = 6.1V for I_{int} max:
= 4.8V for I_{int} min:

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I_{int} min (IL = 6mA) = 4 /56K + 60 = 130µA
I_{int} min (IL = ILb) = 8 /56K + 60 = 200µA

Vpin17 = 2.5V ⇒ R6 = 18KΩ ⇒
Vpin16 min (IL = 6mA) = 2.5 + 18 • 130E - 3 = 4.85V
Vpin16 max (IL = ILb) = 2.5 + 18 • 200E - 3 = 6.1V

♦ Current Sources

I_{up} min (IL = 6mA) = 0.5mA
I_{up} max (IL = ILb) = 2.5mA

I_{ear} min (IL = 6mA) = 0.55mA
I_{ear} max (IL = ILb) = 7.5mA

with R_Z = 75Ω

I_{tr} min (IL = 6mA) = 2.35mA
I_{tr} max (IL = ILb) = 4.5mA

ILS min (IL = 6mA) = 1.17mA

♦ ILb

$$ILb = \frac{2.5 + 7.5 + 4.5 + 0.2 + 1.3}{0.715} \text{ mA}$$

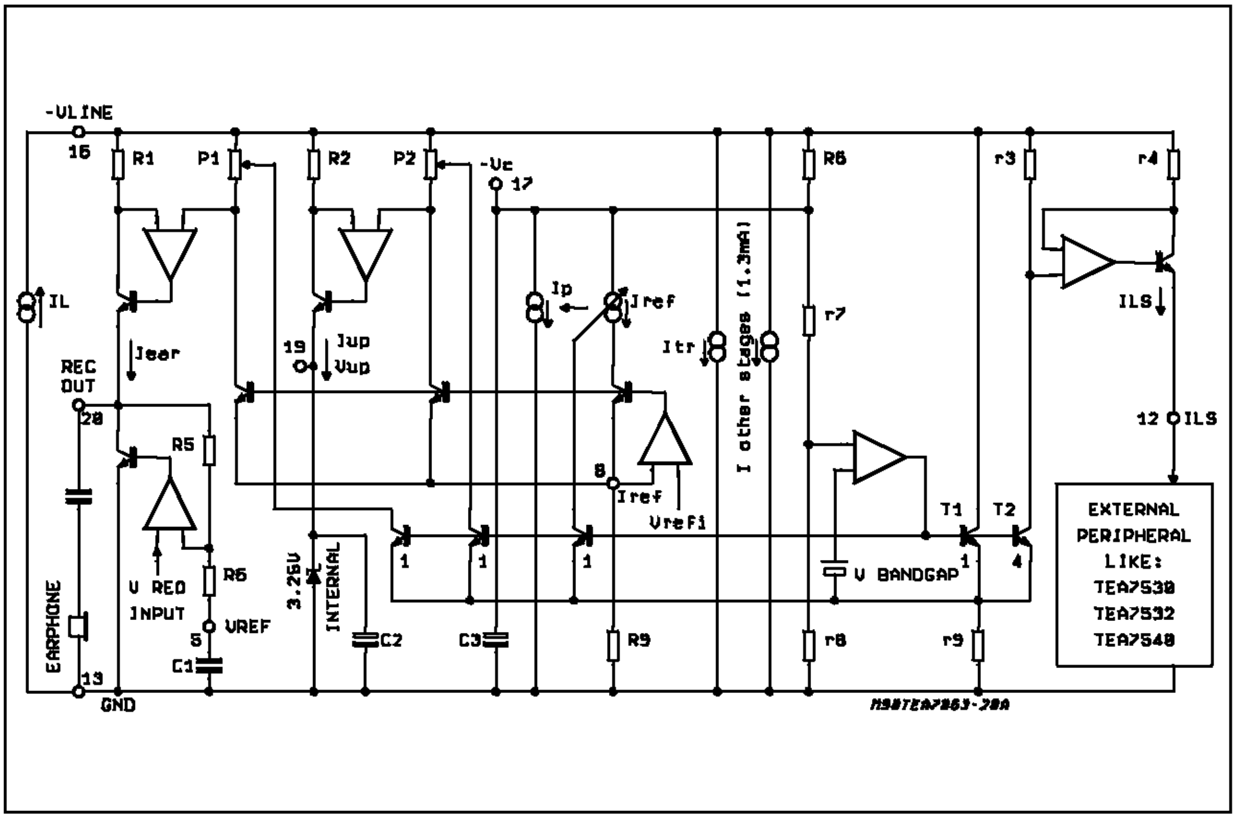
ILb = 22.4mA

ILS (for IL = ILb) = 0.285 • ILb = 6.4mA

♦ at IL = 100mA:

Δ(ILS) = 0.91 • Δ(IL) = 0.91 • (100 - 22.6) = 64mA
ILS = 6.4 + 64 = 70.4mA

Figure 10: Line Power Supply Management



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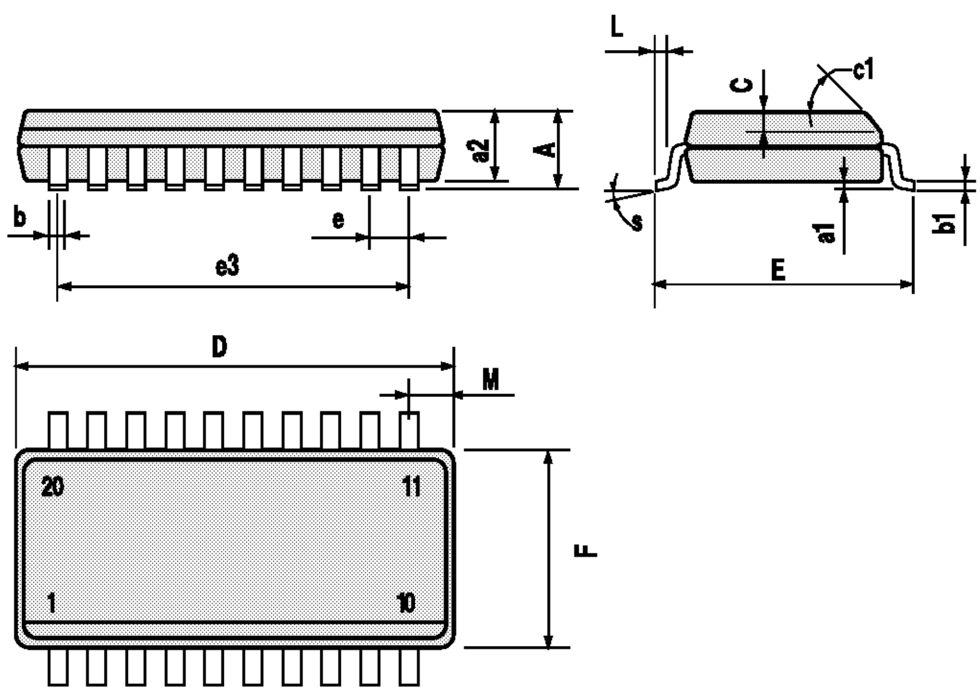
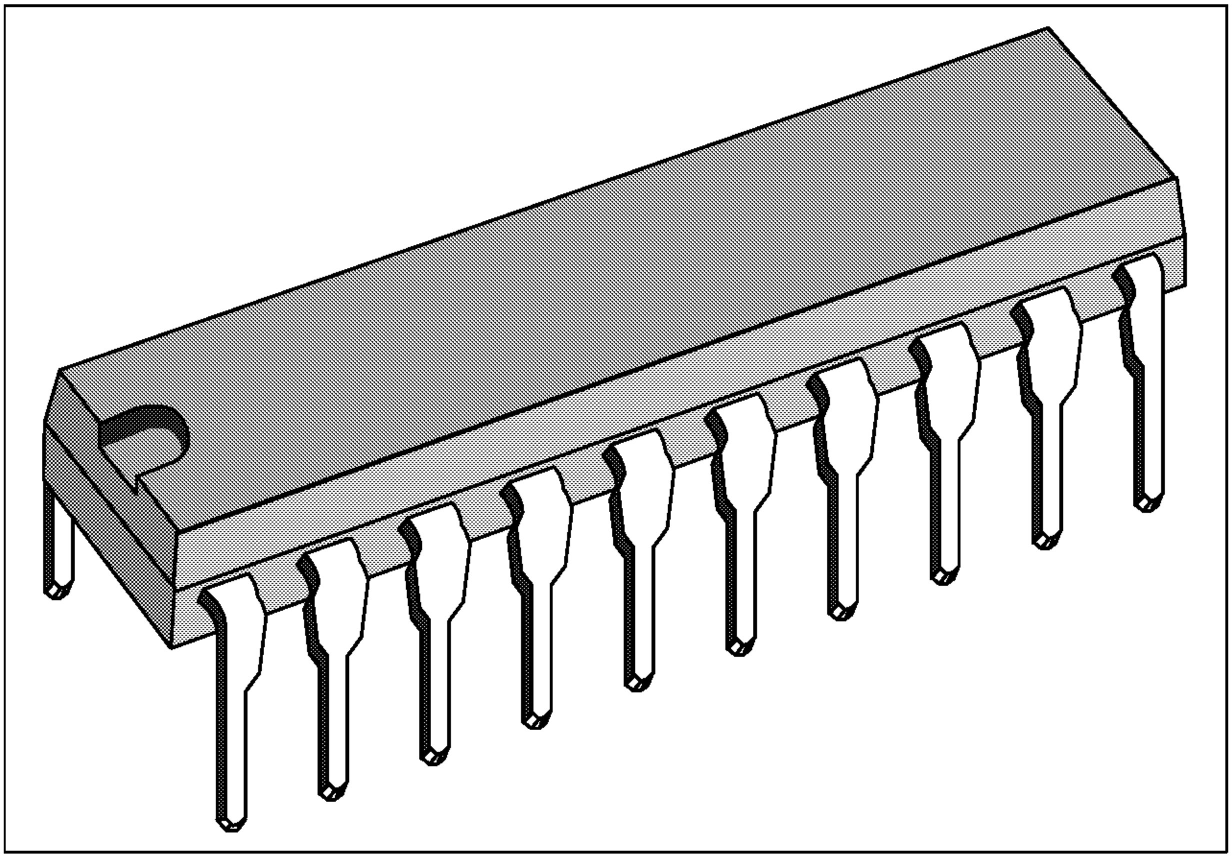
SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					



DIP20 PACKAGE MECHANICAL DATA

DIM	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
i			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



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