



TEA2025D

LINEAR INTEGRATED CIRCUIT

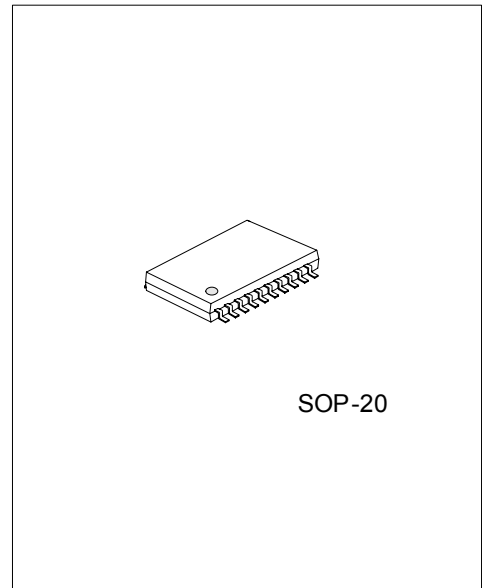
STEREO AUDIO AMPLIFIER

DESCRIPTION

The UTC TEA2025D is a monolithic integrated circuit that intended for use as dual or bridge power audio amplifier portable radio cassette players.

FEATURES

- * Dual or bridge connection modes.
- * Few external components.
- * Supply voltage down to 3V.
- * High channel separation.
- * Very low switch on/off noise.
- * Max gain of 45dB with adjust external resistor.
- * Soft clipping.
- * Thermal protection.
- * $3V < V_{CC} < 15V$
- * $P = 2 * 1W, V_{CC} = 6V, R_L = 4\Omega$
- * $P = 2 * 2.3W, V_{CC} = 9V, R_L = 4\Omega$
- * $P = 2 * 0.1W, V_{CC} = 3V, R_L = 4\Omega$



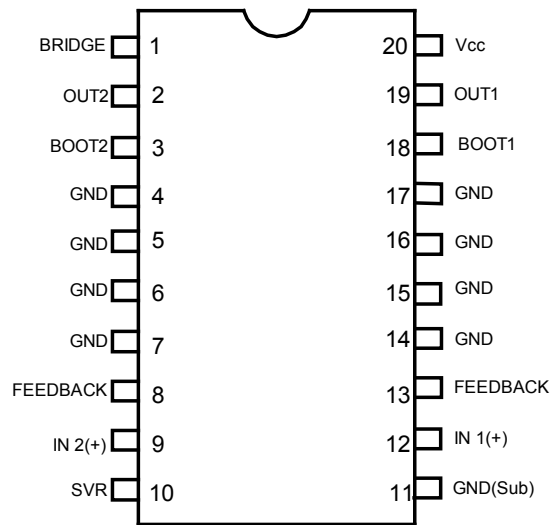
*Pb-free plating product number: TEA2025DL

ORDERING INFORMATION

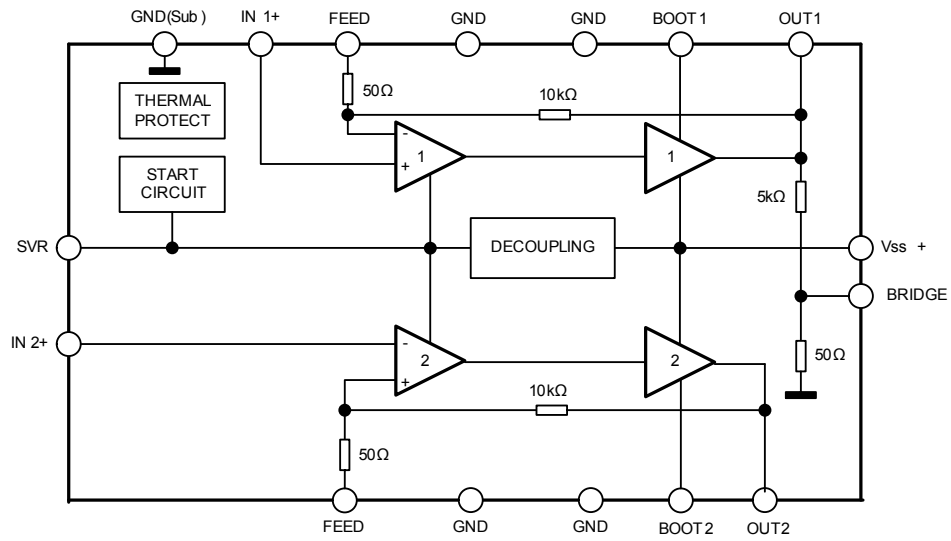
Order Number		Package	Packing
Normal	Lead Free Plating		
TEA2025D-S20-R	TEA2025DL-S20-R	SOP-20	Tape Reel
TEA2025D-S20-T	TEA2025DL-S20-T	SOP-20	Tube

<p>TEA2025DL-S20-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Lead Plating 	<ul style="list-style-type: none"> (1) R: Tape Reel, T: Tube (2) S20: SOP-20 (3) L: Lead Free Plating, Blank: Pb/Sn
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■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{SS}	15	V
Output Peak Current	$I_{O(PEAK)}$	1.5	A
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-case	θ_{JC}	15	°C/W
Thermal Resistance Junction-ambient	θ_{JA}	65	°C/W

Note: The θ_{JA} is measured with 4 cm² copper area heatsink.

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=9V, Stereo unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
Supply Voltage	V_{SS}		3		12	V			
Quiescent Current	I_Q			35	50	mA			
Quiescent Output Voltage	V_{OUT}			4.5		V			
Voltage Gain	G_V	Stereo	43	45	47	dB			
		Bridge	49	51	53	dB			
Voltage Gain Difference	$\Delta G_{V(DIFF)}$				±1	dB			
Input Impedance	R_I			30		kΩ			
Output Power (d=10%)	$R_L=4\Omega$	P_{OUT}	Stereo 8 (per channel)	$V_{SS}=3V$		0.1	W		
	$R_L=32\Omega$					0.02			
	$R_L=4\Omega$			$V_{SS}=6V$		0.7		1	
	$R_L=8\Omega$					0.6			
	$R_L=16\Omega$					0.25			
	$R_L=32\Omega$					0.13			
	$R_L=4\Omega$				$V_{SS}=9V$			1.7	2.3
	$R_L=8\Omega$							1.3	
	$R_L=8\Omega$	$V_{SS}=12V$		2.4					
	$R_L=16\Omega$		P_{OUT}	Bridge	$V_{SS}=3V$			0.18	
	$R_L=32\Omega$							0.06	
	$R_L=4\Omega$				$V_{SS}=6V$			2.8	
	$R_L=8\Omega$							1.5	
	$R_L=8\Omega$		$V_{SS}=9V$		4.7				
Distortion	Stereo	d	$V_{SS}=9V; R_L=4\Omega$		0.3	1.5	%		
	Bridge				0.5	%			
Supply Voltage Rejection	SVR	$f=100Hz, V_R=0.5V, R_g=0$	40	46		dB			
Input Noise Voltage	$eN_{(IN)}$	$R_g=0$		1.5	3	mV			
		$R_g=104\Omega$		3	6	mV			
Cross-Talk	CT	$f=1KHz, R_g=10K\Omega$	40	52		dB			

APPLICATION INFORMATION

Input Capacitor

Input capacitor is PNP type allowing source to be referenced to ground.

In this way no input coupling capacitor is required. However, a series capacitor(0.22µF) to the input side can be useful in case of noise due to variable resistor contact.

Bootstrap

The bootstrap connection allows to increase the output swing.

The suggested value for the bootstrap capacitors (100µF) avoids a reduction of the output signal also at low frequencies and low supply voltage.

Voltage Gain Adjust

STEREO MODE

The voltage gain is determined by on-chip resistors R1 and R2 together with the external RfC1 series connected between pin 8(13) and ground. The frequency response is given approximated by:

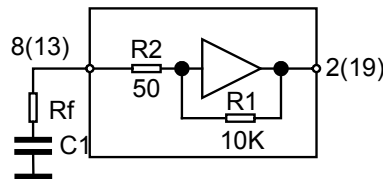
$$\frac{V_{OUT}}{V_{IN}} = \frac{R1}{Rf + R2 + \frac{1}{j\omega C1}}$$

With Rf=0, C1=100µF, the gain results 46dB with pole at f=32Hz

The purpose of Rf is to reduce the gain. It is recommended to not reduce it under 36dB.

BRIDGE MODE

Figure 7



The bridge configuration is realized very easily thanks to an internal voltage divider which provides (at pin 1) the CH1 output signal after reduction. It is enough to connect pin8(inverting input of CH 2) with a capacitor to pin 1 and to connect to ground the pin 9.

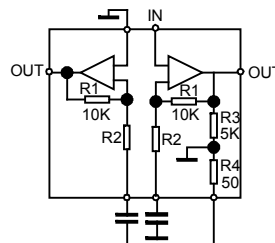
The total gain of the bridge is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R1}{Rf + R2 + \frac{1}{j\omega C1}} \left(1 + \frac{R3}{R4} \frac{R1}{R2 + R4 + \frac{1}{j\omega C1}} \right)$$

and with the suggested values (C1=C2=100µF, Rf=0) means:

Gv=52dB

Figure 8



With first pole at f=32Hz

■ APPLICATION INFORMATION(Cont.)

Output Capacitors.

The low cut off frequency due to output capacitor depending on the load is given by:

$$F_L = \frac{1}{2\pi C_{OUT} * R_L}$$

With C_{OUT} 470 μ F and $R_L=4$ ohm it means $F_L=80$ Hz.

Stability

A good layout is recommended in order to avoid oscillations. In general, the designer must pay attention on the following points:

- Short wires of components and short connections.
- No ground loops.
- Bypass of supply voltage with capacitors as nearest as possible to the supply I.C. pin. The low value (polyester) capacitors must have good temperature and frequency characteristics.
- No sockets.

The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_{OUT} (and therefore P_D) and I_d are reduced.

APPLICATION SUGGESTION

The recommended values of the components are those shown on stereo application circuit of Fig.2 different values can be used, the following table can help the designer.

Component	Recommended	Purpose	Larger Than	Smaller Than
C1,C2	0.22 μ F	Input DC Decoupling in Case of Slider Contact Noise of Variable Resistor		
C3	100 μ F	Ripple Rejection		Degradation of SVR, Increase of THD at Low Frequency and Low Voltage
C4,C5	100 μ F	Bootstrap		
C6,C7	470 μ F	Output DC Decoupling		Increase of Low Frequency Cut-off
C8,C9	0.15 μ F	Frequency Stability		Danger of Oscillations
C10,C11	100 μ F	Inverting Input DC Decoupling		Increase of Low Frequency Cut-off

■ TYPICAL APPLICATION CIRCUIT

Figure 1: Bridge Application (Powerdip)

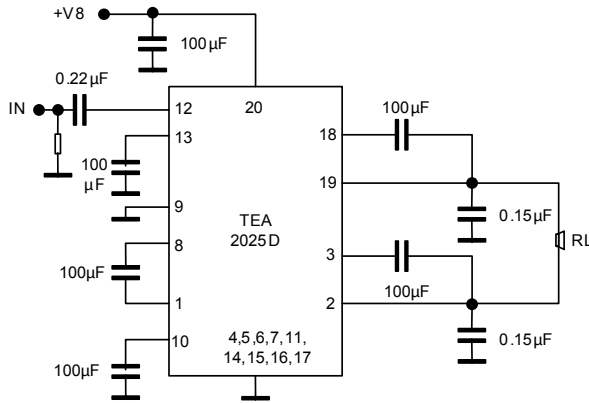
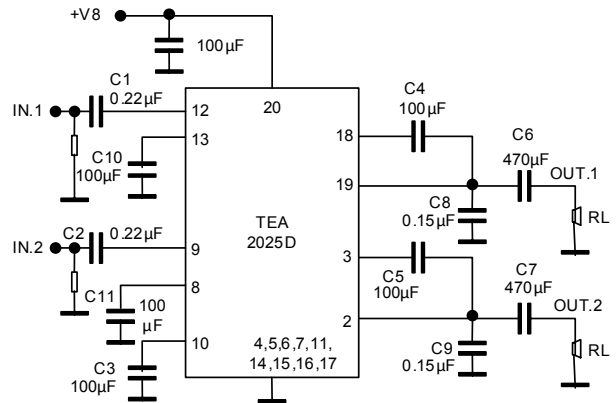
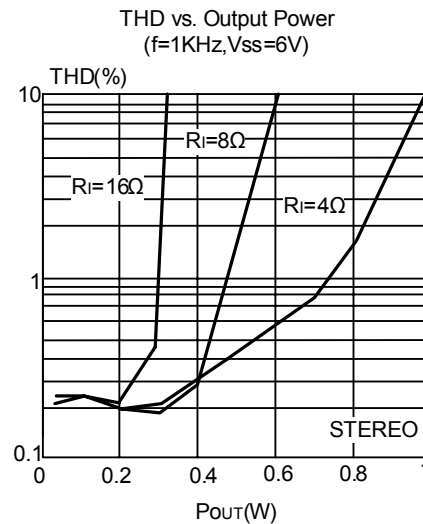
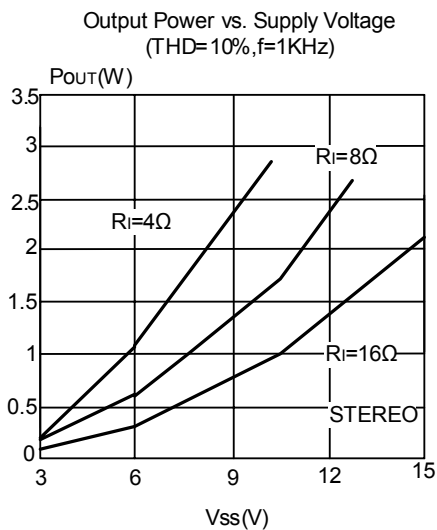
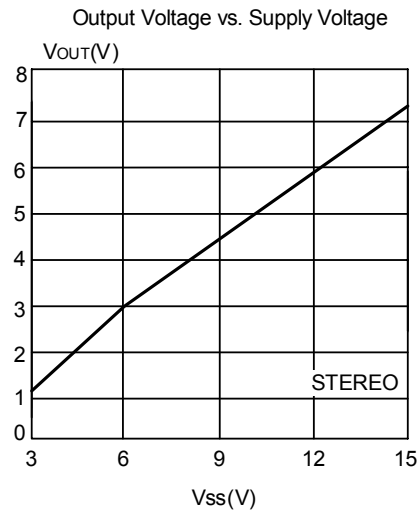
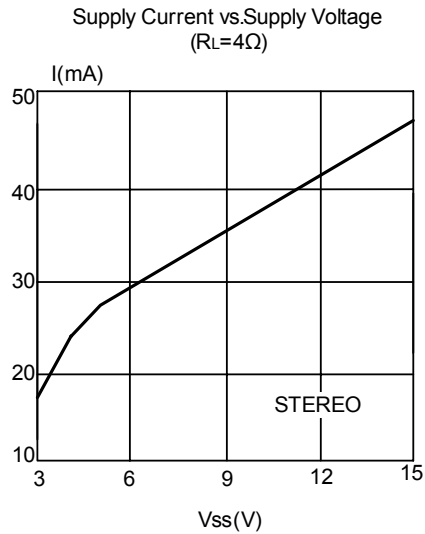


Figure 2: Stereo Application (Powerdip)



■ TYPICAL CHARACTERISTICS



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