Zero Voltage Switch with Fixed Ramp

Description

The monolithic integrated bipolar circuit, TEA1024/ TEA1124 is a zero voltage switch for triac control in domestic equipments. It offers not only the control of a triac in zero crossing mode but also the possibility of power control. This is why the IC contains a mains synchronized ramp generator with 640 ms (1280 ms) duration (50 Hz). It is suitable for a typical load of 750 W (1000 W) meeting the Flicker Standard. (values in brackets relate to TEA1124.)

Features

- Direct supply from the mains
- Definite IC switching characteristics
- Very few external components
- Full wave drive – no dc component in the load circuit
- Current consumption ≤ 1.5 mA
- Output short circuit protected
- Simple power control
- Integrated ramp generator
- Reference voltage variable by external resistance
- Pulse position optimization

Package: DIP8

Block Diagram

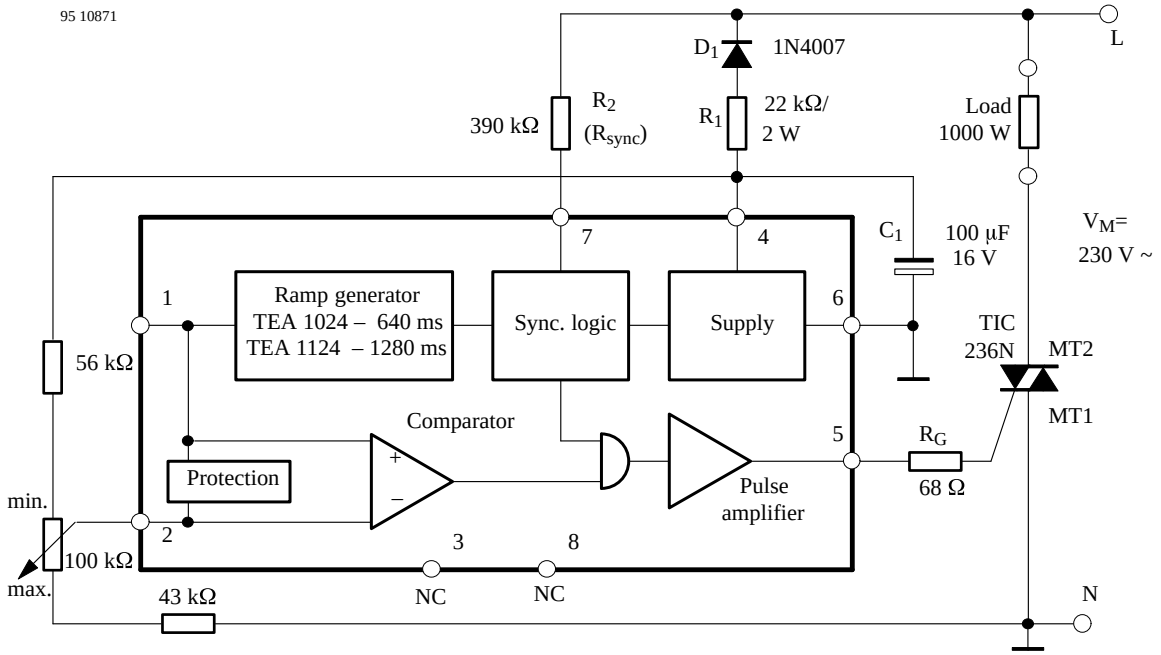


Figure 1. Typical block diagram – open loop power control

Power Supply and its Limitations

The voltage limitation contained in the IC allows it to be powered from mains via series resistance R_1 and recti–fying diode D_1 between Pin 6 (+ Pol/ ⊥) and Pin 4 ($–V_S$). The capacitor C_1 smooths the supply voltage (see figure 1).

An internal temperature-compensated limiting circuit protects the module from random peaks of voltage on the mains, and delivers a defined reference voltage during the negative half-cycle.

Synchronization

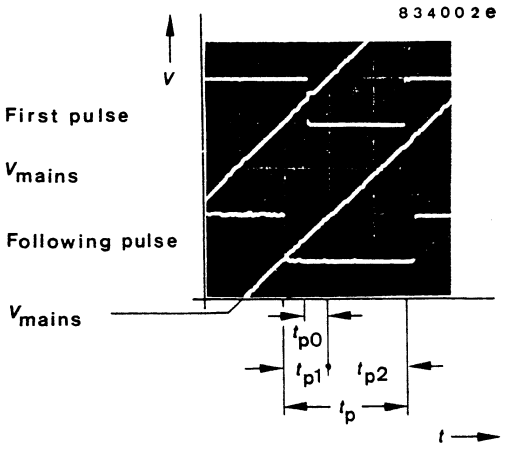


Figure 2. Pulse position optimization

The logic function is synchronized by means of a separate resistance R_2 connected between Pin 7 and phase (voltage-synchronization). The width of the pulse can be varied between wide limits by choice of R_{sync}. The larger the value chosen, the wider the output pulse is on Pin 5. Automatic optimization of the phase of the pulse is necessary, since the latching current of the triac exceeds the steady current by a factor of 3.

The phase of the pulse is chosen so that ca. 1/3 of the pulse width appears before the transition through null and 2/3 after it (see electrical characteristics and figure 2).

In order to avoid phase-clipping after the switch-on the first third of the first pulse is automatically suppressed.

Full-Wave Logic

The full-wave logic ensures that only pairs of pulses can be released, and that these always begin with the positive dv/dt. The load is thus switched on for a minimum of one complete mains cycle. This means that the triac receives a minimum of two driving pulses, so that the unwanted d.c. component in the load circuit is definitely eliminated.

Pulse Amplifier

The pulse amplifier connected to the output of the full-wave logic circuit, is proof against continuos short-circuits, and delivers negative output pulses of typ. 75 mA, via an integrated limiting resistance, to Pin 5.

Ramp Generator (Figures 3, 4)

Ramp voltage which is generated in the IC is available not only at reference Pin 1, but also at the non-inverted input of the comparator.

The current sink which is controlled by D/A converter influences the internal reference voltage at Pin 1 specified by voltage divider. The current sink is turned-off in the reset state of the D/A converter so that the voltage at Pin 1 is primarily specified via the internal voltage divider (ramp starting voltage).

In the maximum state of the 4 stage (5 stage – TEA1124) D/A converter, the current sink overtakes the maximum current, whereby the ramp's final (end) voltage has reached. External resistance R_x, R_y shown in figure 4 are in position to influence the initial ramp voltage as well as the ramp amplitude. If the external resistances ratio R_x, R_y is the same as that of the internal ratio, the ramp voltage at the beginning remains maintained (constant), only the amplitude is compressed.

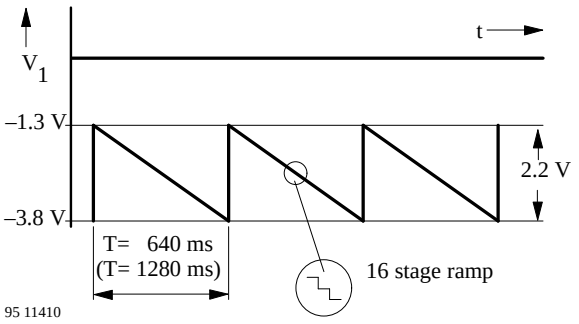


Figure 3. Ramp diagram without external circuit

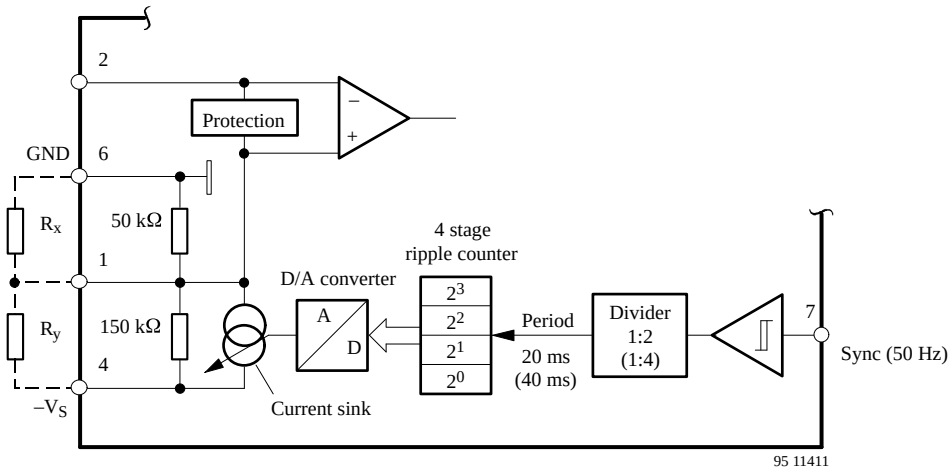


Figure 4. Principle diagram – Generation and evaluation of ramp

Period

1. The time required for one complete cycle of a regular. repeating signal, function, or series of emends.
2. The tune between two consecutive transients of the pointer or indicating means of an electrical indicating instrument in the same disdain the rest position. Something called periodic fine.

Comparator

The comparison of set value and measured value is carried out via the two comparator inputs Pin 1 and Pin 2. Here Pin 2 is the inverting input and has a circuit protecting it against interference spikes. Figure 5 shows the protective circuit of the comparator. Pin 1 is the non-inverting input.

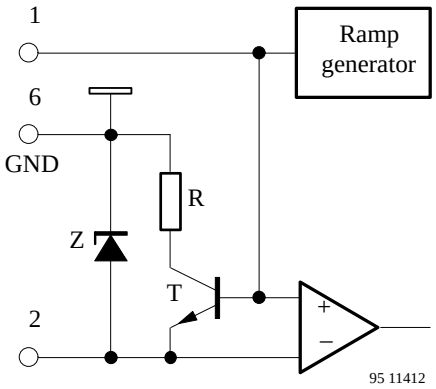


Figure 5. Protective circuit of the comparator

Firing Pulse Width (Figures 6, 7)

It depends on the latching current as well as on the load current of the used triacs.

$$t_p[s] = \frac{3}{4\ \pi\ f}\ \arcsin\frac{I_L \times V_M}{P \times \sqrt{2}}$$

whereas $I_L[A]$ = Latching current of the triac
$V_M[V]$= Mains voltage, effective
P[W] = Power load
f[1/s] = Mains frequency

Firing pulse width is specified through the zero cross over identification which can be influenced by the sync. resistance.

$$R_{sync}\ [\Omega] = \frac{V_M \sqrt{2}\ \sin\left(\frac{2}{3} \times \omega \times t_p\right) - 0.6}{2.5\ \times 10^{-5}} - 1.4\ \times 10^3$$

where
t_p [s] = required ignition pulse width

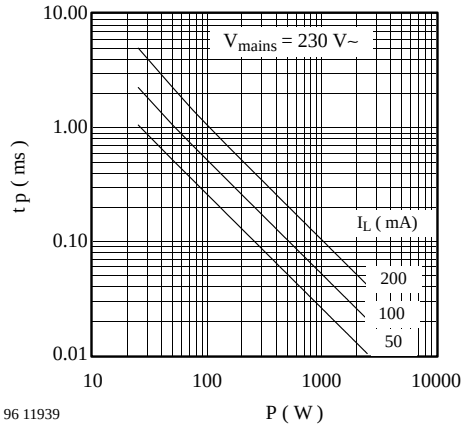


Figure 6.

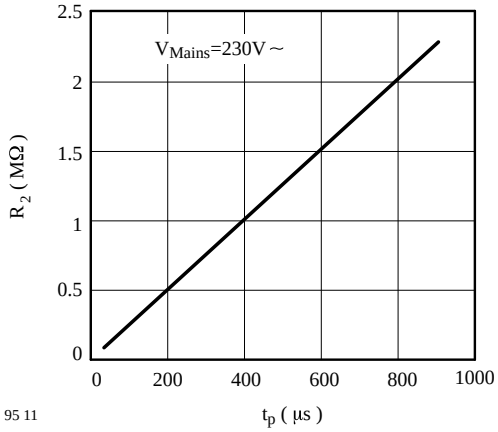


Figure 7.

Ignition (Firing) Current

The necessary ignition current depends on the specified triac. With the help of a resistance, it is possible to limit its value:

$$R_{Gmax}[\Omega] \approx \frac{5.7\ V - V_{Gmax}}{I_{Gmax}} - 25\ \Omega$$

$$I_p[A] = \frac{I_{Gmax}}{T} \times t_p$$

whereas V_G[V]= Gate voltage of the triac
I_G[A]= Max. gate current
I_P[A] = Average gate current requirement
t_P[s] = Ignition pulse width
T[s] = Duration (of mains frequency)

Supply Voltage

Due to higher trigger sensitivity of the triac it is supplied with negative signal. It can be supplied via diode and series resistance from the negative half wave of the mains. An internal parallel controller limits the voltage between Pin 5 and 7 to a typical value of 6.55 V.

Dimensioning of the Series Resistance R_1 (Figures 8, 9)

$$R_{1max} = 0.85\ \frac{V_{Mmin} - V_{Smax}}{2\ I_{tot}} - 65\ \Omega$$

$$I_{tot} = I_S + I_P + I_X \qquad P(R_1) = \frac{(V_M - V_S)^2}{2\ R_1}$$

V_M = Mains supply
V_S = Limiting voltage of the IC
I_{tot} = Total current requirement
I_x = Current requirement for external circuit

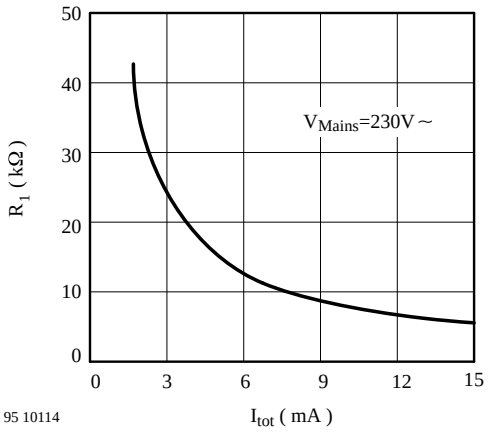


Figure 8.

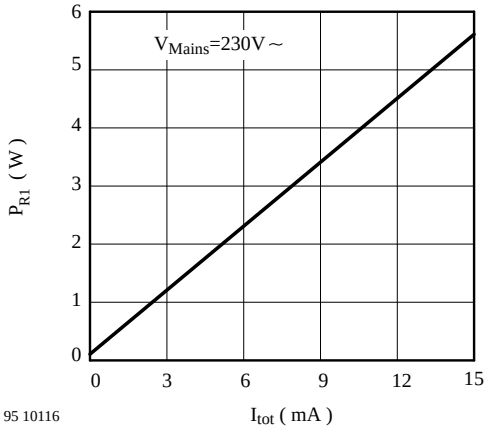


Figure 9.

Absolute Maximum Ratings

Reference point Pin 6

Parameters		Symbol	Value	Unit
Current consumption	Pin 4	$-I_S$	30	mA
$t \leq 10$ µs		i_s	150	
Sync. current	Pin 7	I_{Sync}	5	mA
$t \leq 10$ µs		i_{Sync}	40	
Comparator input current	Pin 2	$\pm I_I$	1	mA
Input voltages	Pin 1,4,5	$-V_I$	$\leq V_S$	V
	Pin 5	$+V_I$	≤ 0.5	
Power dissipation				
$T_{amb} = 45°C$		P_{tot}	400	mW
$T_{amb} = 100°C$			125	
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	0 to 100	°C
Storage temperature range		T_{stg}	–40 to + 125	°C

Thermal Resistance

Parameters	Symbol	Maximum	Unit
Junction ambient	R_{thJA}	200	K/W

Electrical Characteristics

Supply voltage $-V_S = 5.6$ V, $T_{amb} = 25°C$, f = 50 Hz, reference point Pin 6, unless otherwise specified

Parameters	Test Conditions / Pins		Symbol	Min	Typ	Max	Unit
Supply voltage limitation	$-I_4 = 1$ mA	Pin 4	$-V_S$	5.7		7.4	V
Current consumption	Pos. half, cycle	Pin 4	$-I_S$			1	mA
	Zero cross over						
	(Pin 5 open)	Pin 4	$-I_S$			1	
	neg. half cycle	Pin 4	$-I_S$			1.8	
Synchronization		Pin 7					
Voltage limitation	$\pm I_7 = 1$ mA		$\pm V_I$	1.0		1.8	V
Synchronization current			$\pm I_{Sync}$	0.15			mA
Zero cross detection			$\pm I_{Sync}$		25		µA
Comparator, figure 5							
Input zero voltage		Pin 1, 2	V_{10}		10		mV
Input quiescent current		Pin 2	I_B			1	µA
Common mode input range		Pin 1, 2	$-V_{IC}$	1	$(V_S-1.6)$		V

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Ramp generator, figures 3, 4	Pin 1					
Period	TEA1024	T		640		ms
	TEA1124			1280		
Step number		n		16		
Initial voltage		$-V_1$	1.2	1.4	1.6	V
Final voltage		$-V_1$	3.3	3.6	3.9	V
Internal reference				$\left(\frac{V_S + 2.5\%}{4–7.5\%}\right)$		V
Temperature coefficient of internal reference		$\pm TC_{Ref}$		1.2		mV/K
Pulse amplifier	Pin 5					
Output pulse current	$V_G \leq 1.5$ V	$-I_O$	50		100	mA
Output pulse width	V_{Sync} = 230 V ~, R_2 = 220 kΩ	t_0 t_1 t_2		33 65 110		µs

Applications

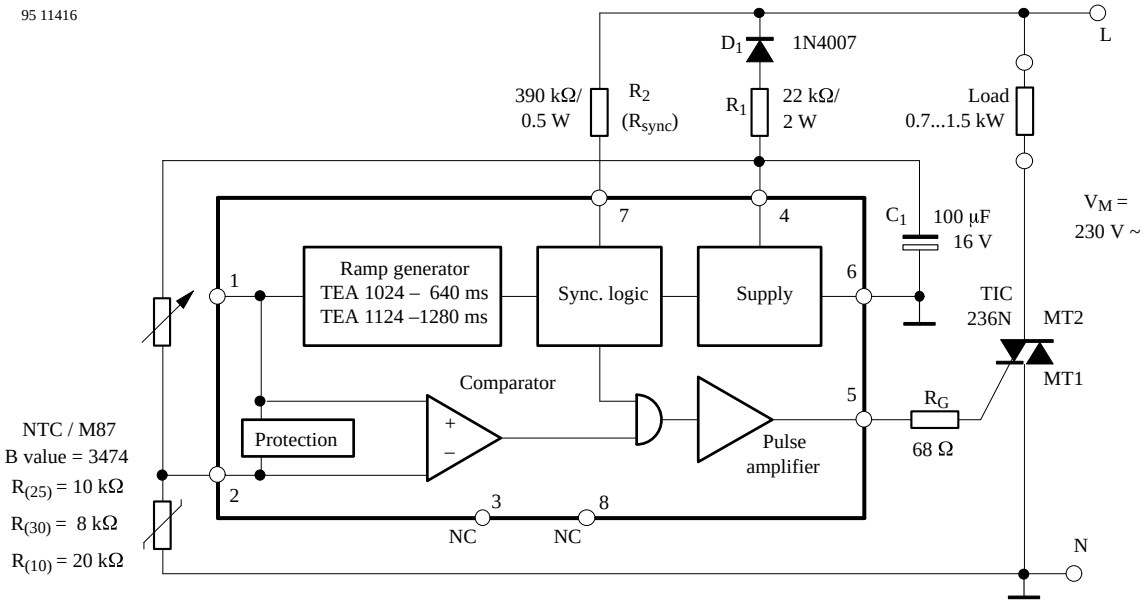


Figure 10. Simple temperature regulation with maximum proportional range

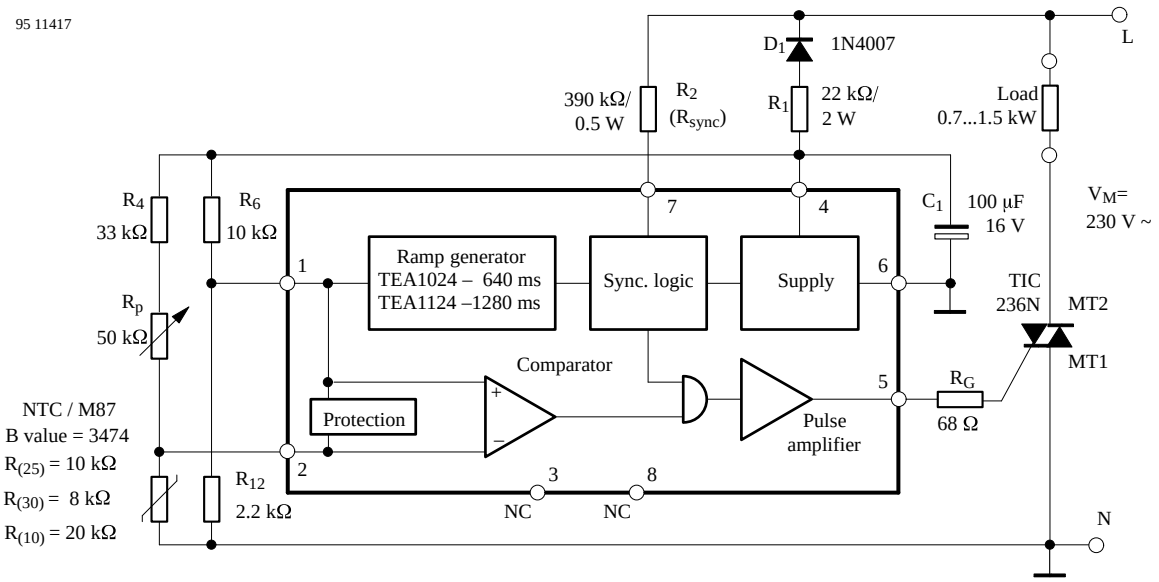
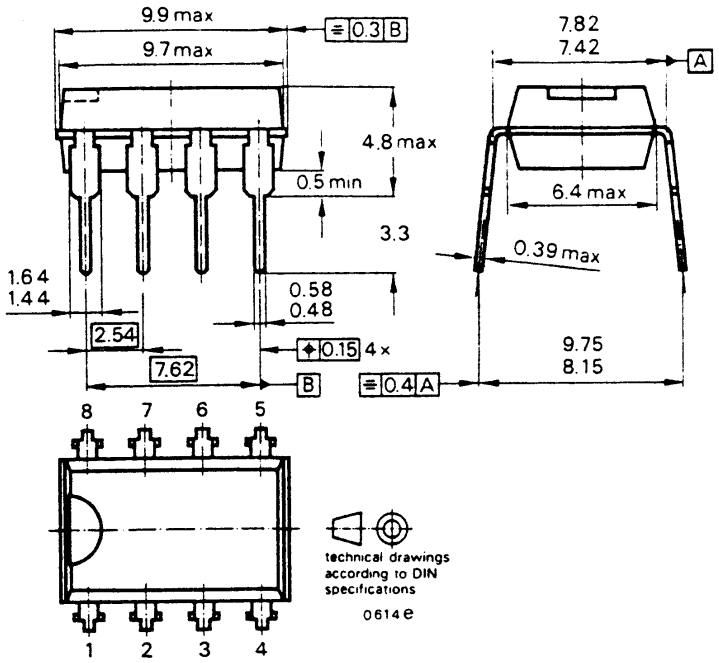


Figure 11. Temperature regulation with proportional range, 10 to 30 °C/ 640 ms ramp cycle

Dimensions in mm

Package: DIP8



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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