

Dual N-Channel 60-V (D-S) MOSFET

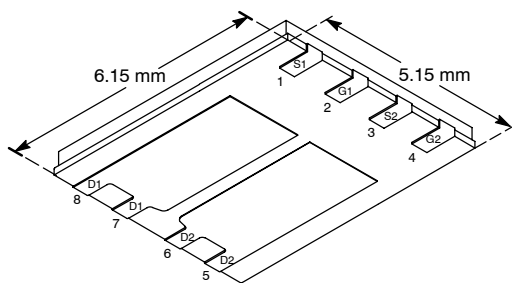
PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
60	0.023 @ $V_{GS} = 10$ V	9.6	43

FEATURES

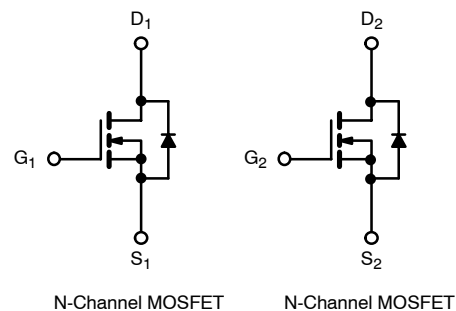
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings
- 100% R_g Tested
- High Threshold Voltage At High Temperature

PowerPAK SO-8



Bottom View

Ordering Information: Si7964DP-T1—E3



N-Channel MOSFET

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ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	60		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	9.6	6.1	A
	$T_A = 70^\circ\text{C}$		7.7	4.9	
Pulsed Drain Current		I_{DM}	40		
Continuous Source Current (Diode Conduction) ^a		I_S	2.9	1.2	
Single Avalanche Current	$L = 0.1$ mH	I_{AS}	25		
Single Avalanche Energy		E_{AS}	31		mJ
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	3.5	1.4	W
	$T_A = 70^\circ\text{C}$		2.2	0.9	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	26	35	$^\circ\text{C/W}$
	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.2	2.7	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

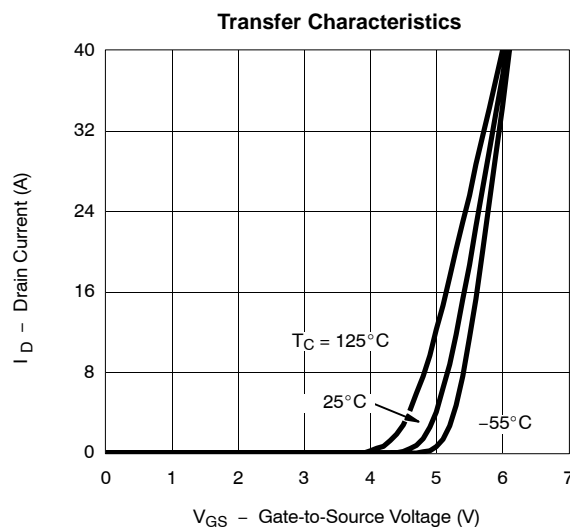
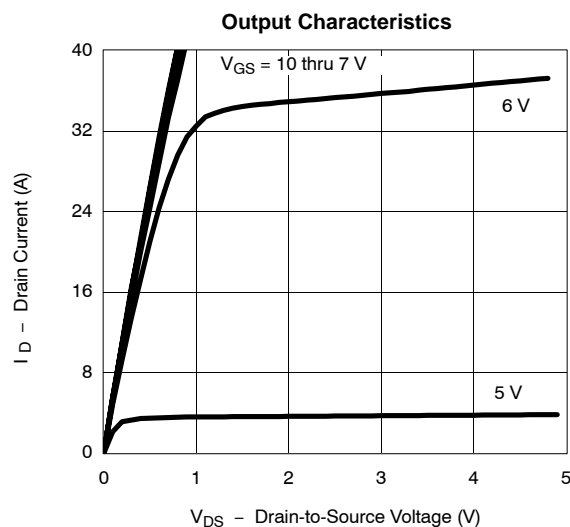
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3.4		4.5	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 9.6 A		0.019	0.023	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 9.6 A		30		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 9.6 A		43	65	nC
Gate-Source Charge	Q _{gs}			15		
Gate-Drain Charge	Q _{gd}			8.5		
Gate Resostamce	R _g	f = 1 MHz	1	2	3	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 20 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω		20	30	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			50	75	
Fall Time	t _f			15	25	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 2.9 A, di/dt = 100 A/μs		35	

Notes

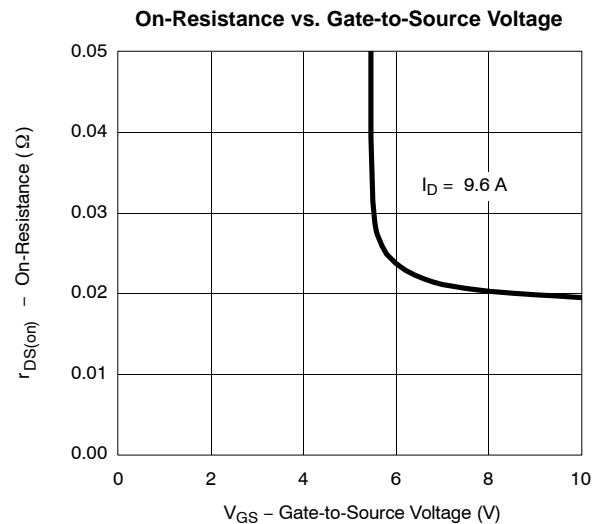
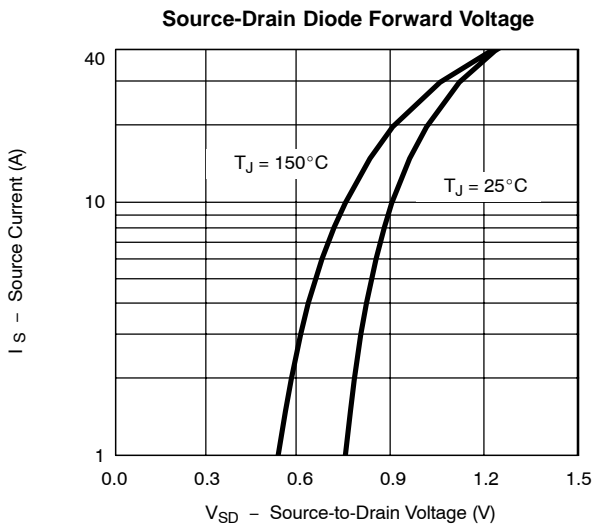
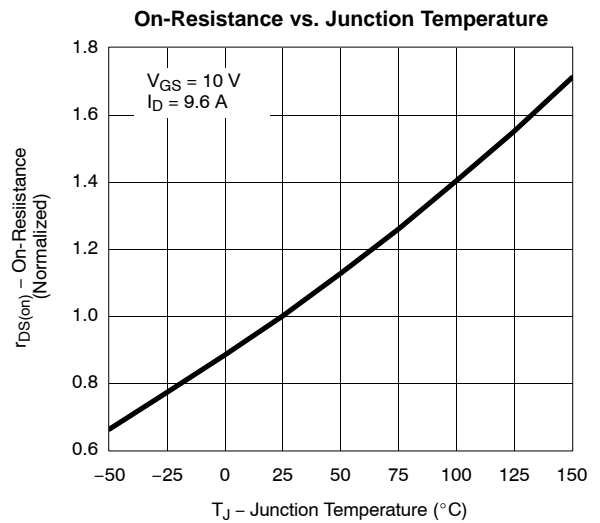
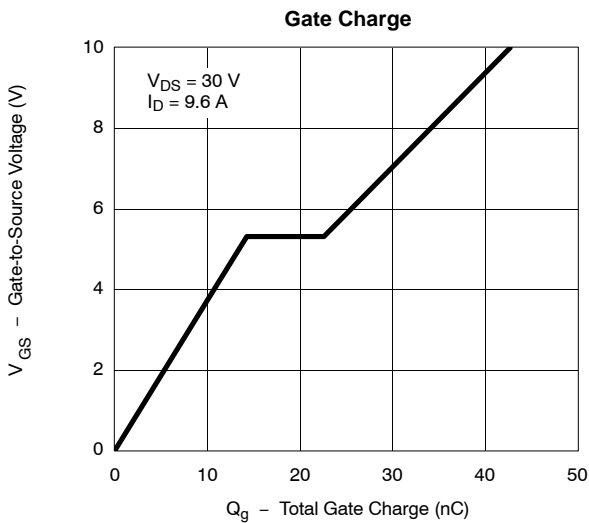
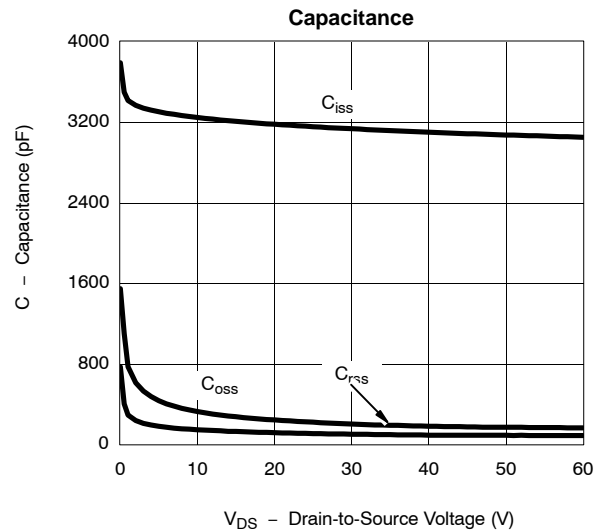
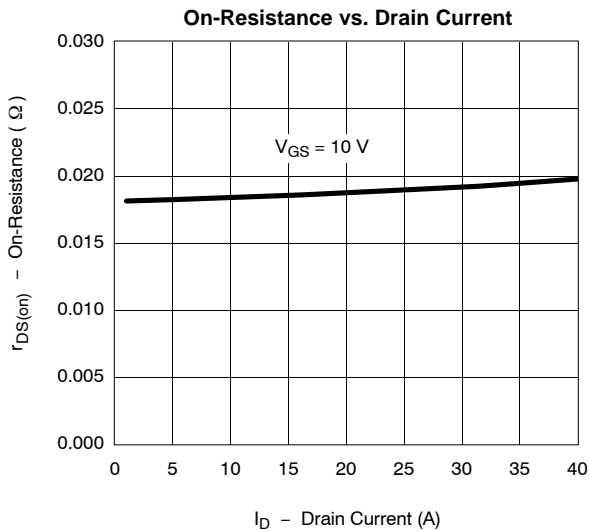
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

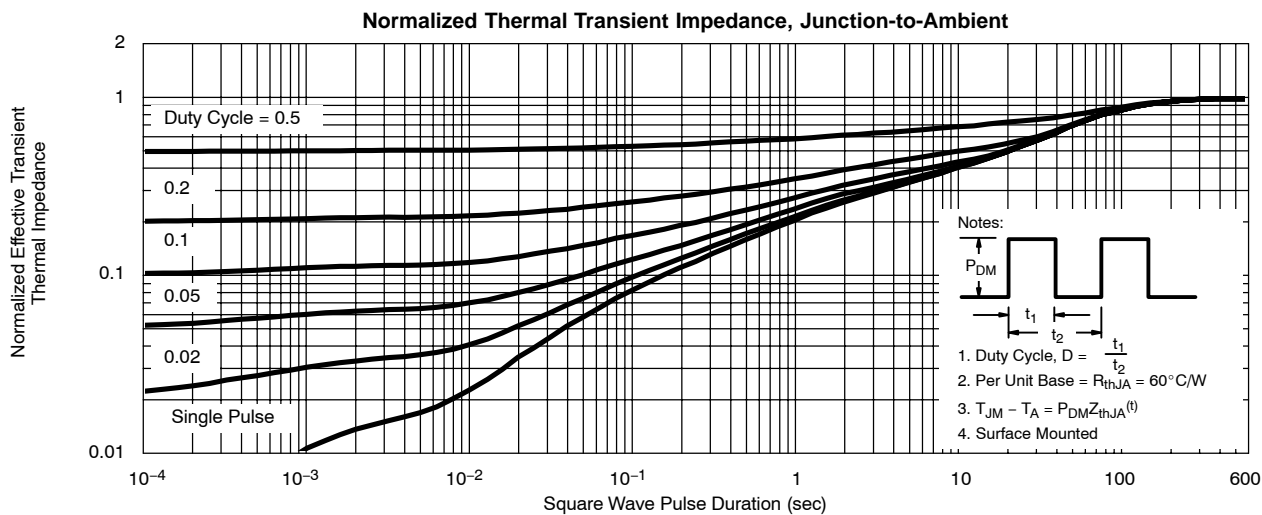
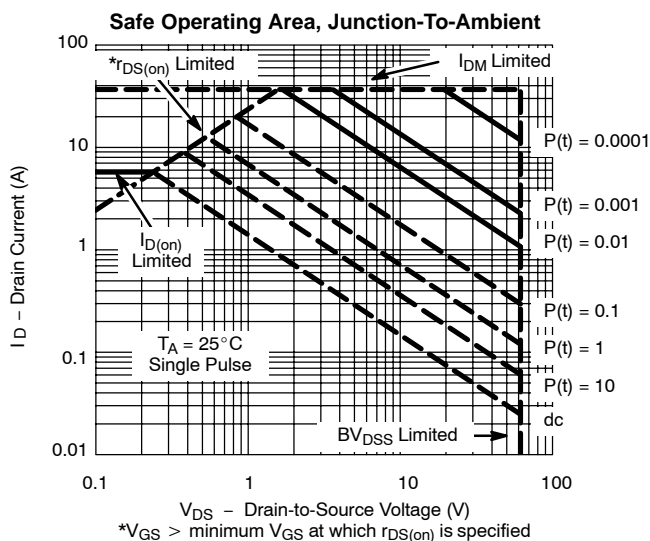
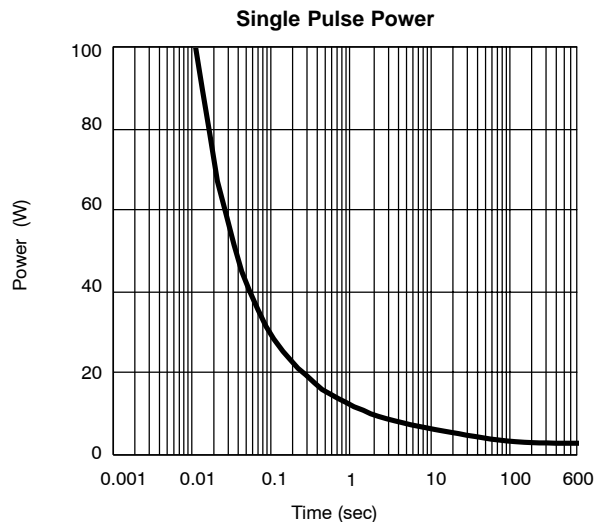
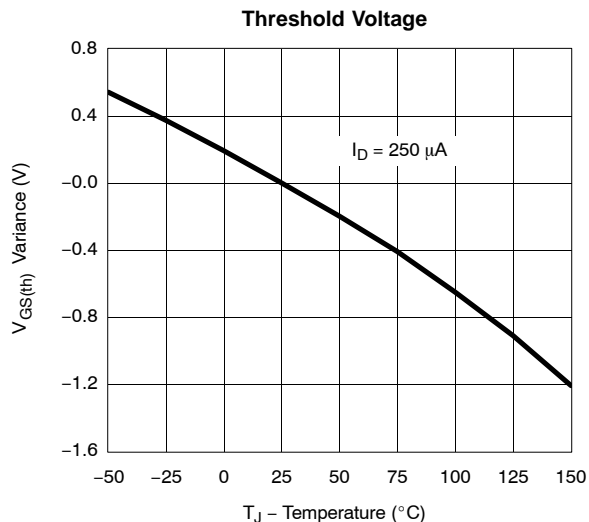
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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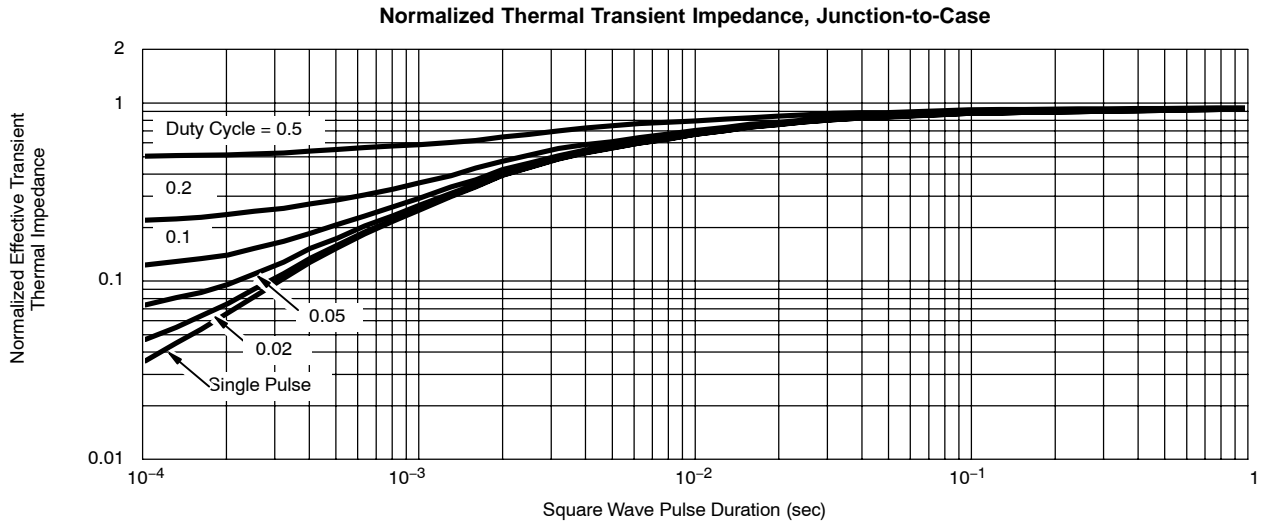


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