

## Dual N-Channel 100-V (D-S) MOSFET

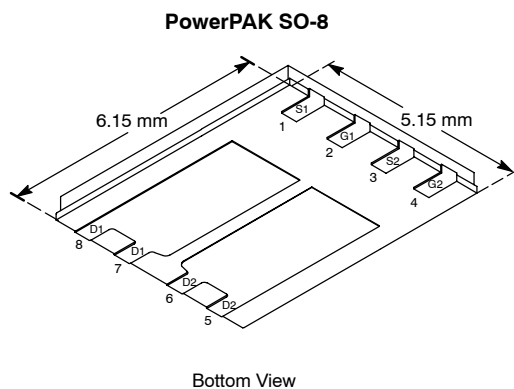
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.049 @ $V_{GS} = 10$ V	5.9
	0.060 @ $V_{GS} = 6$ V	5.5

### FEATURES

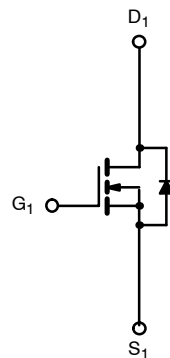
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings

### APPLICATIONS

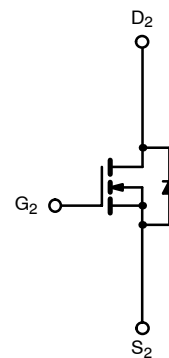
- Synchronous Buck Shoot-Through Resistant
- Optimized for Primary Side Switch



Ordering Information: Si7942DP-T1



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	100		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	5.9	3.8	A
		$T_A = 70^\circ\text{C}$	4.7	3.0	
Pulsed Drain Current	$I_{DM}$	20			
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	2.9	1.2		
Single Avalanche Current	$I_{AS}$	L = 0.1 mH	20		
Single Avalanche Energy			$E_{AS}$	20	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	3.5	1.4	W
		$T_A = 70^\circ\text{C}$	2.2	0.9	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	26	35	$^\circ\text{C}/\text{W}$
		Steady State	60	85	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	2.2	2.7		

Notes

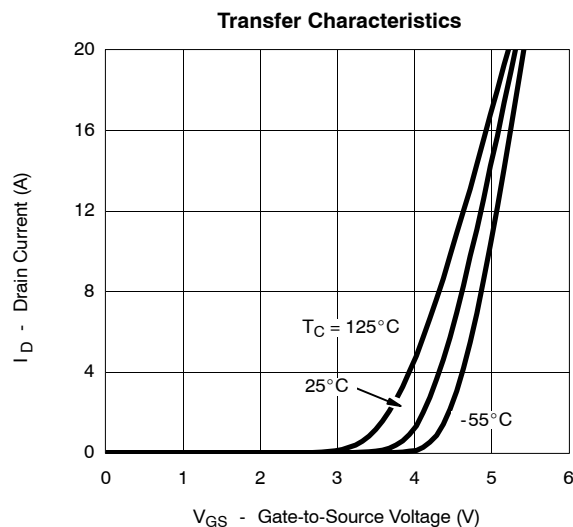
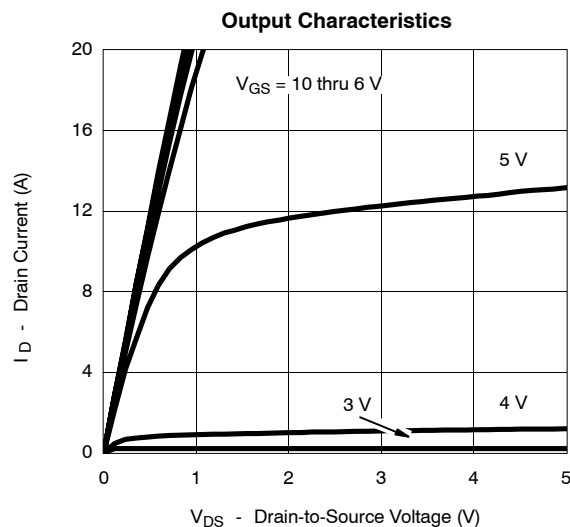
a. Surface Mounted on 1" x 1" FR4 Board.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

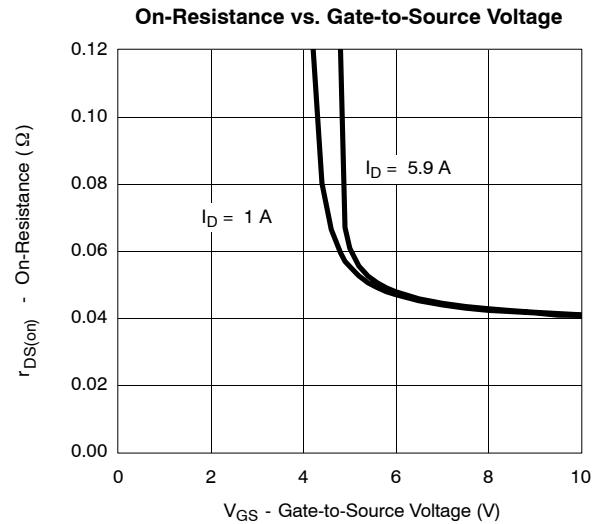
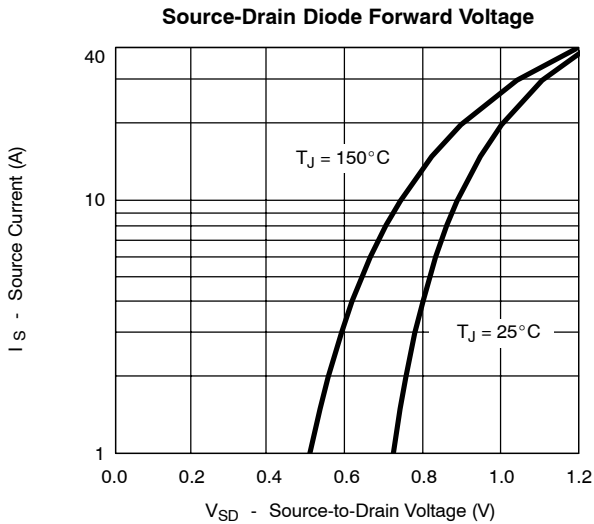
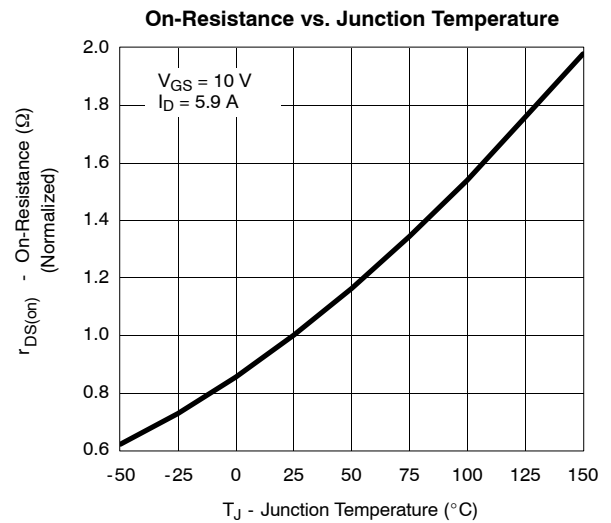
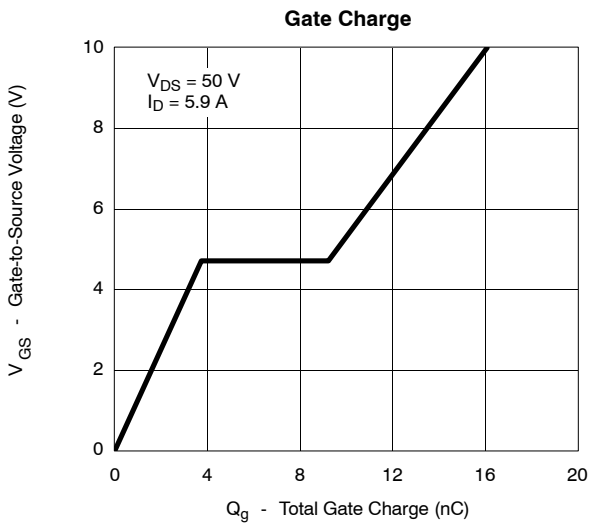
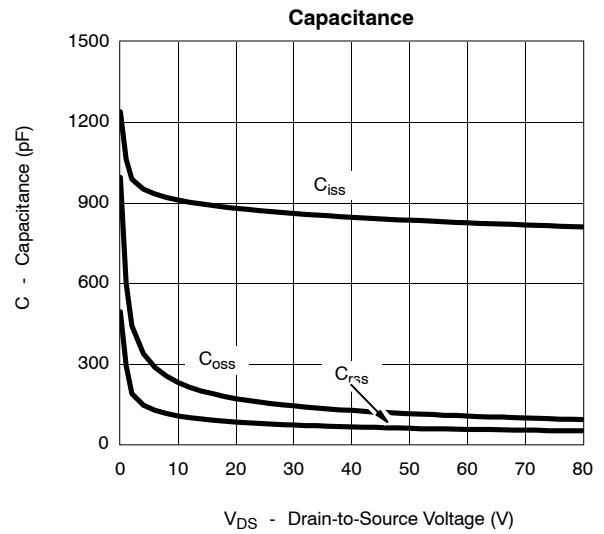
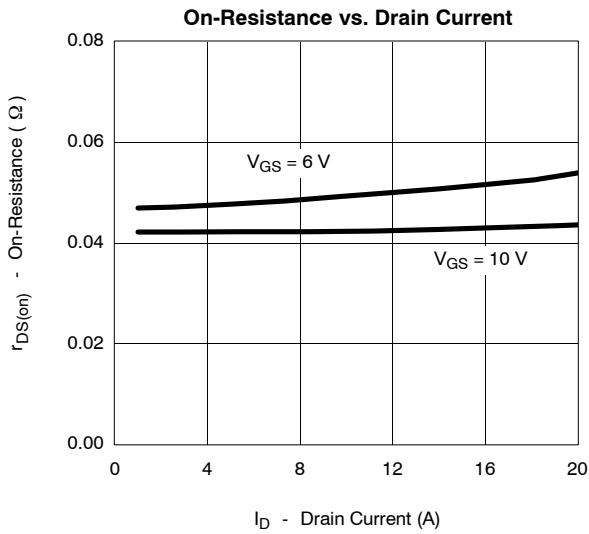
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	20			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.9 A		0.041	0.049	Ω
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 5.5 A		0.048	0.060	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5.9 A		14		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.9 A, V <sub>GS</sub> = 0 V		0.77	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.9 A		16	24	nC
Gate-Source Charge	Q <sub>gs</sub>			3.8		
Gate-Drain Charge	Q <sub>gd</sub>			5.5		
Gate Resostance	R <sub>g</sub>			2.2		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 50 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		15	25	ns
Rise Time	t <sub>r</sub>			15	25	
Turn-Off Delay Time	t <sub>d(off)</sub>			35	55	
Fall Time	t <sub>f</sub>			20	30	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.9 A, di/dt = 100 A/μs		50	75	

## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

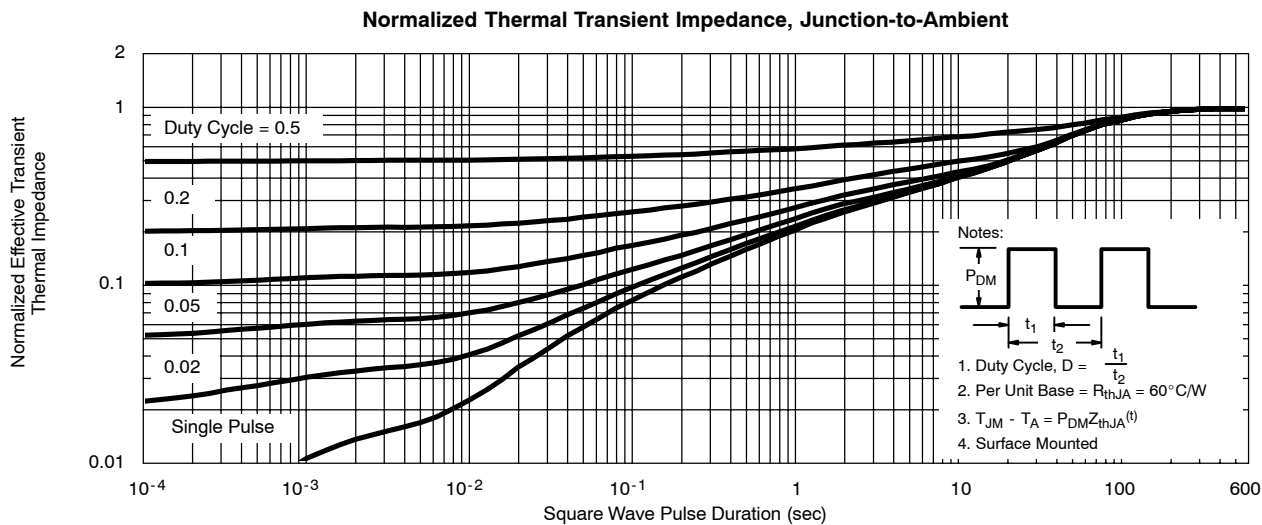
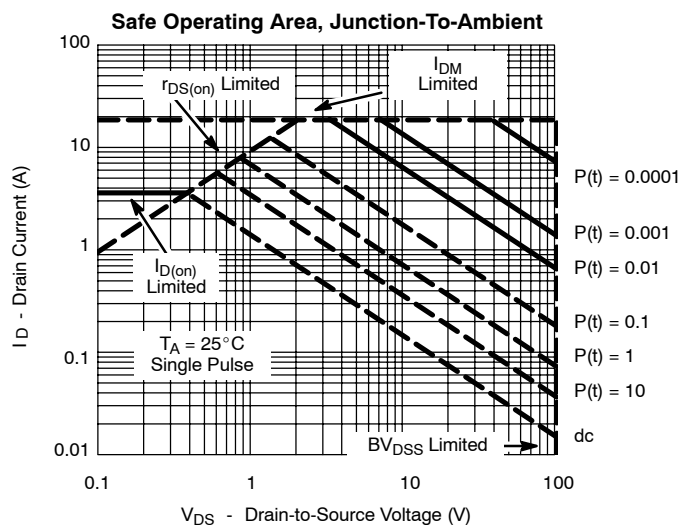
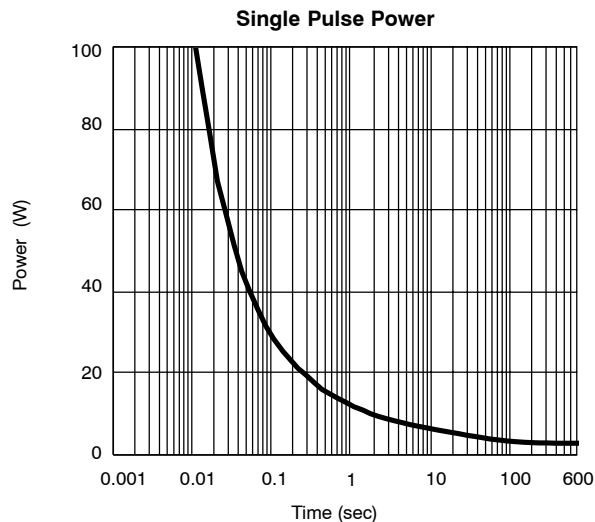
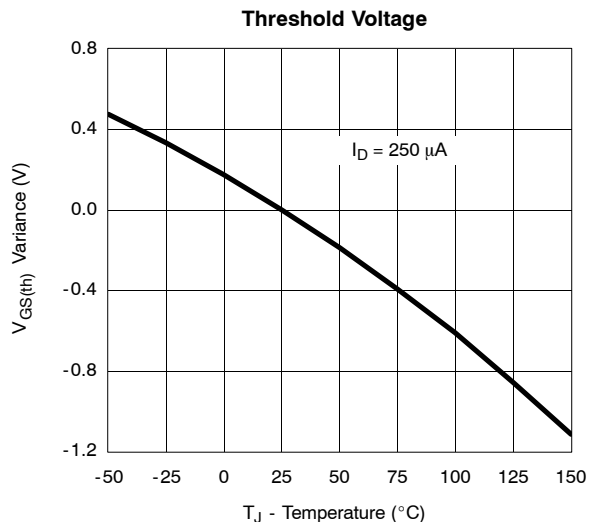
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

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