

Dual N-Channel 12-V (D-S) MOSFET

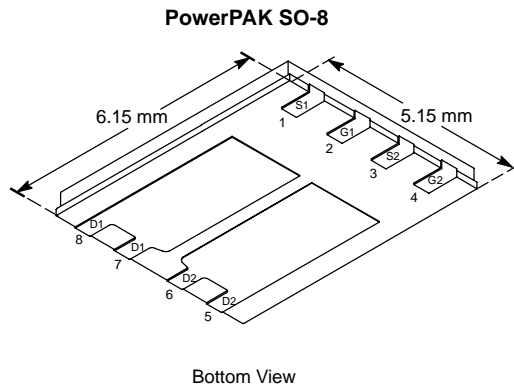
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
12	0.017 @ $V_{GS} = 4.5$ V	11.8
	0.025 @ $V_{GS} = 2.5$ V	9.8

FEATURES

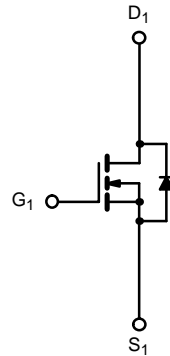
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized
- 100% R_g Tested

APPLICATIONS

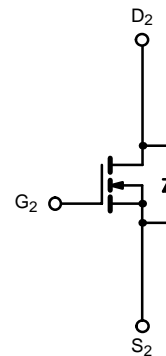
- Point-of-Load Synchronous Rectifier
 - 5-V or 3.3-V BUS Step Down
 - Q_g Optimized for 500-kHz + Operation
- Synchronous Buck Shoot-Through Resistant



Ordering Information: Si7940DP-T1



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	12		V	
Gate-Source Voltage	V_{GS}	± 8			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	11.8	7.6	A
		$T_A = 70^\circ\text{C}$	9.5	6.1	
Pulsed Drain Current	I_{DM}	20			
Continuous Source Current (Diode Conduction) ^a	I_S	2.9	1.1		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.5	1.4	W
		$T_A = 70^\circ\text{C}$	2.2	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	35	$^\circ\text{C/W}$
		Steady State	60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	3.9	5.5		

Notes

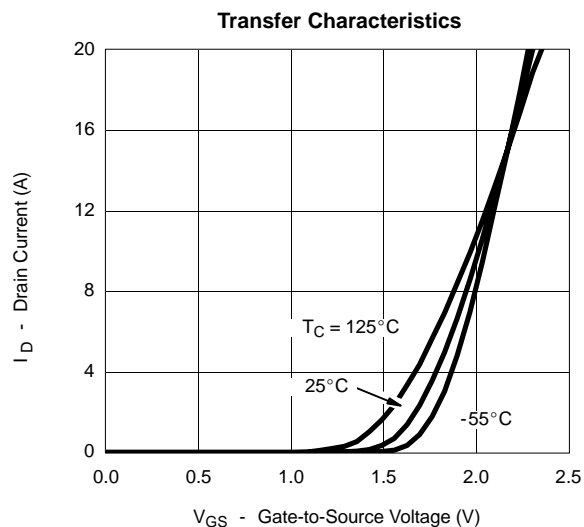
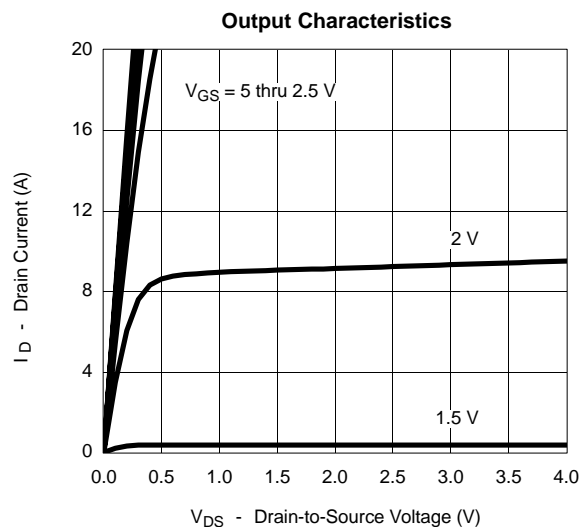
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6		1.5	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 9.6 V, V _{GS} = 0 V			1	μA
		V _{DS} = 9.6 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 11.8 A		0.014	0.017	Ω
		V _{GS} = 2.5 V, I _D = 9.8 A		0.020	0.025	
Forward Transconductance ^a	g _{fs}	V _{DS} = 5 V, I _D = 11.8 A		32		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.77	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 11.8 A		11.5	17	nC
Gate-Source Charge	Q _{gs}			3.2		
Gate-Drain Charge	Q _{gd}			2.5		
Gate Resistance	R _g		0.5		2.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 6 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		30	45	ns
Rise Time	t _r			50	75	
Turn-Off Delay Time	t _{d(off)}			60	90	
Fall Time	t _f			25	40	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, di/dt = 100 A/μs		40	80	

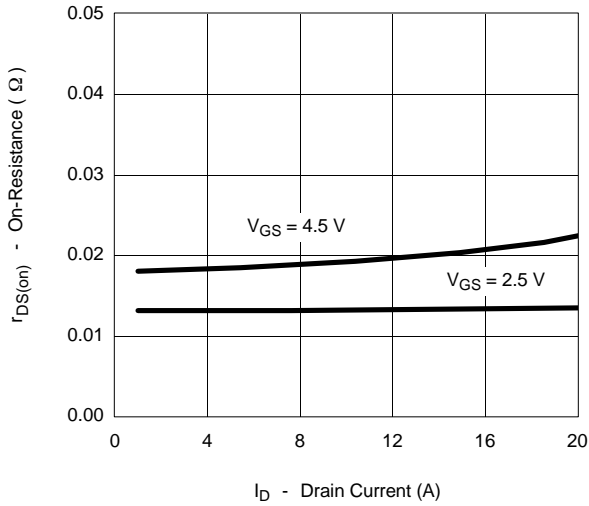
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

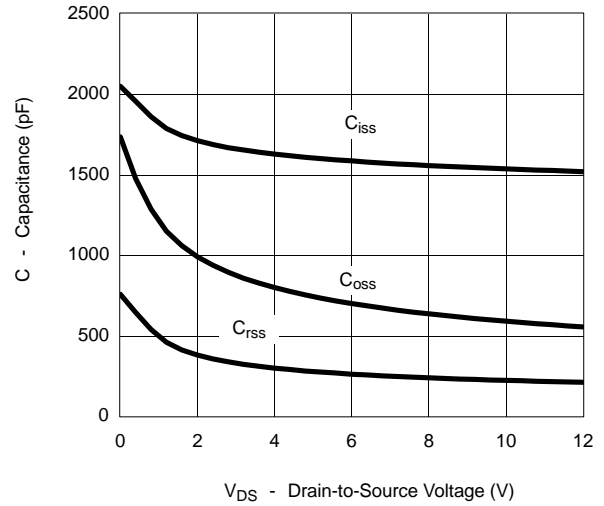
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

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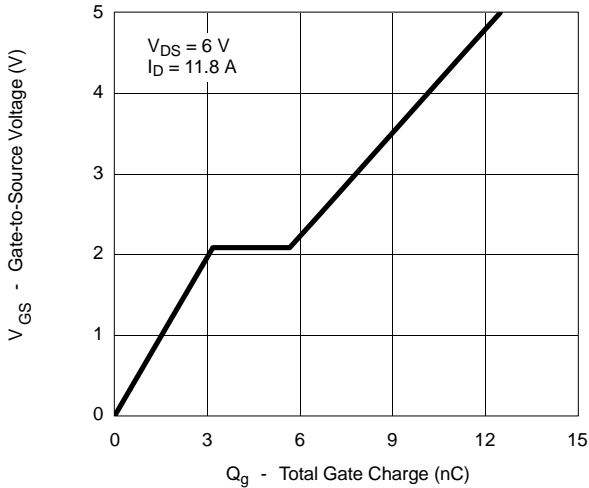
On-Resistance vs. Drain Current



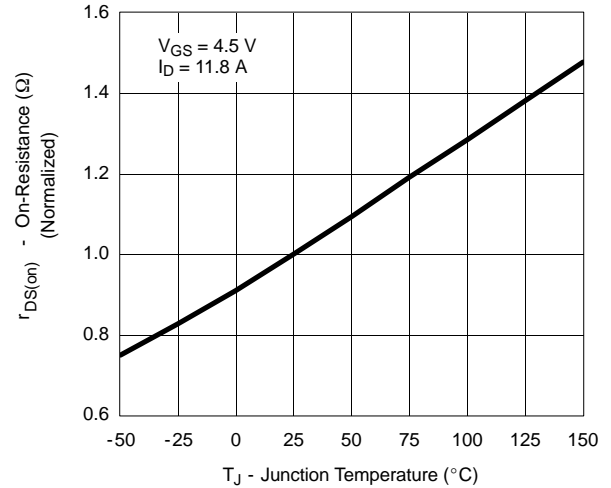
Capacitance



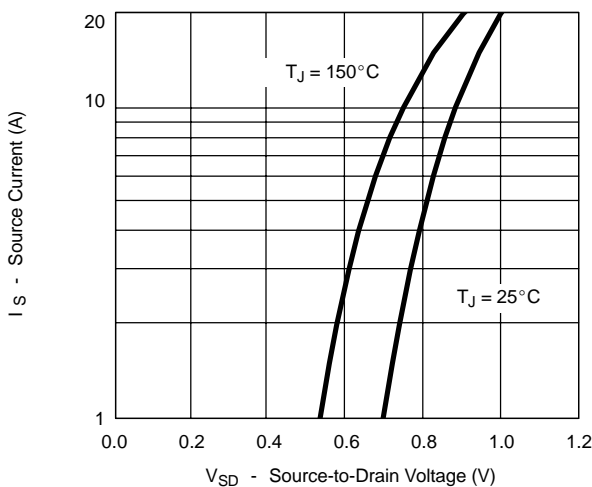
Gate Charge



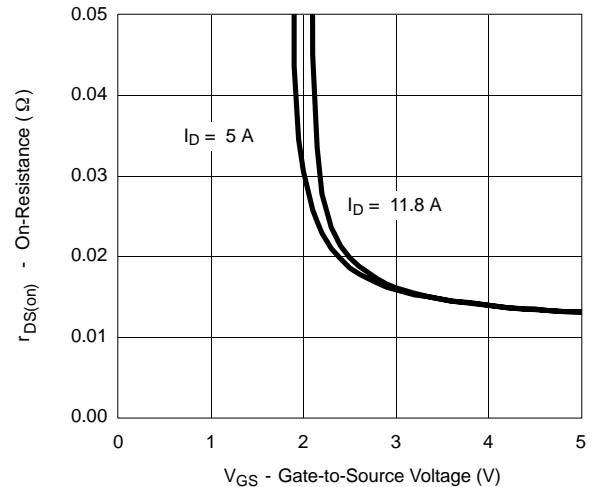
On-Resistance vs. Junction Temperature



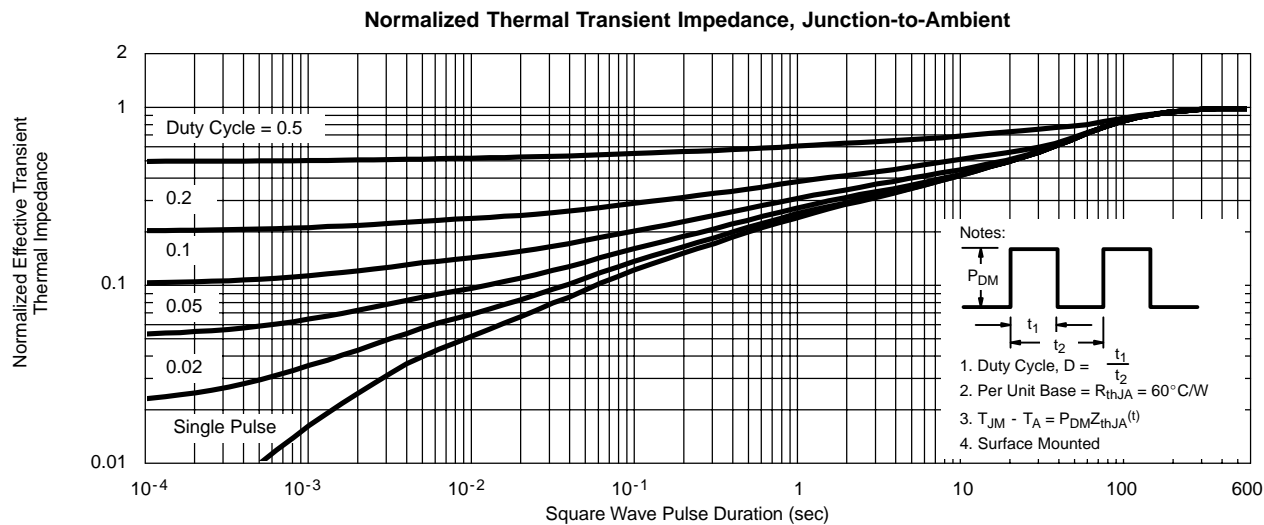
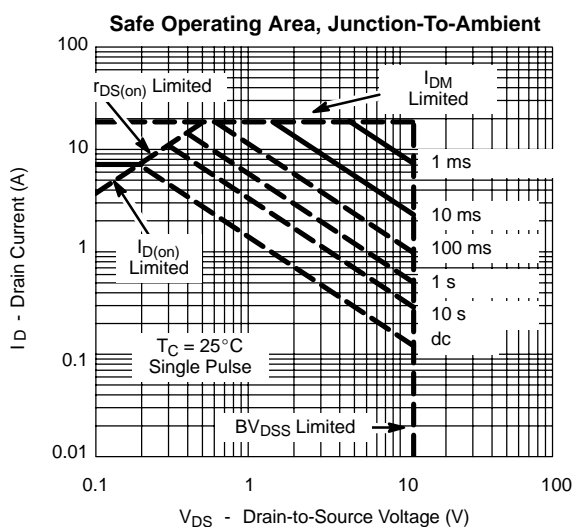
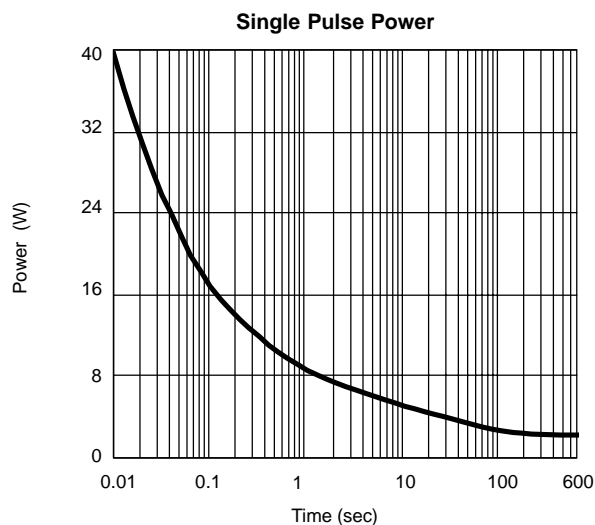
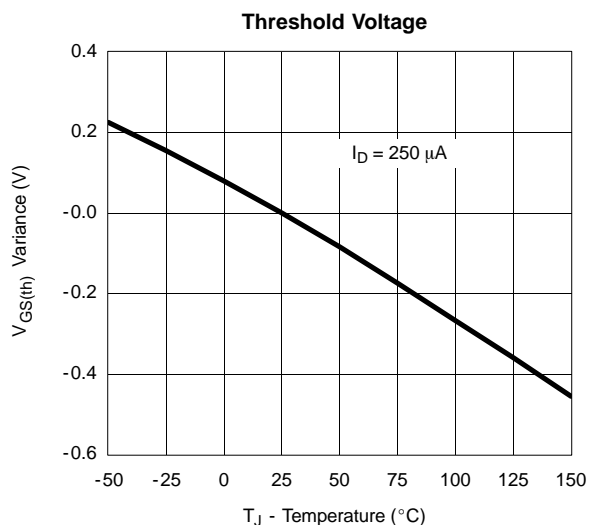
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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