Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.195 @ V_{GS} = 10 V	2.5
	0.230 @ V_{GS} = 6 V	2.3

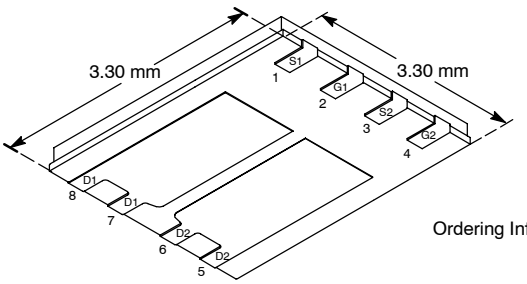
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package, $^1/_3$ the Space of An SO-8 While Thermally Comparable
- PWM Optimized

APPLICATIONS

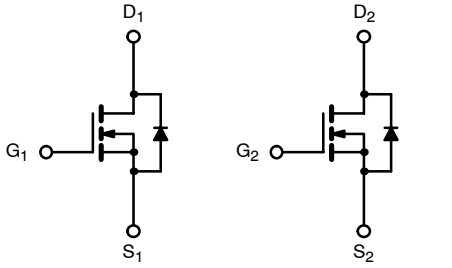
- DC/DC Primary-Side Switch
- 48-V Battery Monitoring

PowerPAK 1212-8



Bottom View

Ordering Information: Si7922DN-T1



N-Channel MOSFET N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	100		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	2.5	1.8	A
	T_A = 85°C		1.8	1.3	
Pulsed Drain Current		I_{DM}	10		
Avalanche Current	0.1 mH	I_{AS}	5		
Single Avalanche Energy		E_{AS}	1.25		mJ
Continuous Source Current (Diode Conduction)[a]		I_S	2.2	1.1	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.6	1.3	W
	T_A = 85°C		1.4	0.69	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	38	48	°C/W
	Steady State		77	94	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.3	5.4	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

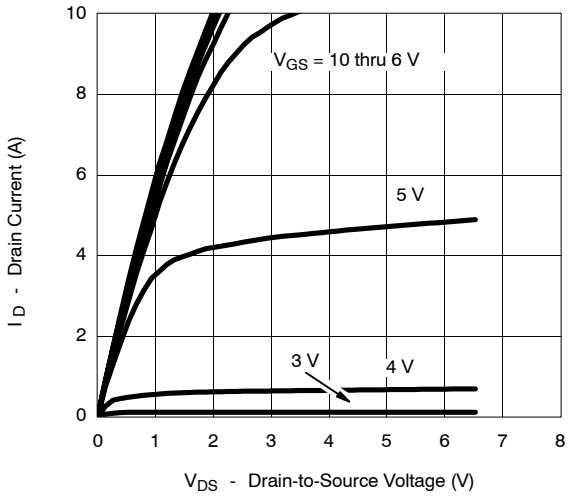
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.5		3.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 85°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	10			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A		0.162	0.195	Ω
		V_{GS} = 6 V, I_D = 2.3 A		0.190	0.230	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 2.5 A		5.3		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.2 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 2.5 A		5.2	8	nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			1.9		
Gate Resistance	R_g			1.7		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 50 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		7	15	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			8	15	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.2 A, di/dt = 100 A/μs		40	80	

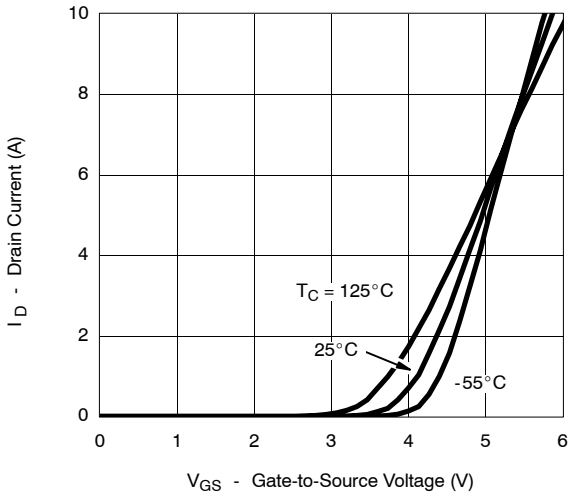
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

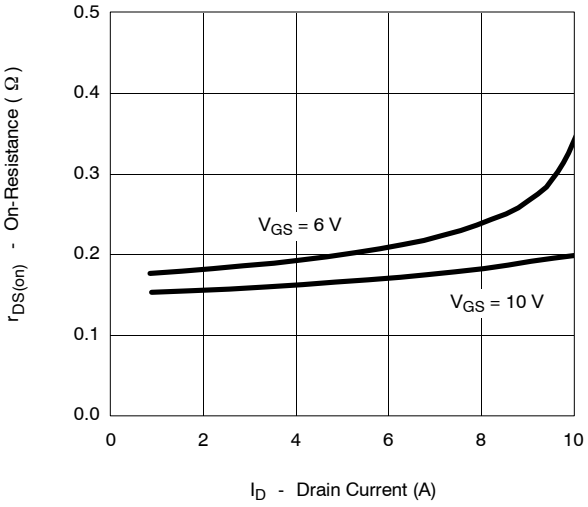


Transfer Characteristics

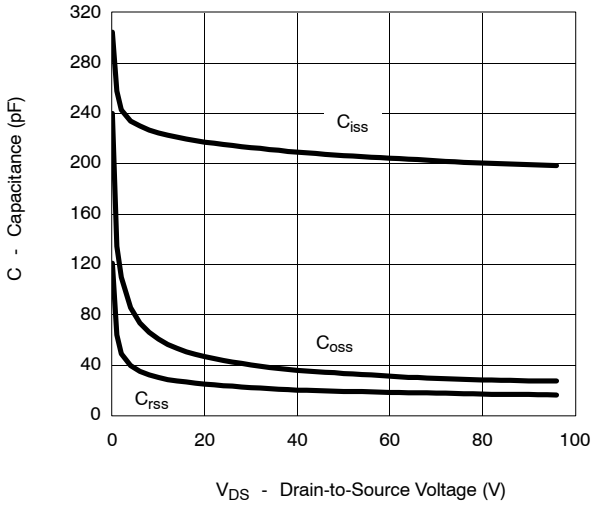


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

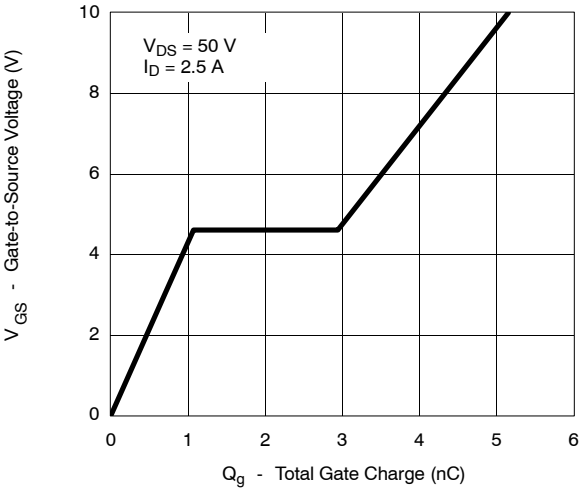
On-Resistance vs. Drain Current



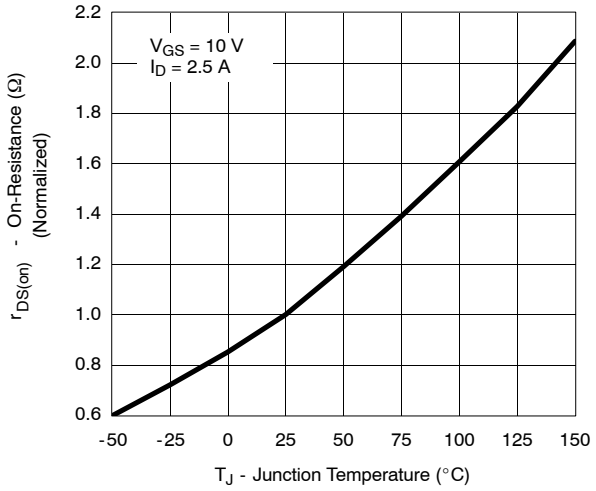
Capacitance



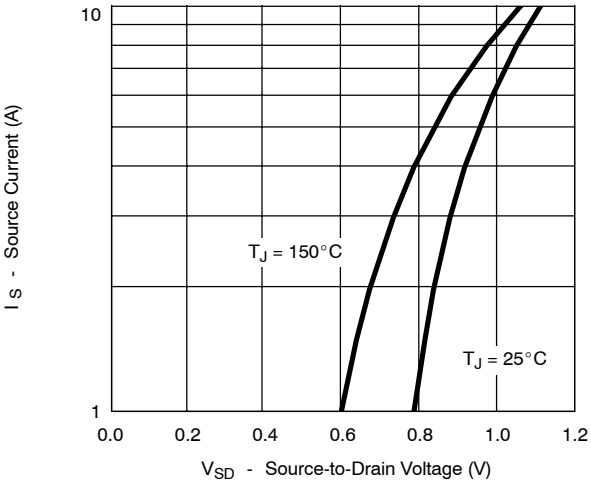
Gate Charge



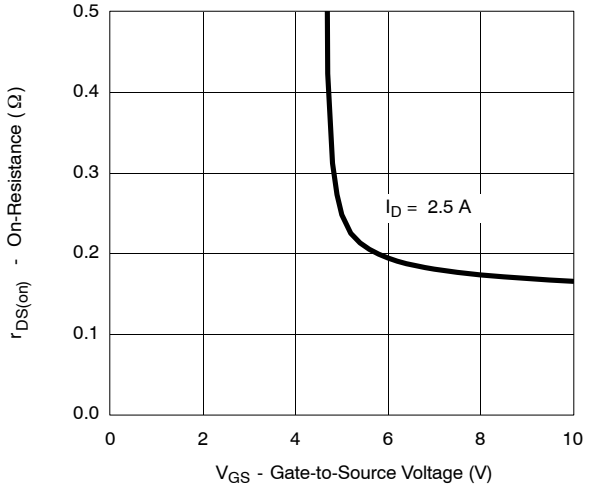
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

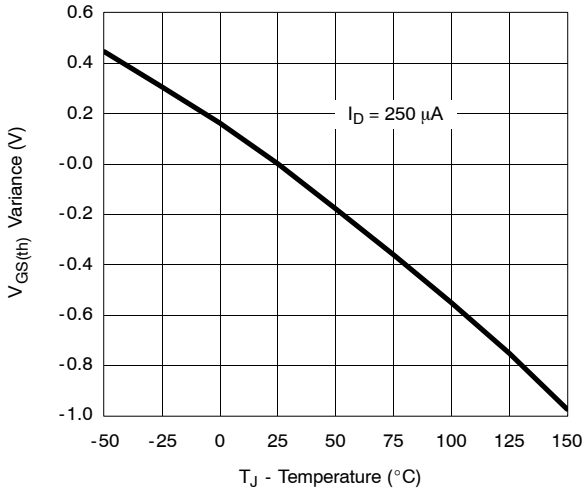


On-Resistance vs. Gate-to-Source Voltage

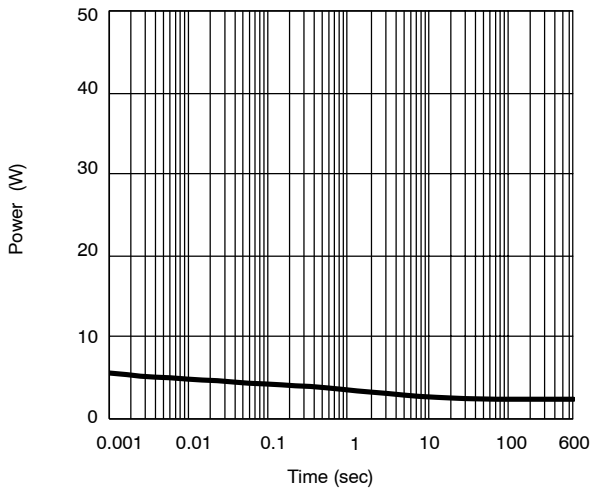


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

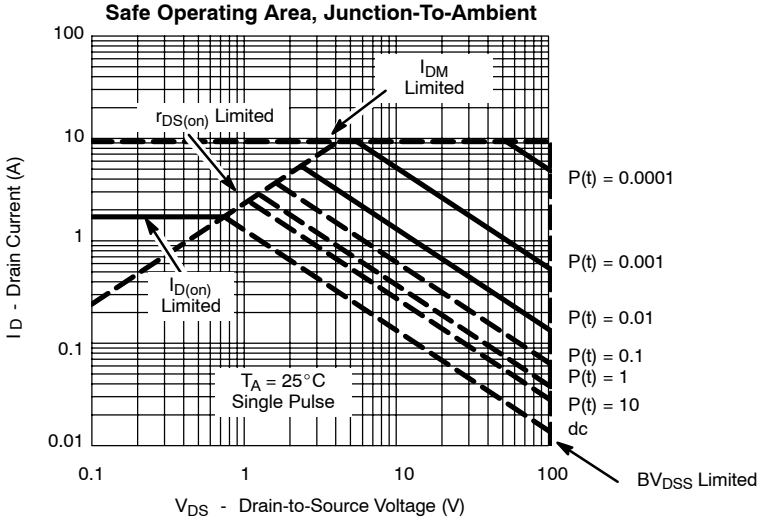
Threshold Voltage



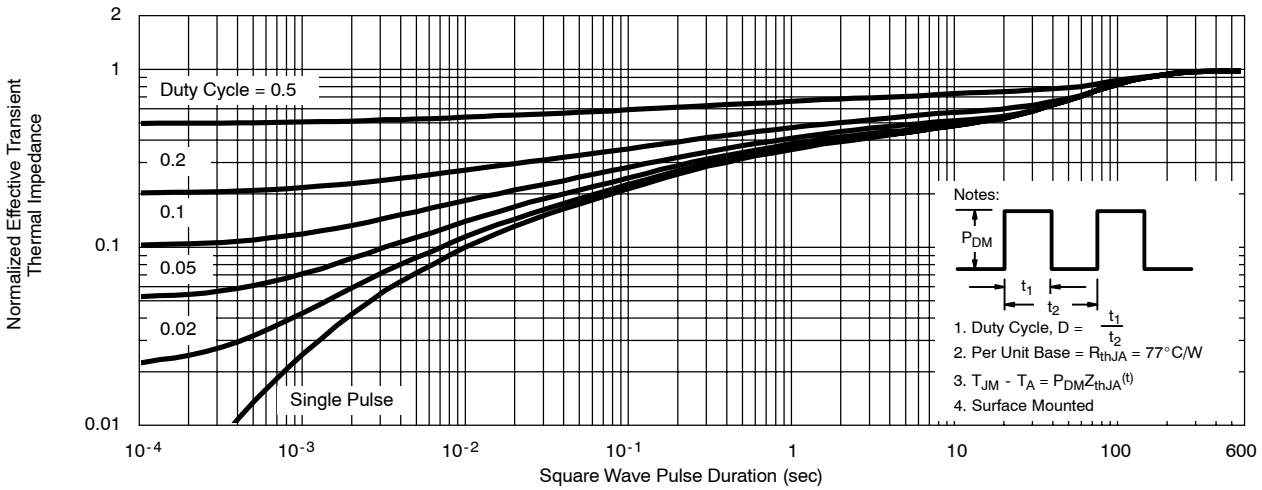
Single Pulse Power



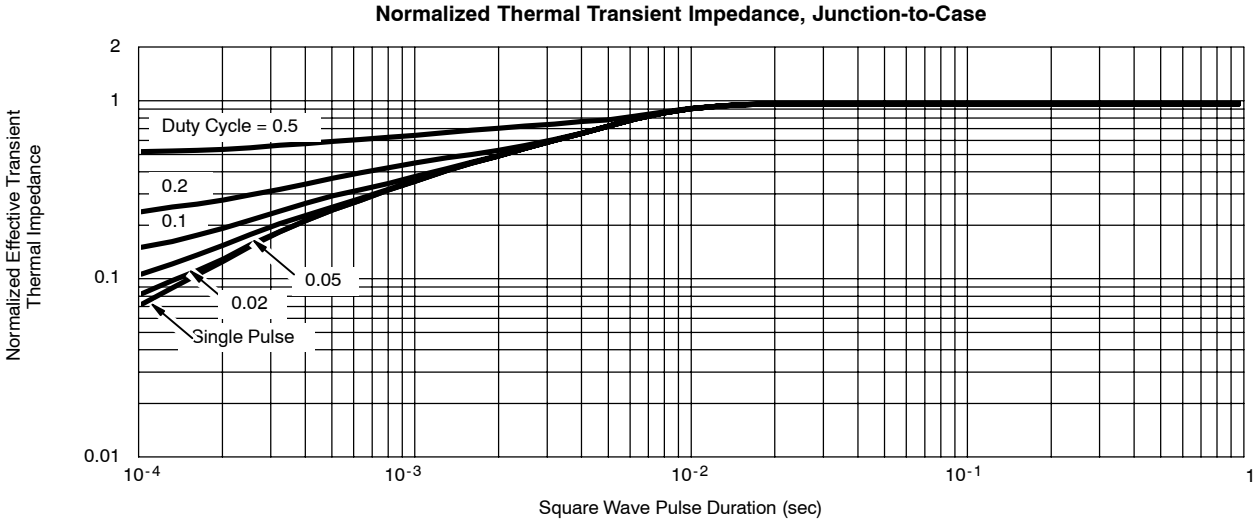
Safe Operating Area, Junction-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



NOTE:

The minimum creepage between D1 and D2 for this 100-V device is 0.2 mm. Please see PowerPAK 1212-8 outline drawing, document # 71656, for more information.