

Dual N-Channel 20-V (D-S) MOSFET, Common Drain

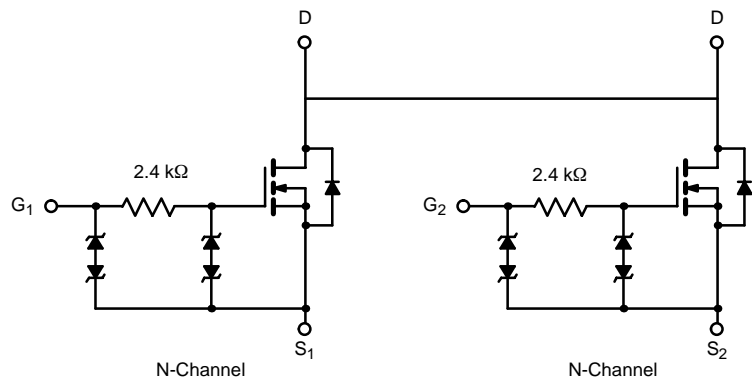
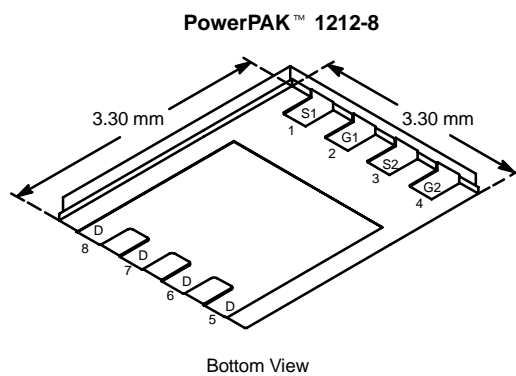
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.026 @ V _{GS} = 4.5 V	9
	0.031 @ V _{GS} = 2.5 V	8
	0.039 @ V _{GS} = 1.8 V	7

FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- New PowerPak™ Package
 - Low-Thermal Resistance, R_{thJC}
 - Low 1.07-mm Profile
- 3000-V ESD Protection

APPLICATIONS

- Protection Switch for 1-2 Li-ion Batteries



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	20		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	9	6	A
		T _A = 85 °C	6.4	4.3	
Pulsed Drain Current	I _{DM}	30			
Continuous Source Current (Diode Conduction) ^a	I _S	2.9	1.4		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.2	1.5	W
		T _A = 85 °C	1.7	0.79	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	30	38	°C/W
		Steady State	65	82	
Maximum Junction-to-Case	R _{thJC}	1.9	2.4		

Notes

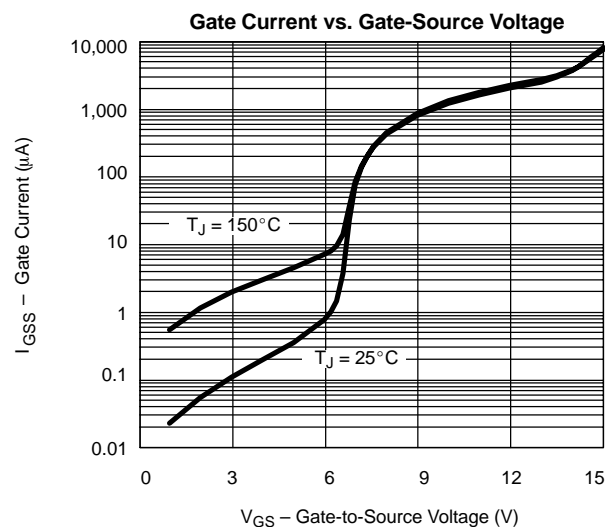
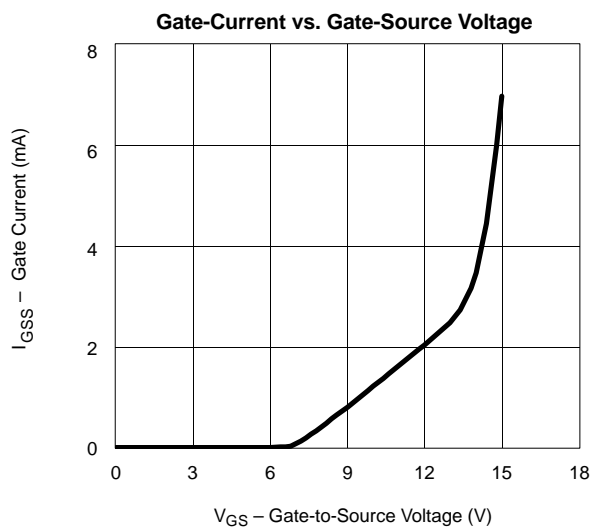
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

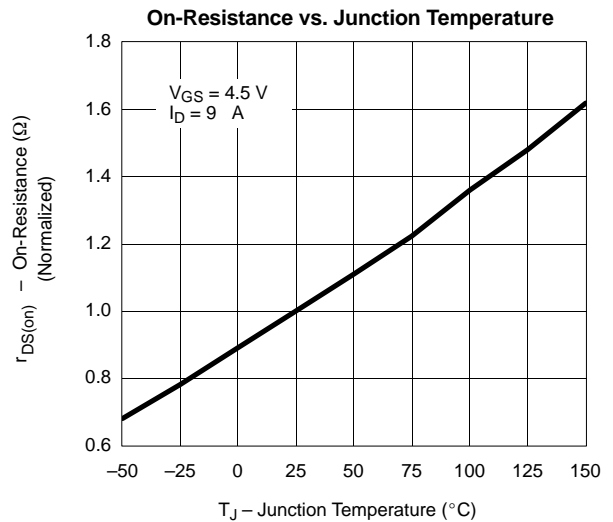
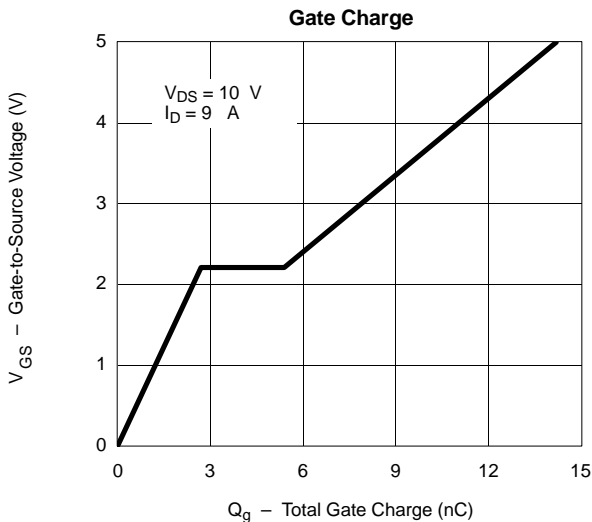
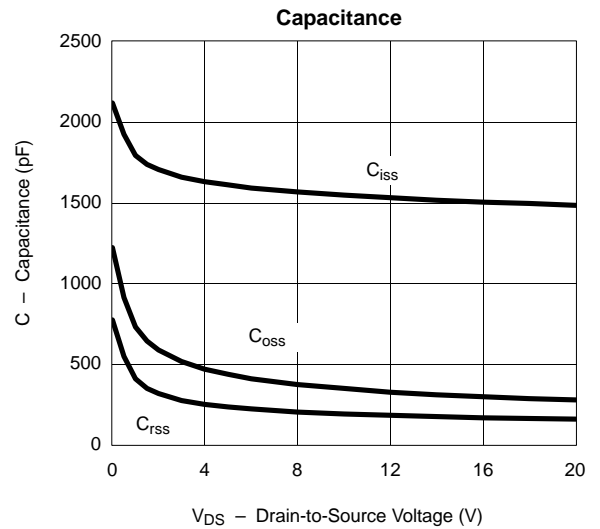
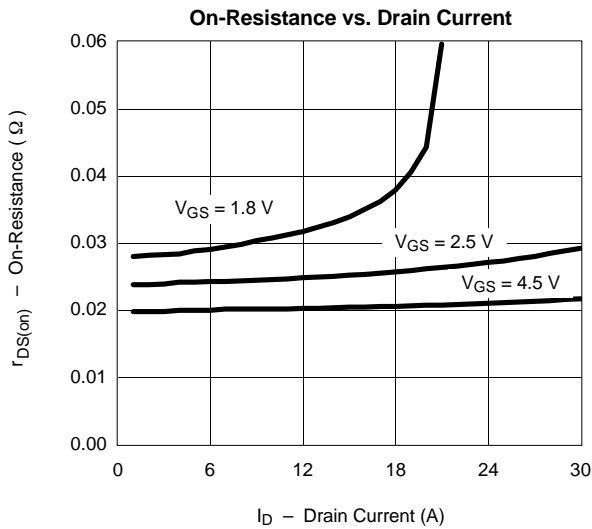
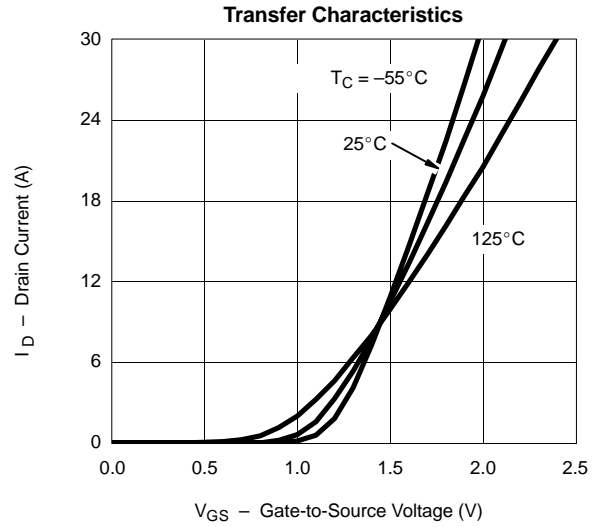
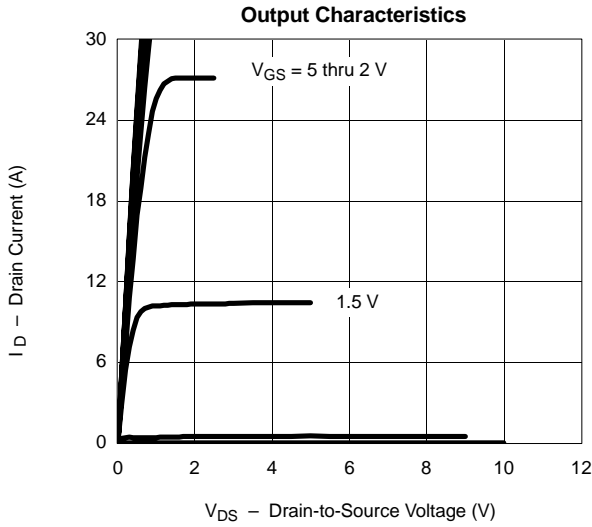
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.40			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 1	μA
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 10	mA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 6.5 \text{ A}$		0.021	0.026	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 5.8 \text{ A}$		0.025	0.031	
		$V_{GS} = 1.8 \text{ V}, I_D = 5.0 \text{ A}$		0.031	0.039	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 6.5 \text{ A}$		25		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.65	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 6.5 \text{ A}$		12.5	18	nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			2.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_G = 6 \Omega$		0.7	1.0	μs
Rise Time	t_r			1.3	2.0	
Turn-Off Delay Time	$t_{d(off)}$			5.5	8.0	
Fall Time	t_f			4.6	7.0	

Notes

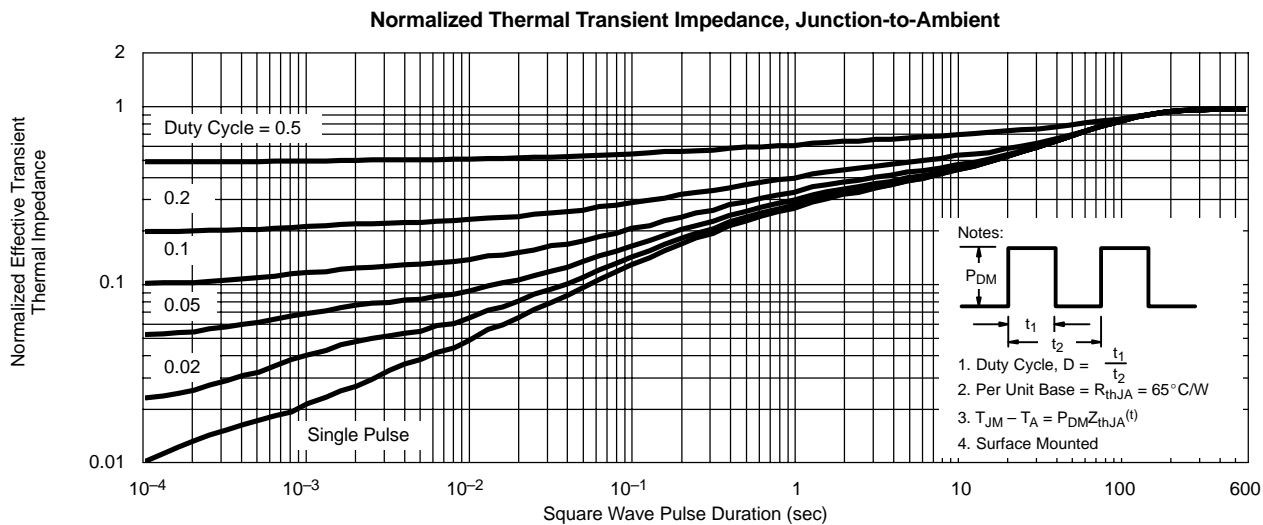
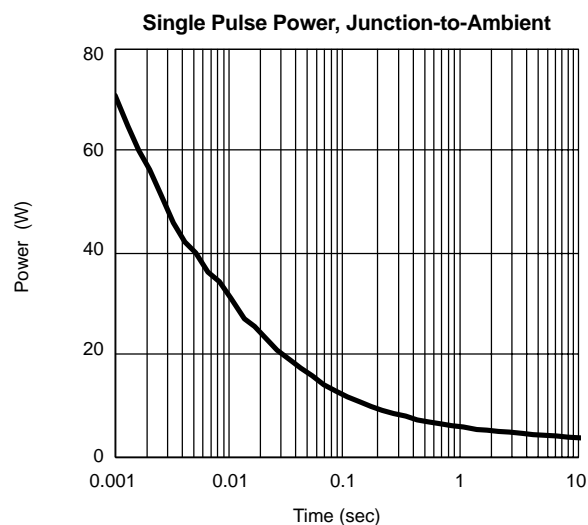
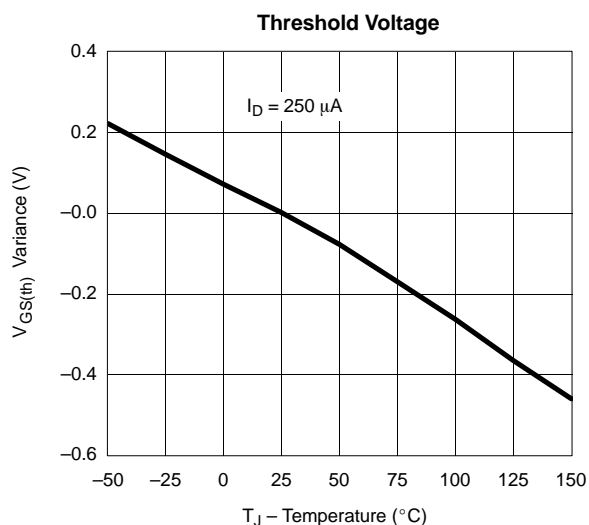
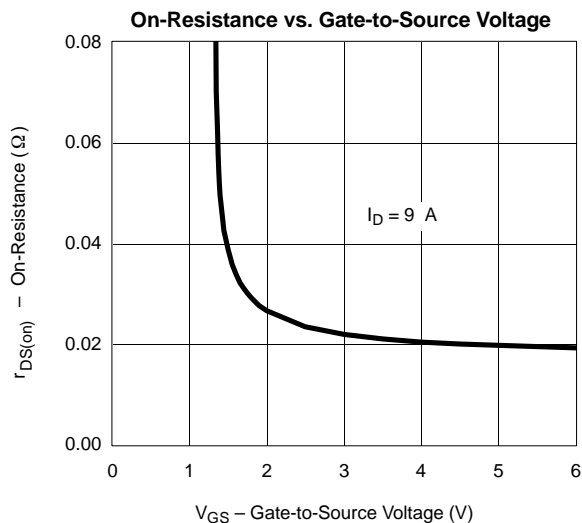
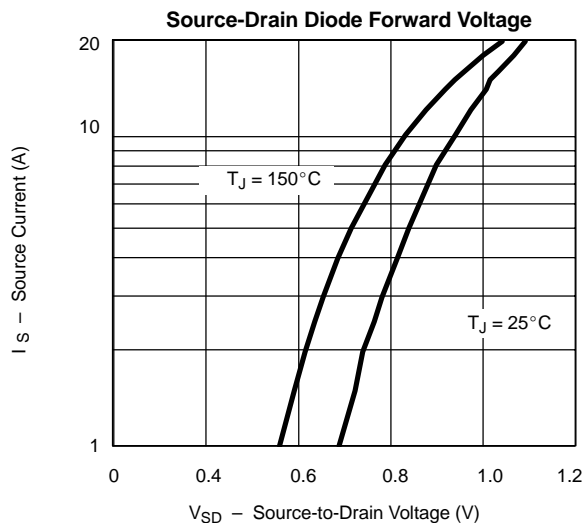
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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