



Dual N-Channel 60-V (D-S) MOSFET

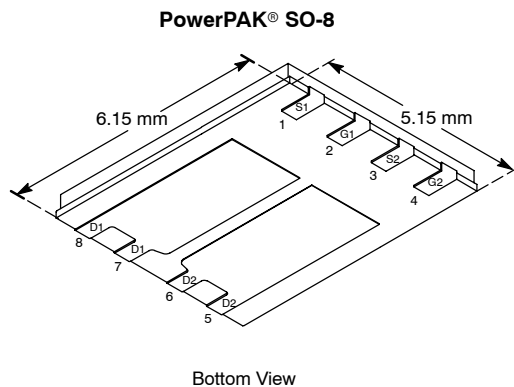
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.075 @ $V_{GS} = 10$ V	4.6
	0.100 @ $V_{GS} = 4.5$ V	4.0

FEATURES

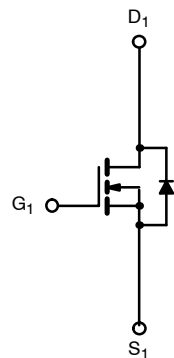
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings

APPLICATIONS

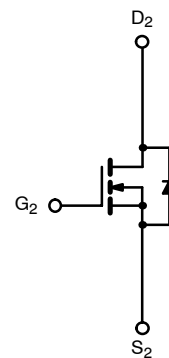
- Automotive
 - ABS
 - Coil Driver
 - Load Switch



Bottom View
Ordering Information: Si7948DP-T1



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	60		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	4.6	3.0	A
		$T_A = 70^\circ\text{C}$	3.6	2.4	
Pulsed Drain Current	I_{DM}	15			
Continuous Source Current (Diode Conduction) ^a	I_S	2.7	1.2		
Single Avalanche Current	I_{AS}	15			
Single Avalanche Energy	E_{AS}	11		mJ	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.3	1.4	W
		$T_A = 70^\circ\text{C}$	2.1	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	29	38	$^\circ\text{C}/\text{W}$
		Steady State	60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	4.0	5.2		

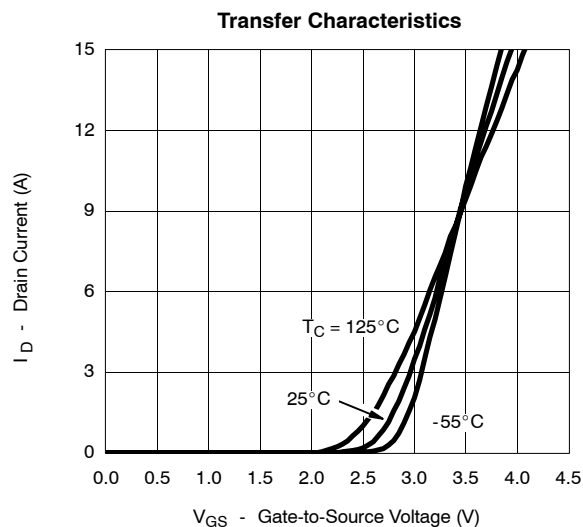
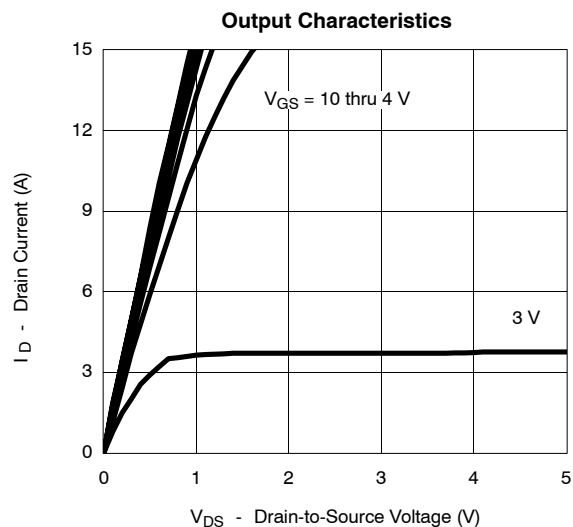
Notes
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	15			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.6 A		0.060	0.075	Ω
		V _{GS} = 4.5 V, I _D = 4.0 A		0.080	0.100	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.6 A		6		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.7 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 15 A		12	20	nC
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			3.5		
Gate Resostance	R _g			1.5		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 2 Ω I _D ≅ 15 A, V _{GEN} = 10 V, R _G = 2.5 Ω		7	20	ns
Rise Time	t _r			8	25	
Turn-Off Delay Time	t _{d(off)}			15	40	
Fall Time	t _f			7	20	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.7 A, di/dt = 100 A/μs		30	60	

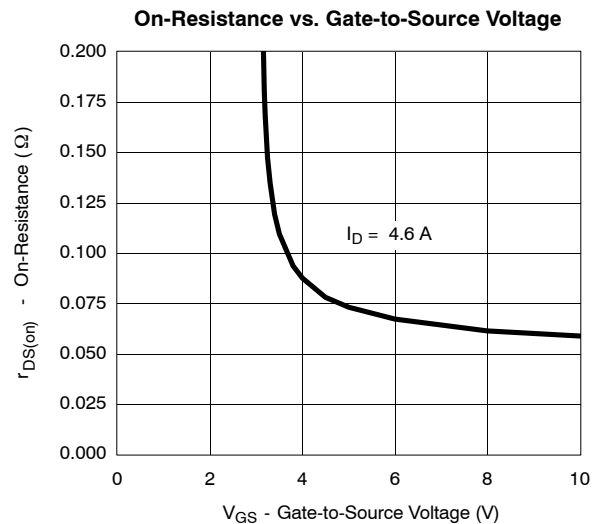
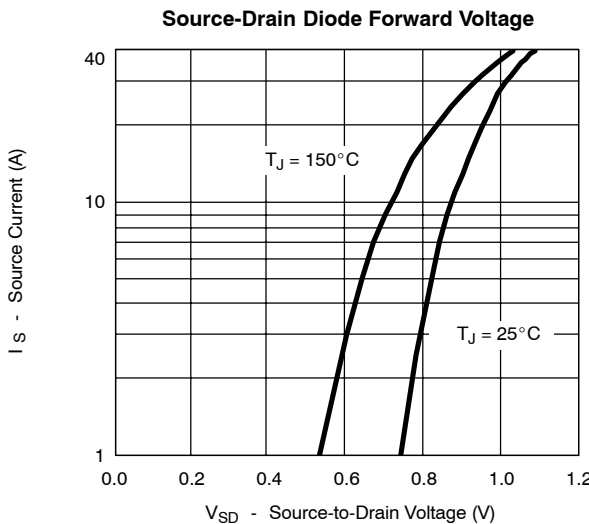
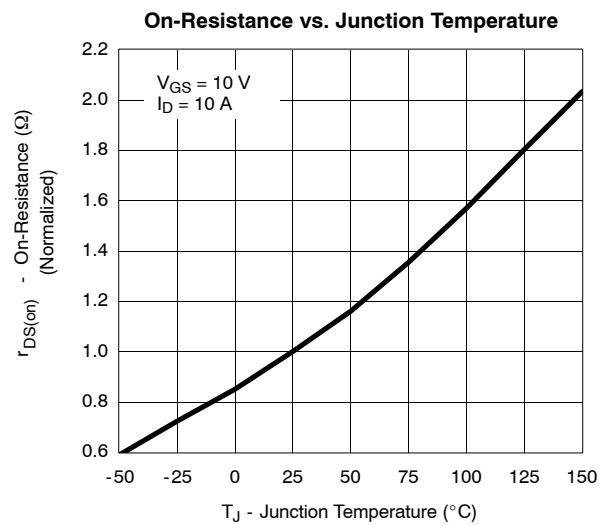
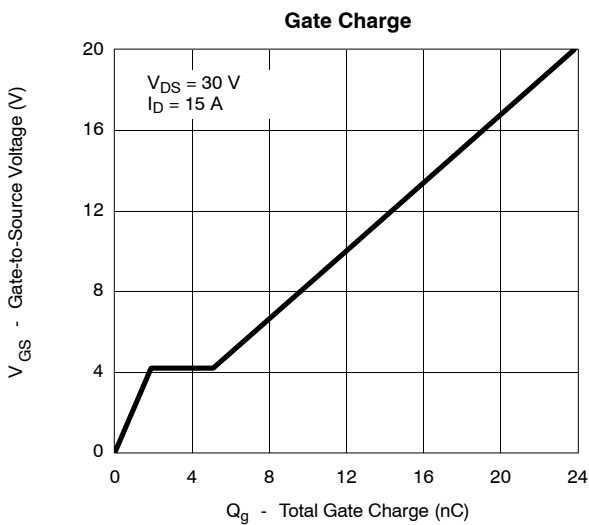
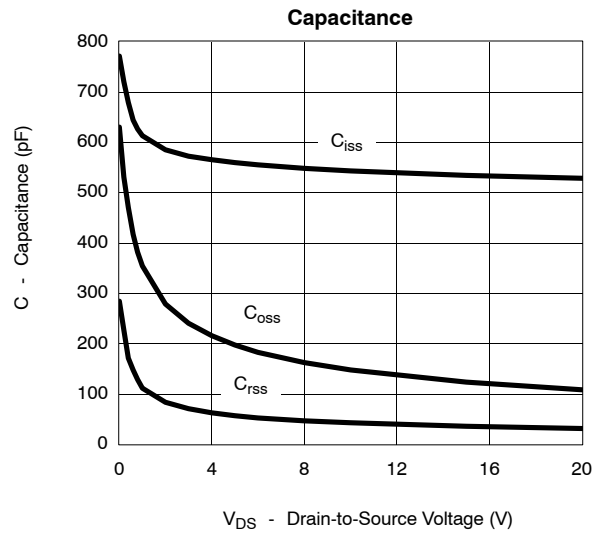
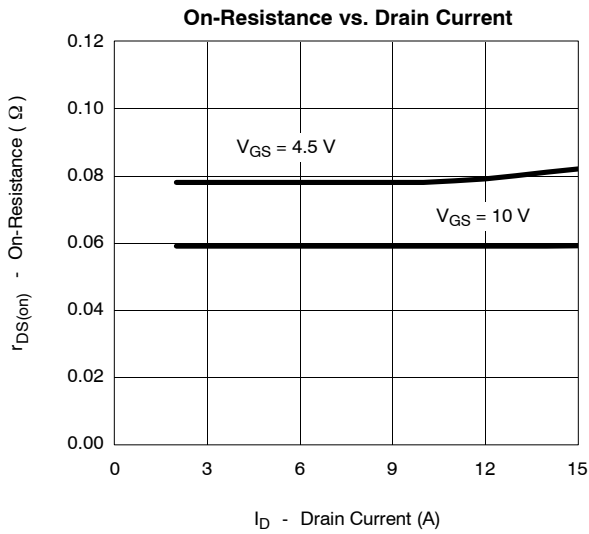
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

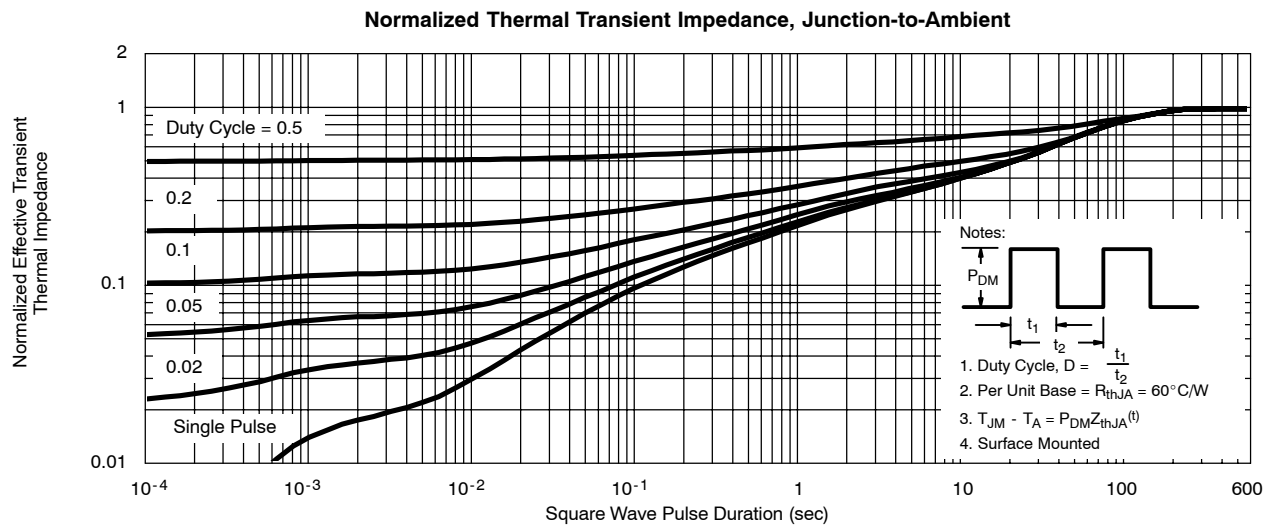
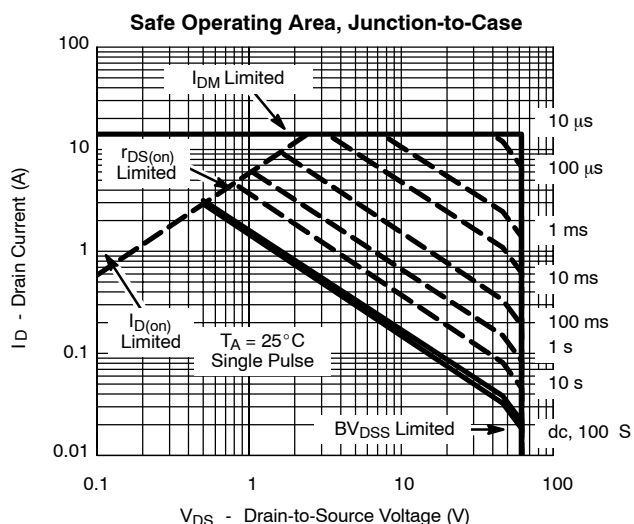
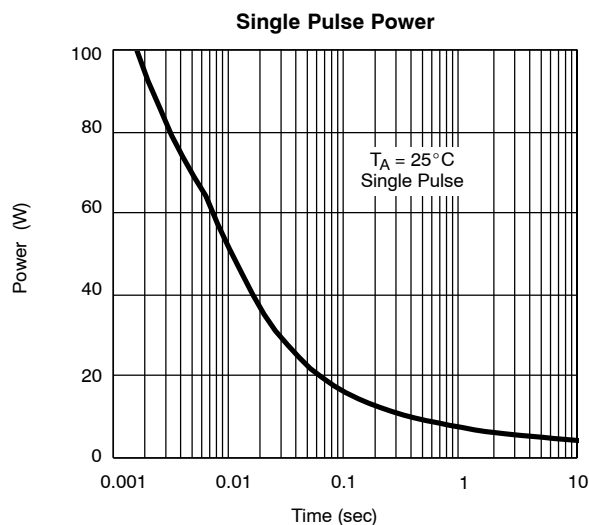
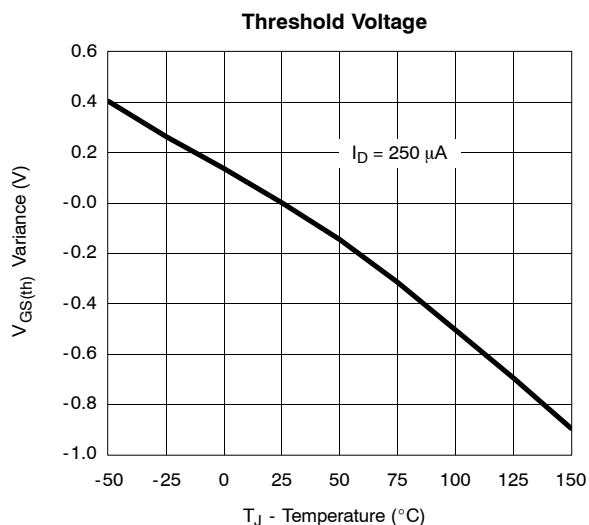
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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