

N-Channel Reduced Q_g , Fast Switching MOSFET

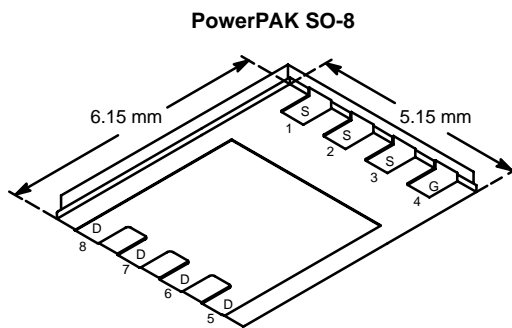
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
12	0.0055 @ $V_{GS} = 4.5$ V	22
	0.008 @ $V_{GS} = 2.5$ V	18

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for High Efficiency
- 100% R_g Tested

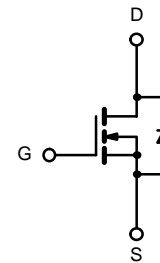
APPLICATIONS

- Point-of-Load Synchronous Rectifier
 - 5-V or 3.3-V BUS Step Down
 - Q_g Optimized for 500-kHz Operation
- Synchronous Buck, Shoot-Thru Resistant



Bottom View

Ordering Information: Si7882DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	12		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	22	13
		$T_A = 70^\circ\text{C}$	18	11
Pulsed Drain Current	I_{DM}	50		A
Continuous Source Current (Diode Conduction) ^a	I_S	4.1	1.6	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	5	1.9
		$T_A = 70^\circ\text{C}$	3.2	1.2
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^a	R_{thJA}	$t \leq 10$ sec	20	25
		Steady State	55	65
Maximum Junction-to-Case (Drain)	R_{thJC}	2.0	2.6	$^\circ\text{C/W}$

Notes

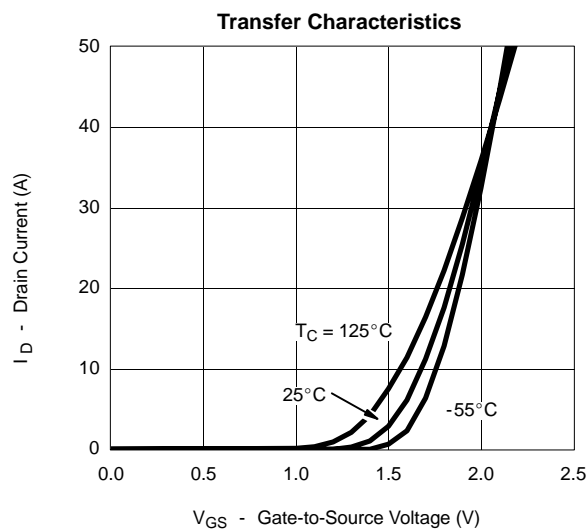
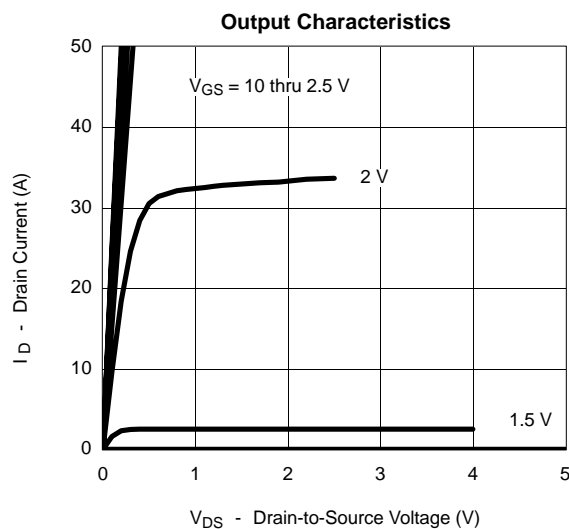
a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

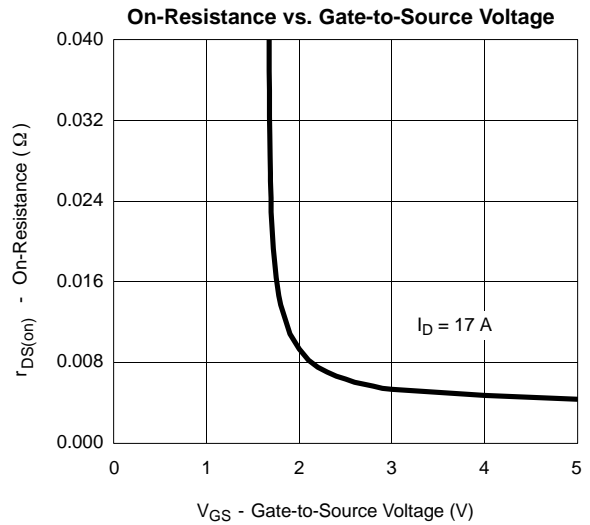
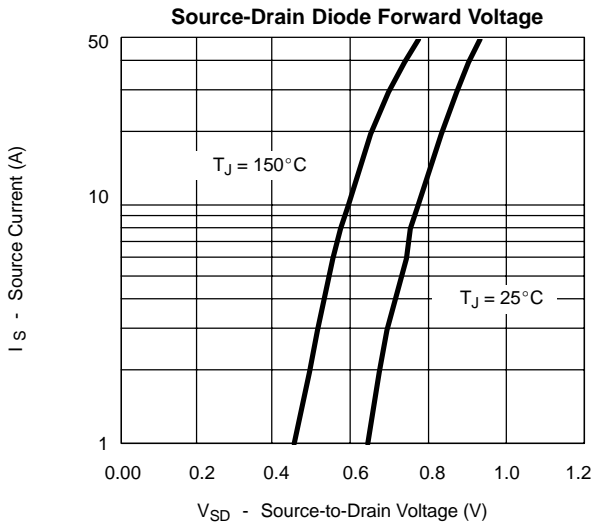
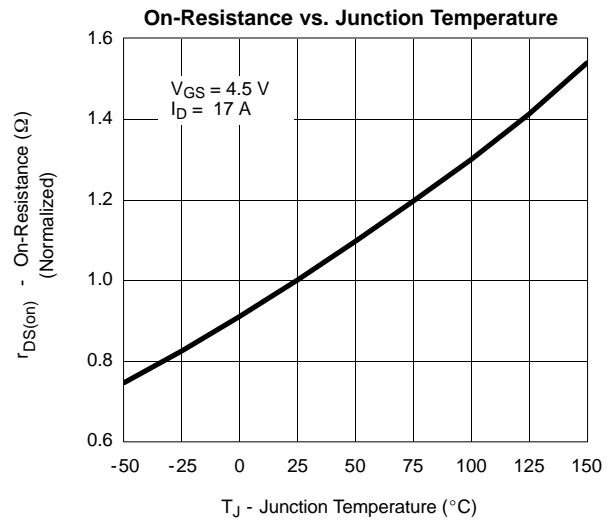
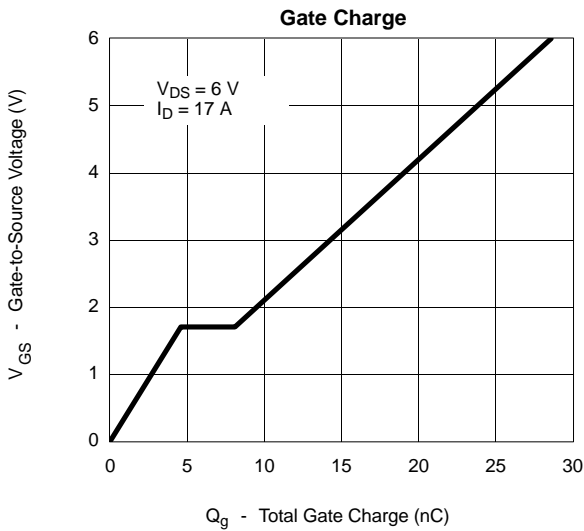
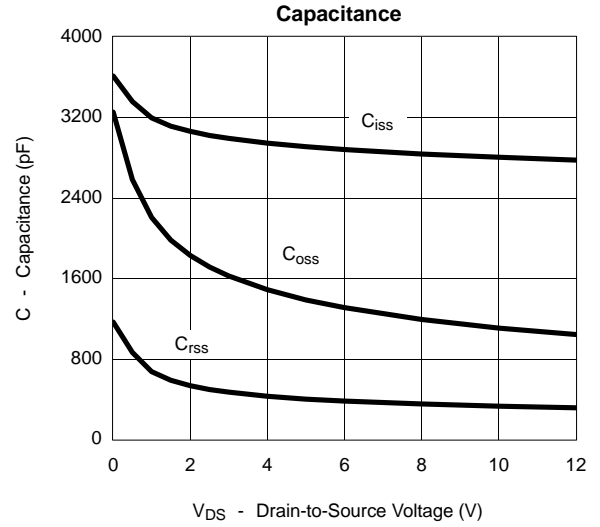
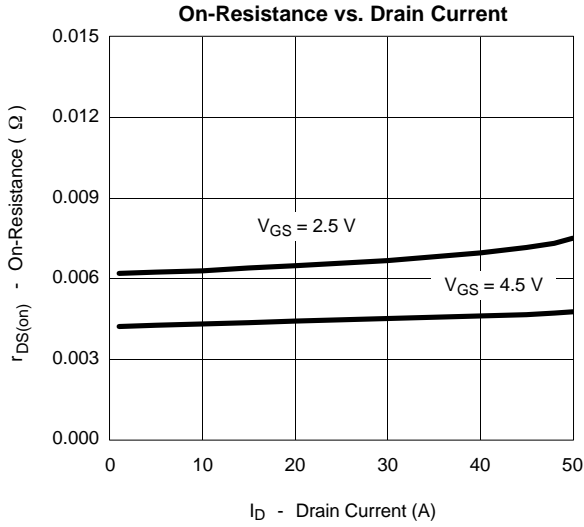
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6		1.4	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 9.6\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 9.6\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 17\ \text{A}$		0.0045	0.0055	Ω
		$V_{GS} = 2.5\ \text{V}, I_D = 14\ \text{A}$		0.0065	0.008	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 6\ \text{V}, I_D = 17\ \text{A}$		80		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.7\ \text{A}, V_{GS} = 0\ \text{V}$		0.70	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 6\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 17\ \text{A}$		21	30	nC
Gate-Source Charge	Q_{gs}		4.6			
Gate-Drain Charge	Q_{gd}		3.5			
Gate Resistance	R_g		0.8		3.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\ \text{V}, R_L = 6\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_G = 6\ \Omega$		28	42	ns
Rise Time	t_r			32	48	
Turn-Off Delay Time	$t_{d(off)}$			82	123	
Fall Time	t_f			35	53	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	90	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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