

N-Channel 60-V (D-S) Fast Switching MOSFET

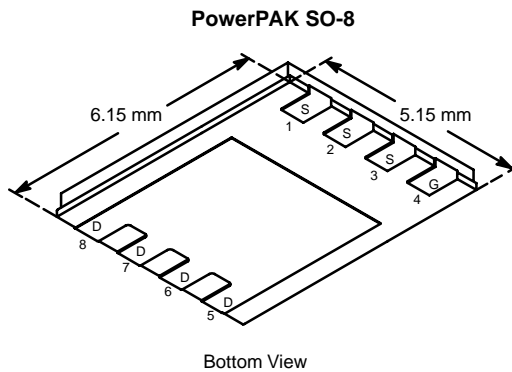
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.022 @ $V_{GS} = 10$ V	10.3
	0.031 @ $V_{GS} = 4.5$ V	8.7

FEATURES

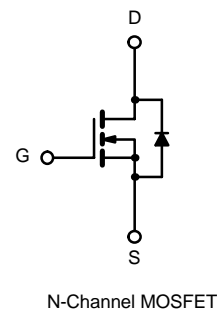
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100% R_g Tested

APPLICATIONS

- Primary Side Switch for 24-V DC/DC Applications
- Secondary Synchronous Rectifier



Ordering Information: Si7850DP-T1



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	60		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	10.3	6.2	A
		$T_A = 85^\circ\text{C}$	7.5	4.5	
Continuous Source Current	I_S	3.7	1.5		
Pulsed Drain Current	I_{DM}	40			
Avalanche Current ^b	I_{AS}	15			
Single Avalanche Energy ^b	E_{AS}	11		mJ	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	4.5	1.8	W
		$T_A = 85^\circ\text{C}$	2.3	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	22	28	$^\circ\text{C/W}$
		Steady State	58	70	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.6	3.3		

Notes

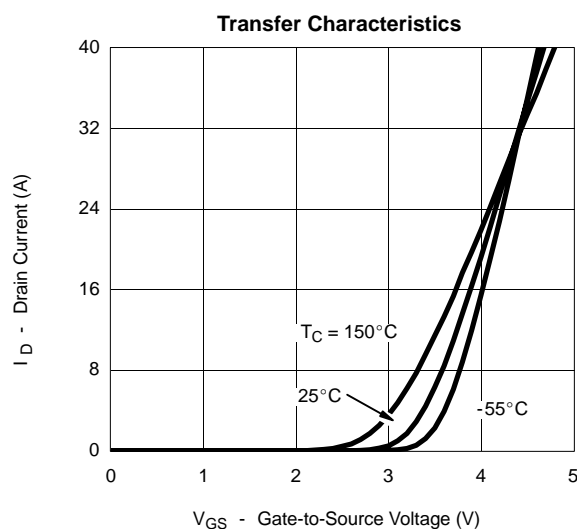
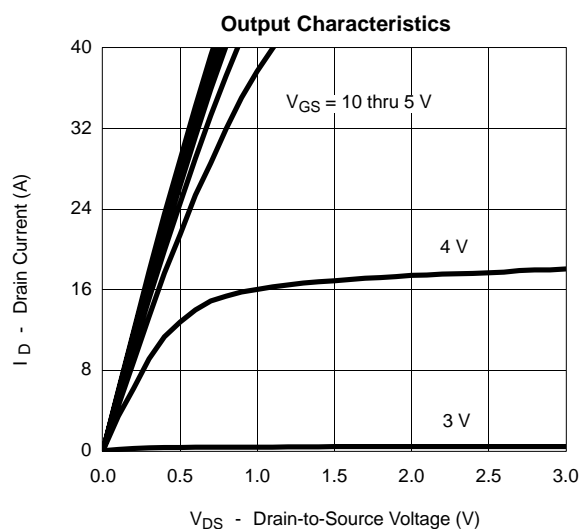
- a. Surface Mounted on 1" x 1" FR4 Board.
b. Guaranteed by design, not subject to production testing.

MOSFET SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			20	
On-State Drain Current ^{NO TAG}	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40			A
Drain-Source On-State Resistance ^{NO TAG}	r _{DS(on)}	V _{GS} = 10 V, I _D = 10.3 A		0.018	0.022	Ω
		V _{GS} = 4.5 V, I _D = 8.7 A		0.025	0.031	
Forward Transconductance ^{NO TAG}	g _{fs}	V _{DS} = 15 V, I _D = 10.3 A		26		S
Diode Forward Voltage ^{NO TAG}	V _{SD}	I _S = 3.8 A, V _{GS} = 0 V		0.85	1.2	V
Dynamic^{NO TAG}						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 10.3 A		18	27	nC
Gate-Source Charge	Q _{gs}			3.4		
Gate-Drain Charge	Q _{gd}			5.3		
Gate-Resistance	R _G		0.5	1.4	2.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		10	20	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			25	50	
Fall Time	t _f			12	24	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3.8 A, di/dt = 100 A/μs		50	80	

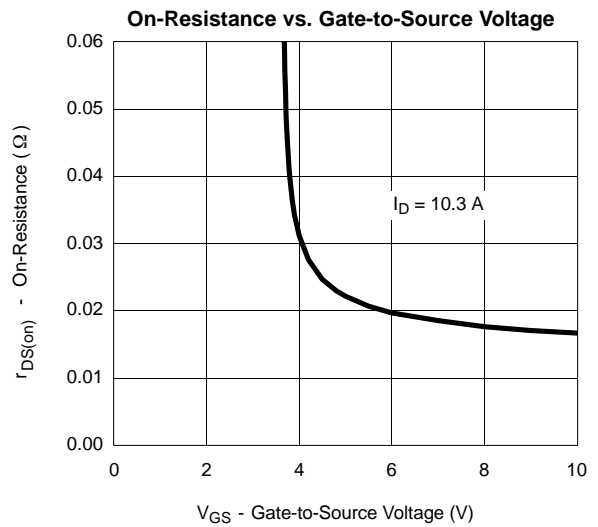
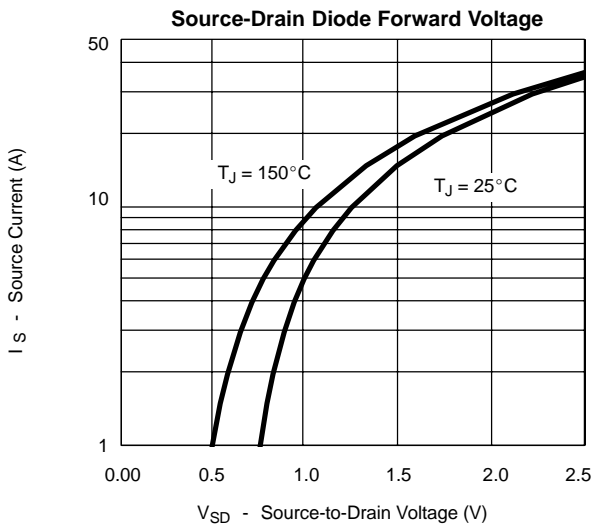
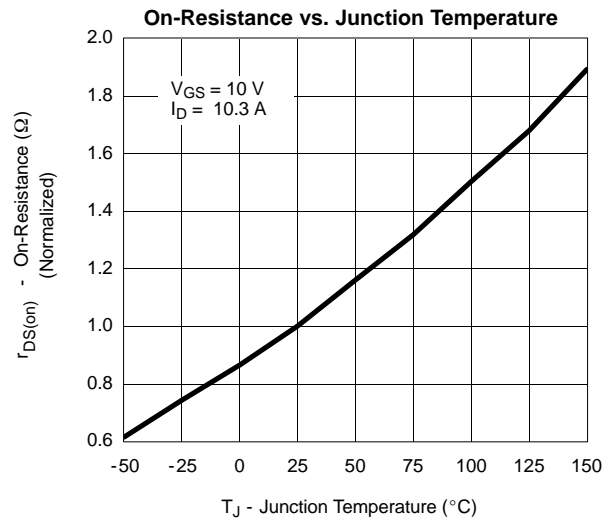
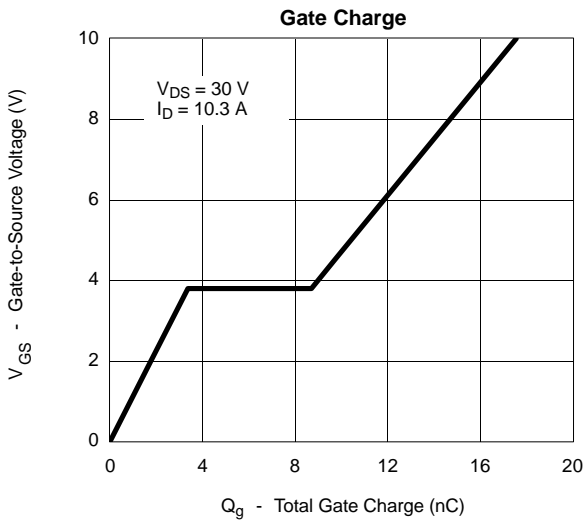
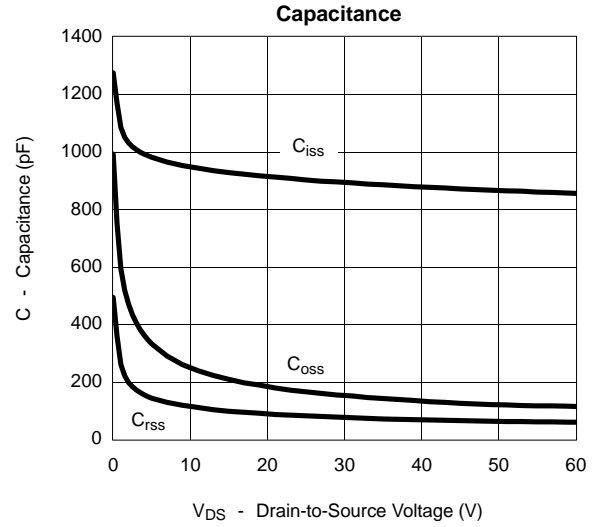
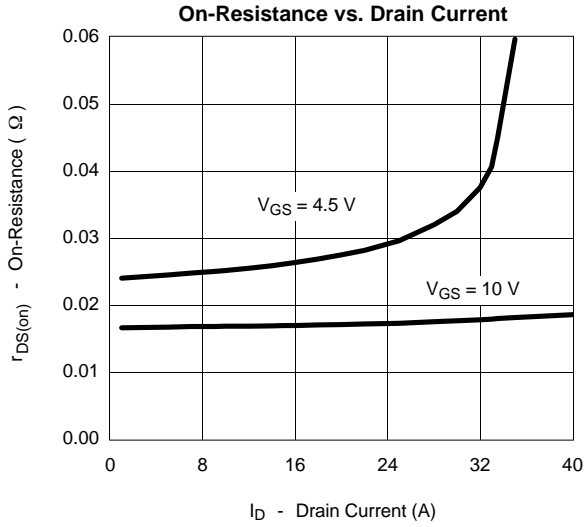
Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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