



N-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

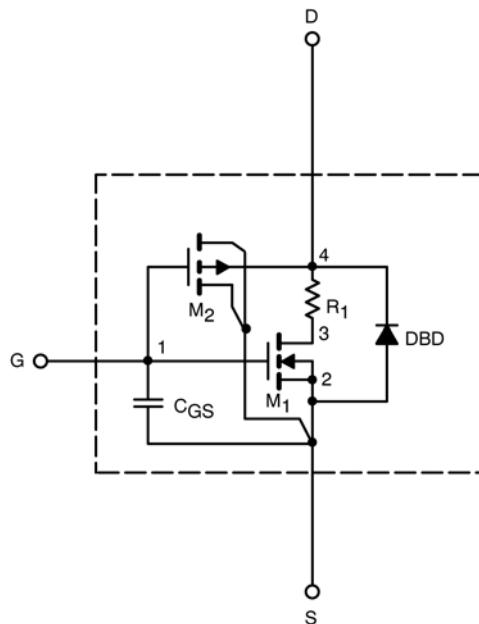
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



| SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---------------------|--|----------------|---------------|------|
| Parameter | Symbol | Test Condition | Simulated Data | Measured Data | Unit |
| Static | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1.9 | | V |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} ≥ 5 V, V _{GS} = 10 V | 1882 | | A |
| Drain-Source On-State Resistance ^a | r _{DS(on)} | V _{GS} = 10 V, I _D = 25 A | 0.0033 | 0.0033 | Ω |
| | | V _{GS} = 4.5 V, I _D = 19 A | 0.0040 | 0.0040 | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 15 V, I _D = 25 A | 95 | 110 | S |
| Forward Voltage ^a | V _{SD} | I _S = 2.9 A, V _{GS} = 0 V | 0.83 | 0.72 | V |
| Dynamic^b | | | | | |
| Total Gate Charge | Q _g | V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A | 37 | 32 | nC |
| Gate-Source Charge | Q _{gs} | | 16.5 | 16.5 | |
| Gate-Drain Charge | Q _{gd} | | 8.5 | 8.5 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω | 22 | 24 | ns |
| Rise Time | t _r | | 13 | 16 | |
| Turn-Off Delay Time | t _{d(off)} | | 70 | 90 | |
| Fall Time | t _f | | 55 | 32 | |

Notes

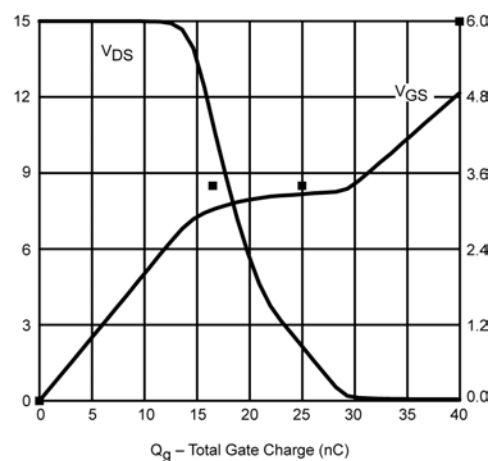
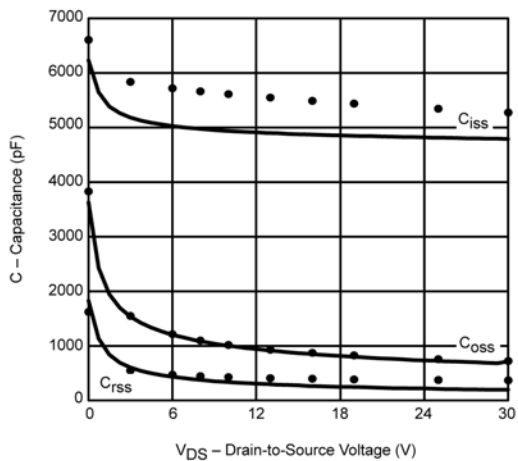
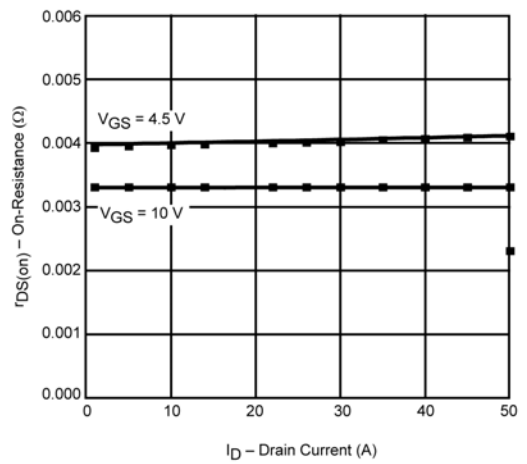
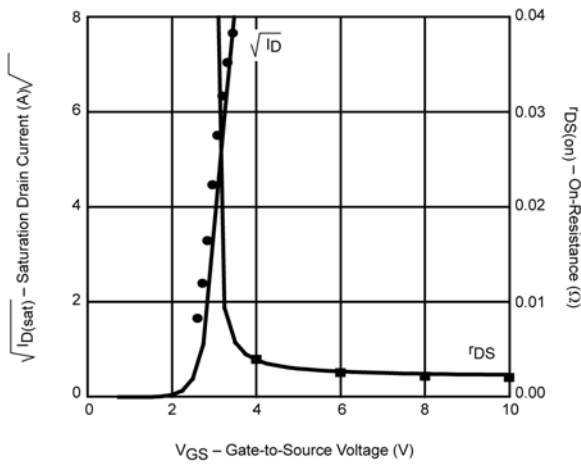
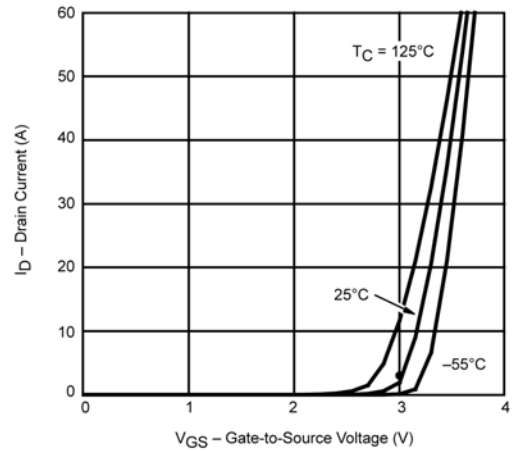
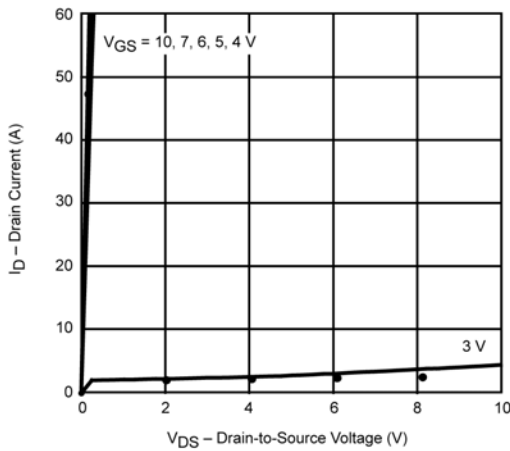
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si7636DP

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.