

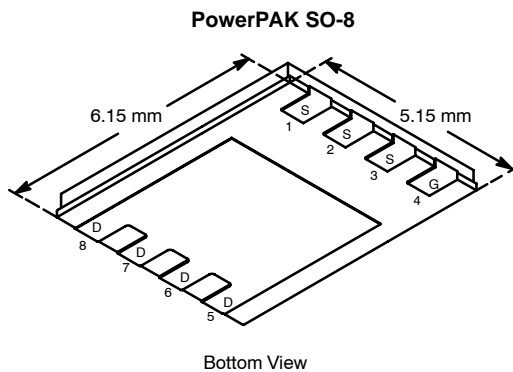


N-Channel 60-V (D-S) Fast Switching MOSFET

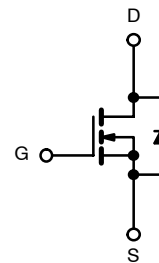
PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
60	0.0083 @ V _{GS} = 10 V	19.3	105

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100% R_g Tested
- High Threshold Voltage At High Temperature



Ordering Information: Si7452DP-T1—E3



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	60		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	19.3	11.5	A
	T _A = 70 °C		15.5	9.2	
Pulsed Drain Current		I _{DM}	60		
Continuous Source Current (Diode Conduction) ^a		I _S	4.5	1.6	
Avalanche Current		I _{AS}	40		
Avalanche Energy		E _{AS}	80		mJ
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	5.4	1.9	W
	T _A = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 sec	R _{thJA}	18	23	°C/W
	Steady State		52	65	
Maximum Junction-to-Case (Drain)		R _{thJC}	1.0	1.3	

Notes

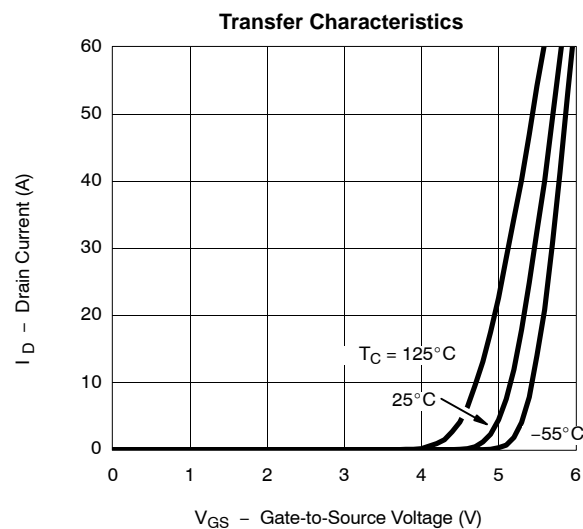
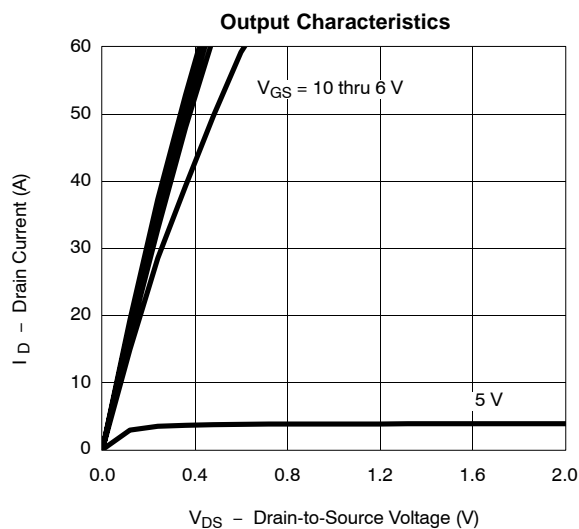
a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3.4		4.5	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 19.3 A		0.007	0.0083	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 19.3 A		51		S
Diode Forward Voltage ^a	V _{SD}	I _S = 4.5 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 19.3 A		105	160	nC
Gate-Source Charge	Q _{gs}			40		
Gate-Drain Charge	Q _{gd}			21		
Gate Resistance	R _g	f = 1 MHz	0.5	1.0	1.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω		45	70	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			90	135	
Fall Time	t _f			40	60	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 4.5 A, di/dt = 100 A/μs		46	

Notes

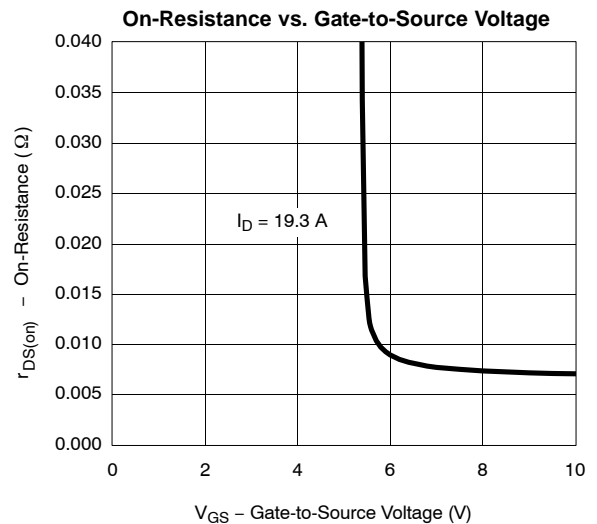
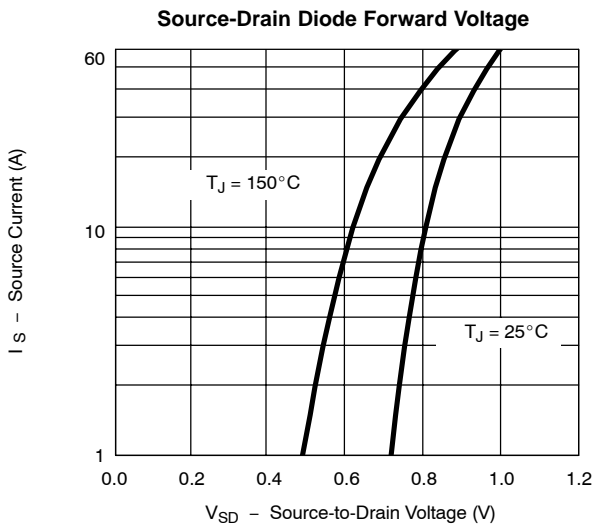
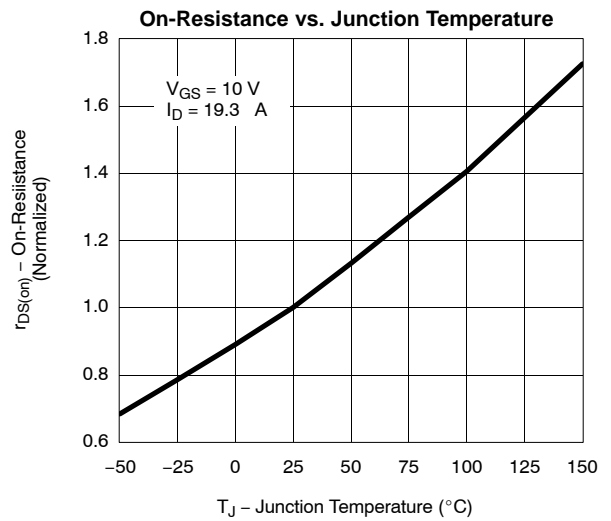
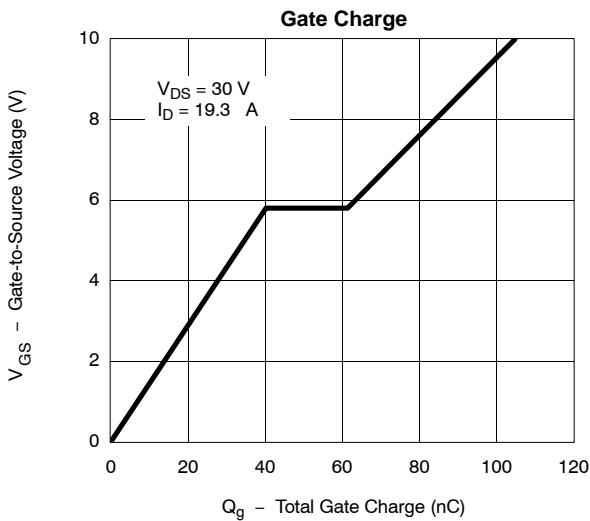
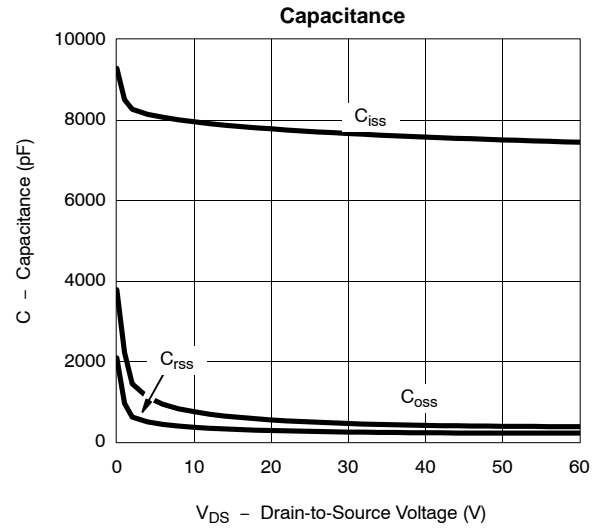
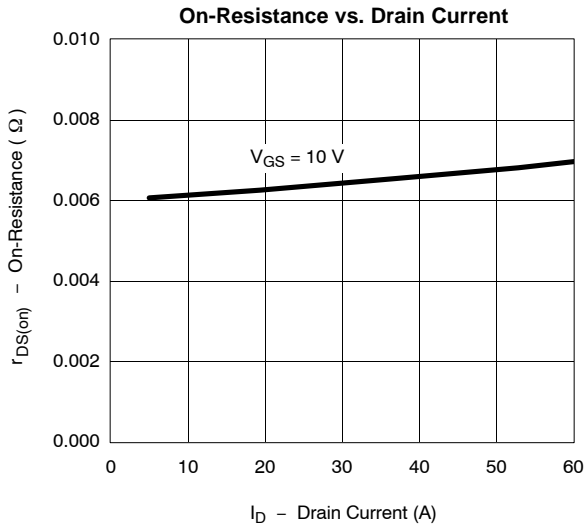
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

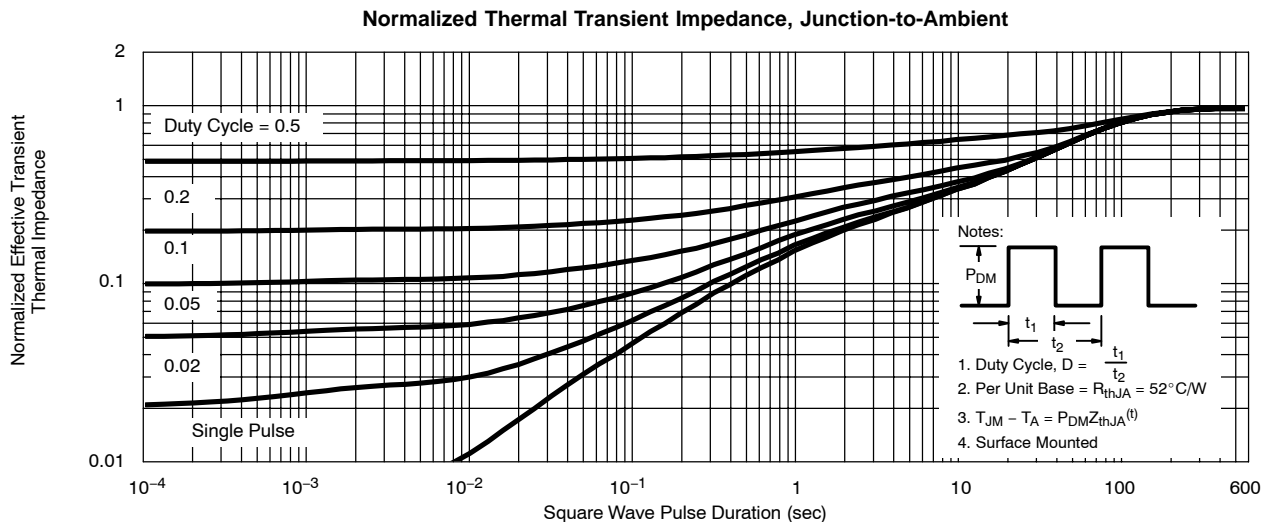
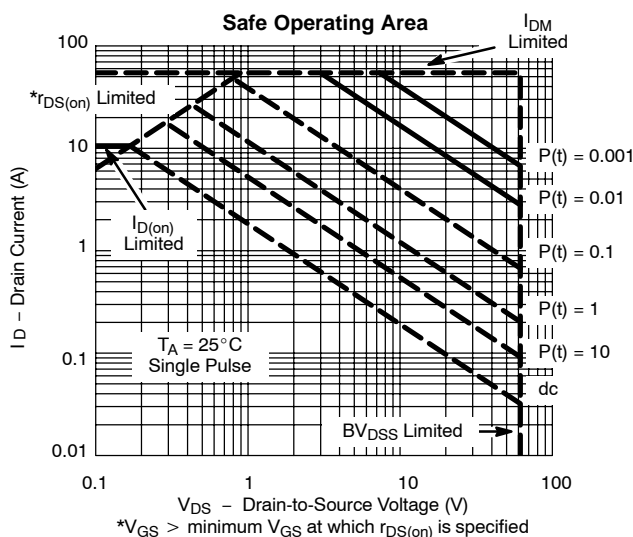
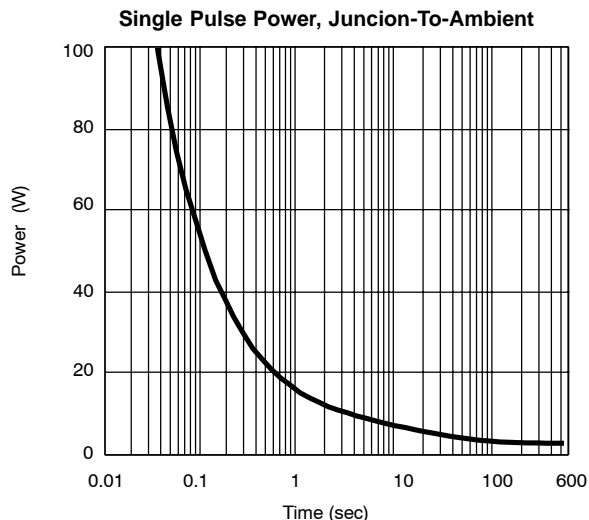
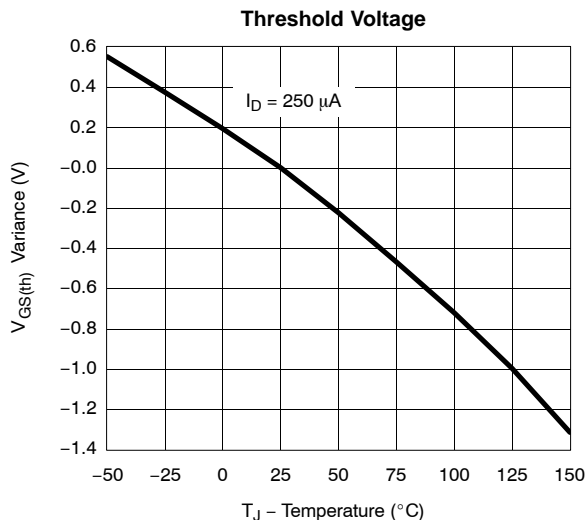
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)




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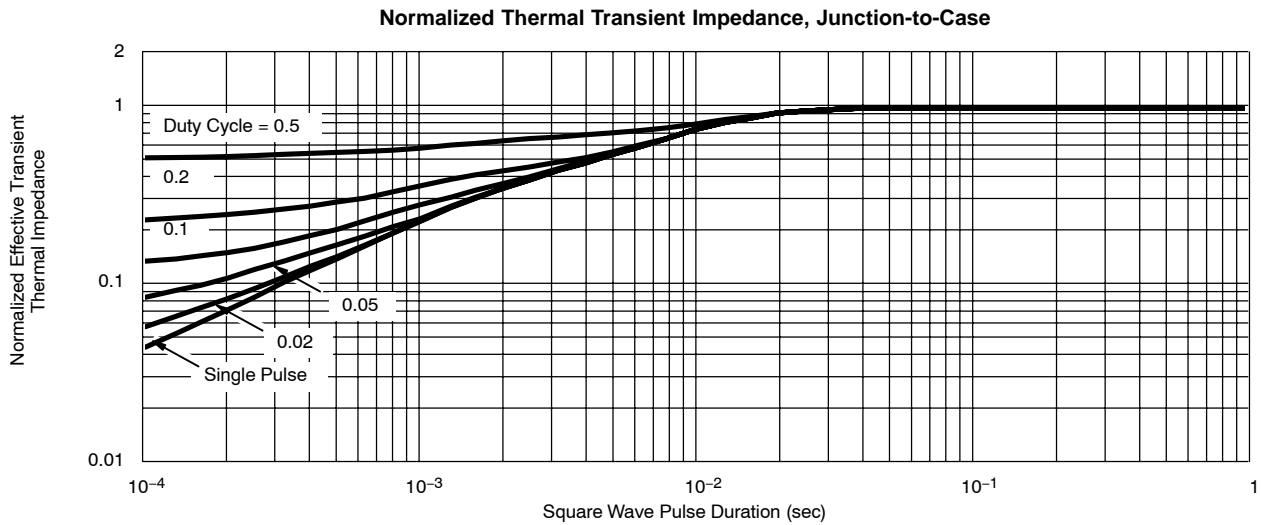


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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72972>.