

N-Channel 200-V (D-S) Fast Switching MOSFET

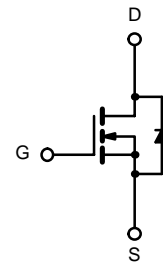
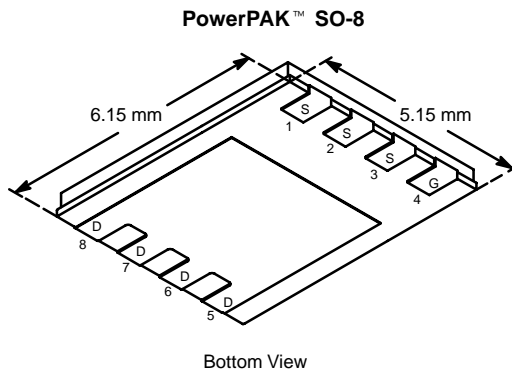
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.24 @ $V_{GS} = 10$ V	2.8
	0.26 @ $V_{GS} = 6$ V	2.7

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching

APPLICATIONS

- Primary Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	200		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	2.8	1.8	A
		$T_A = 70^\circ\text{C}$	2.2	1.5	
Continuous Source Current	I_S	3.5	1.5		
Pulsed Drain Current	I_{DM}	8			
Avalanche Current ^b	I_{AS}	3			
Single Avalanche Energy ^b	E_{AS}	0.45		mJ	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	4.2	1.8	W
		$T_A = 70^\circ\text{C}$	2.6	1.1	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	25	30	$^\circ\text{C/W}$
		Steady State	60	70	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.9	3.5		

Notes

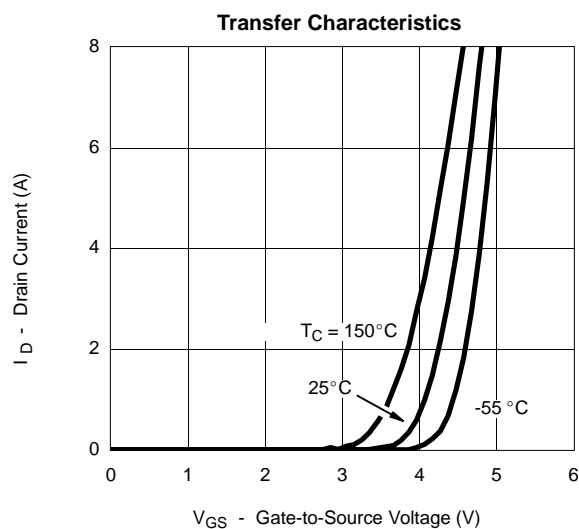
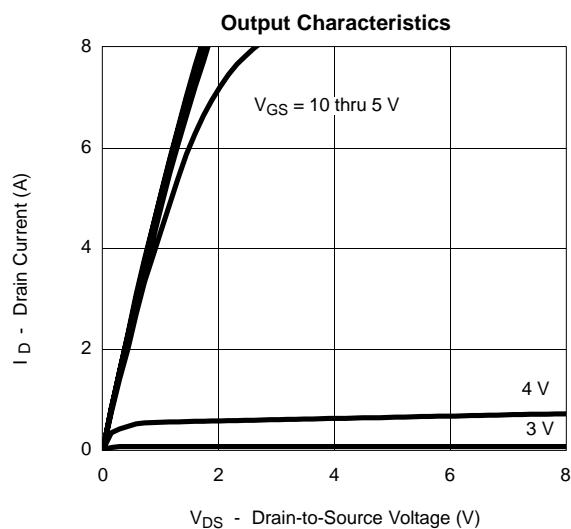
- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Guaranteed by design, not subject to production testing.

MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

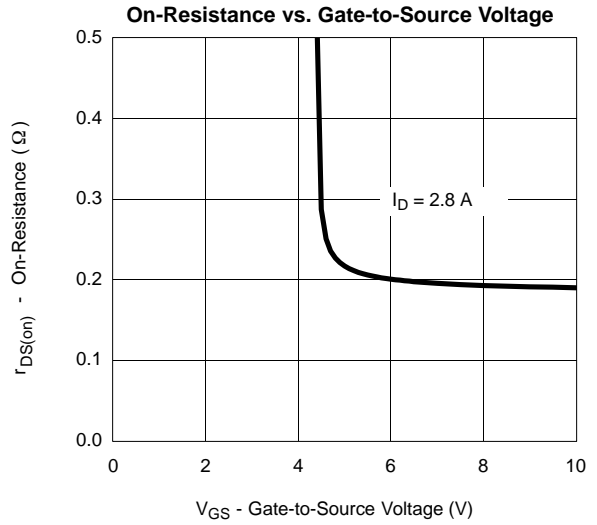
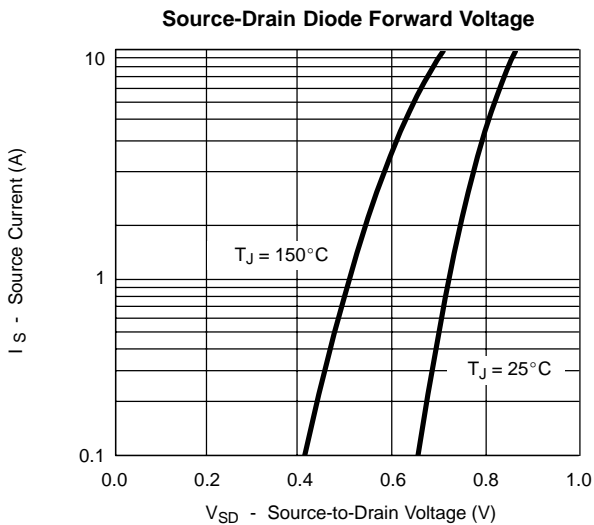
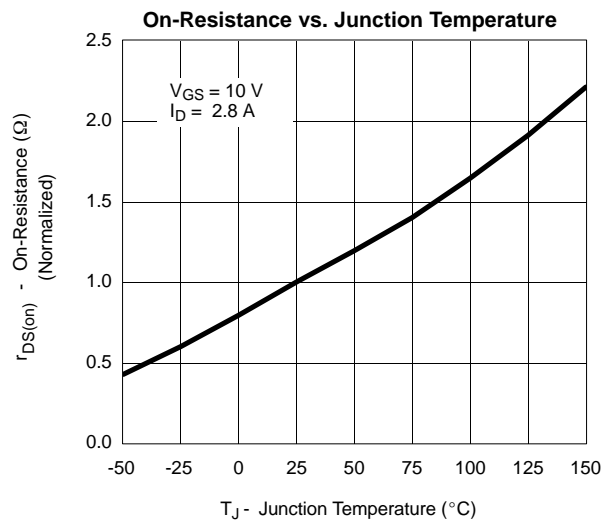
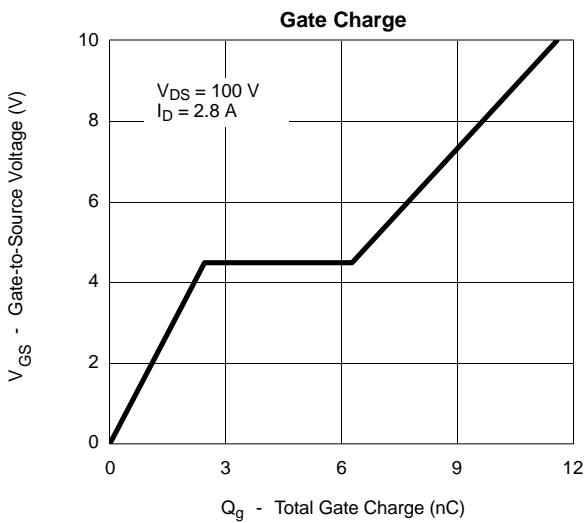
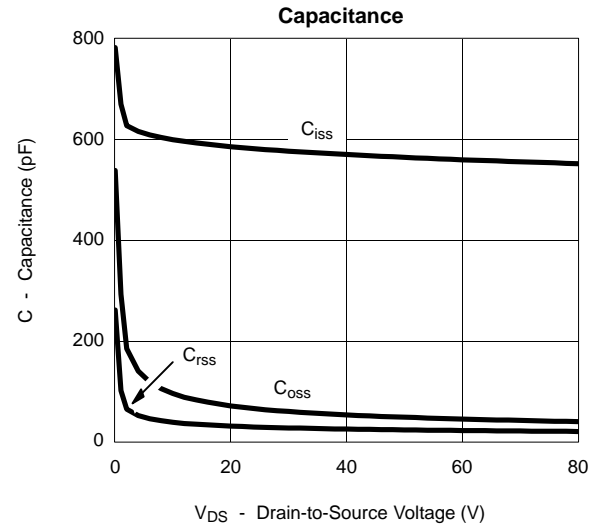
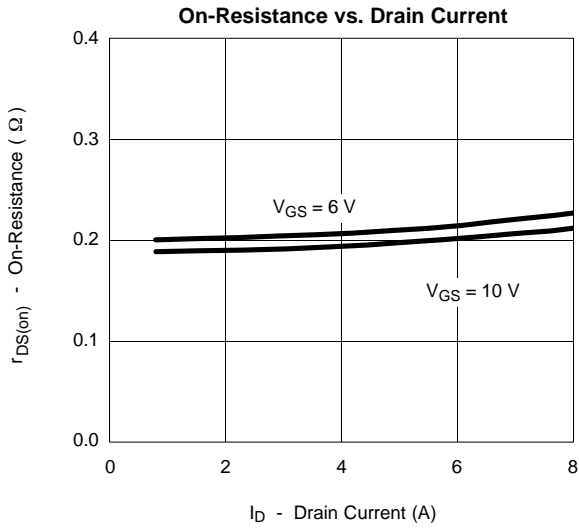
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2		4	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 160 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 160 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	8			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 2.8 \text{ A}$		0.195	0.24	Ω
		$V_{GS} = 6 \text{ V}, I_D = 2.7 \text{ A}$		0.210	0.26	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 2.8 \text{ A}$		8		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2.8 \text{ A}$		12	18	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			3.8		
Gate-Resistance	R_G			2.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}, R_L = 100 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		10	15	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		60	90	

Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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