

## N-Channel 200-V (D-S) MOSFET

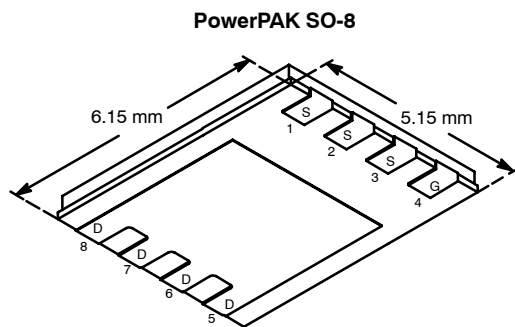
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
200	0.130 @ $V_{GS} = 10$ V	4.1
	0.142 @ $V_{GS} = 6.0$ V	3.9

### FEATURES

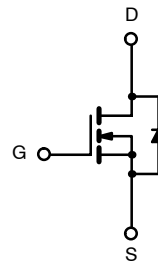
- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized For Fast Switching

### APPLICATIONS

- Primary Side Switch



Bottom View  
Ordering Information: Si7462DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	200		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	4.1	2.6	A
		$T_A = 85^\circ\text{C}$	3.0	1.9	
Pulsed Drain Current	$I_{DM}$	12			
Avalanche Current	$I_{AS}$	6			
Single Avalanche Energy (Duty Cycle $\leq 1\%$ )	$E_{AS}$	L = 0.1 mH	1.8		mJ
Continuous Source Current (Diode Conduction) <sup>a</sup>			$I_S$	4.0	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	4.8	1.9	W
		$T_A = 85^\circ\text{C}$	2.6	1.0	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	21	26	$^\circ\text{C/W}$
		Steady State	55	65	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.7	2.1		

**Notes**

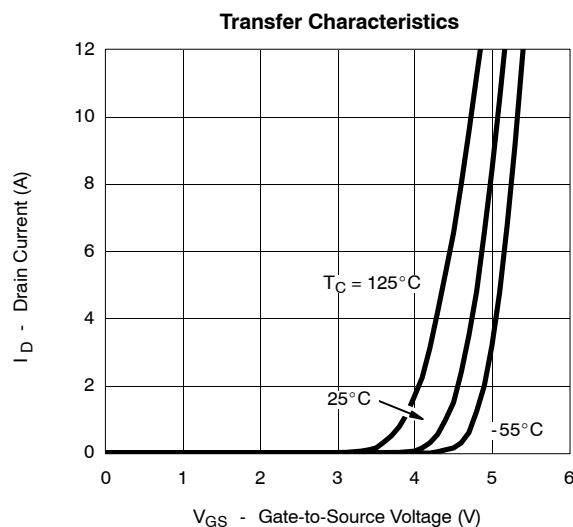
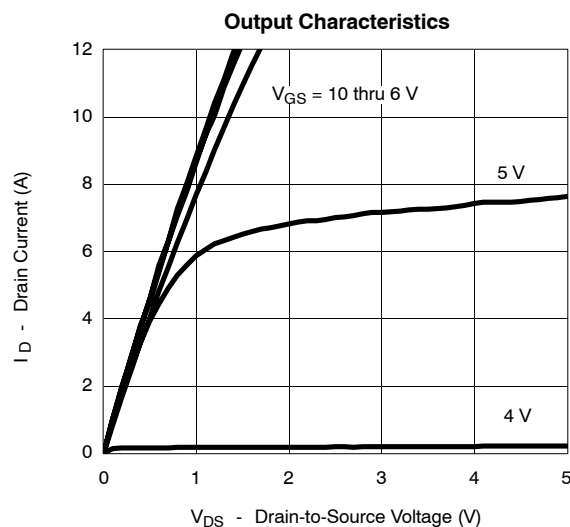
a. Surface Mounted on 1" x 1" FR4 Board.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			20	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	12			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.1 A		0.110	0.130	Ω
		V <sub>GS</sub> = 6.0 V, I <sub>D</sub> = 3.9 A		0.120	0.142	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.1 A		13		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 4 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.1 A		20	30	nC
Gate-Source Charge	Q <sub>gs</sub>		4.5			
Gate-Drain Charge	Q <sub>gd</sub>		6.5			
Gate Resistance	R <sub>G</sub>			2		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, R <sub>L</sub> = 100 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		15	25	ns
Rise Time	t <sub>r</sub>		15	25		
Turn-Off Delay Time	t <sub>d(off)</sub>		40	60		
Fall Time	t <sub>f</sub>		20	30		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 4 A, di/dt = 100 A/μs		70	110	

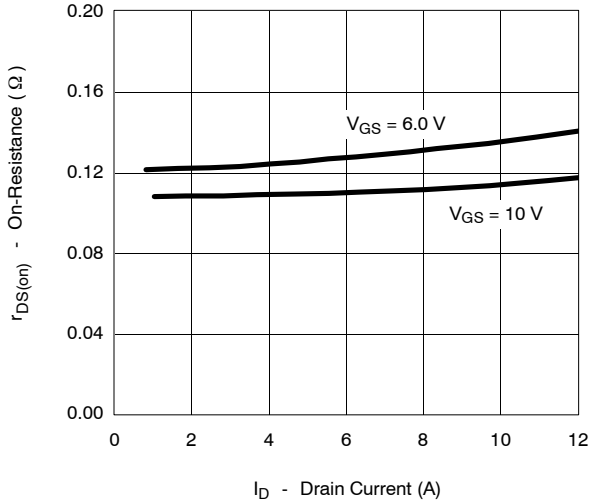
## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

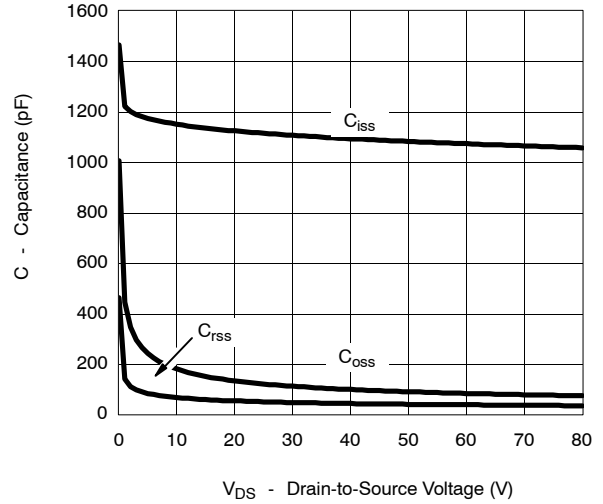
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

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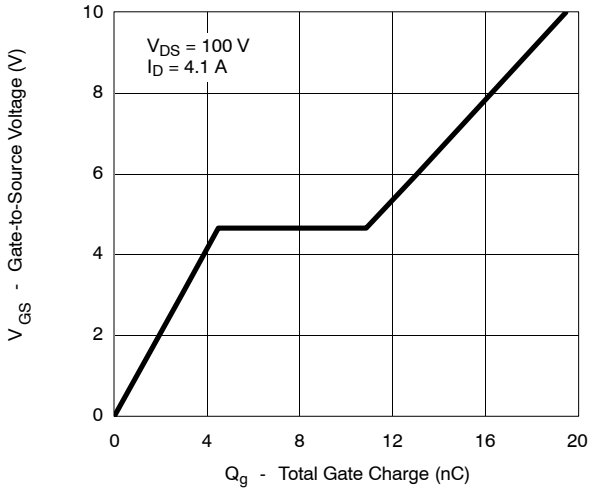
**On-Resistance vs. Drain Current**



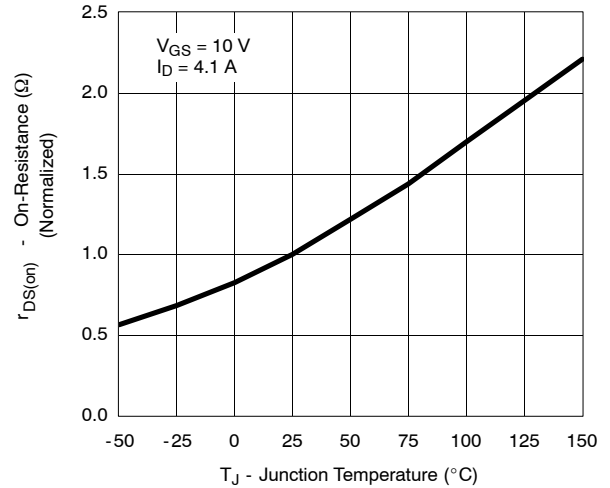
**Capacitance**



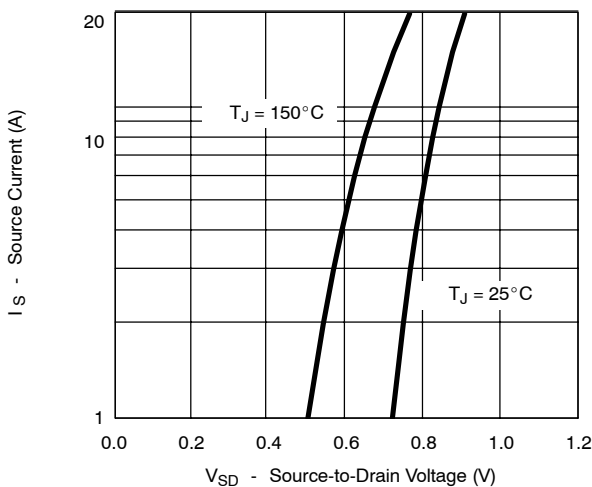
**Gate Charge**



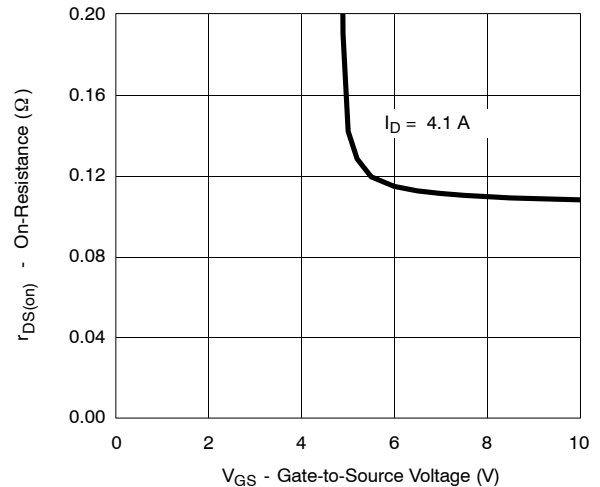
**On-Resistance vs. Junction Temperature**



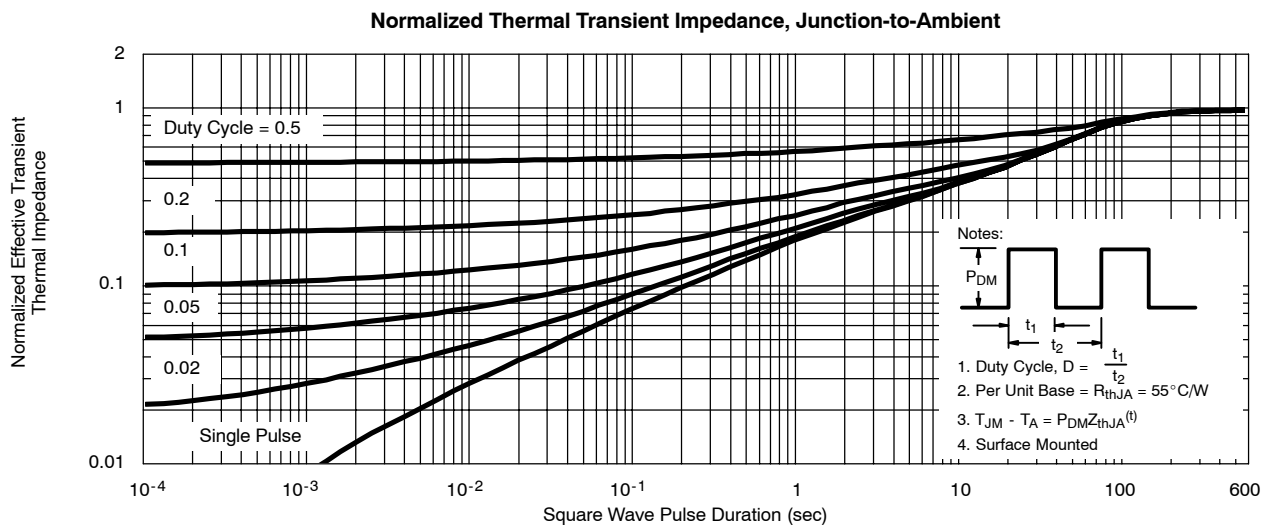
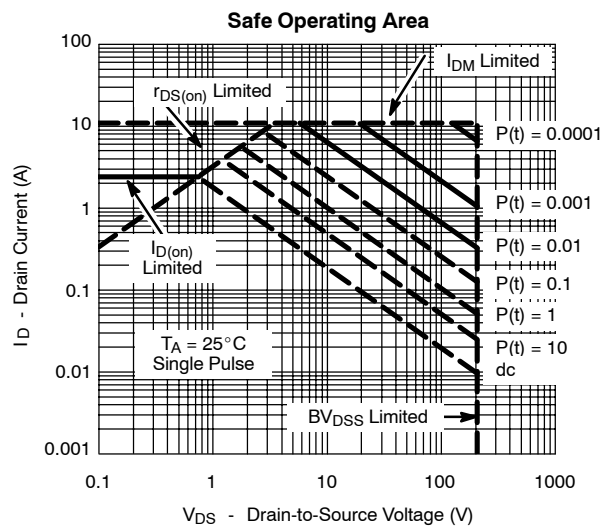
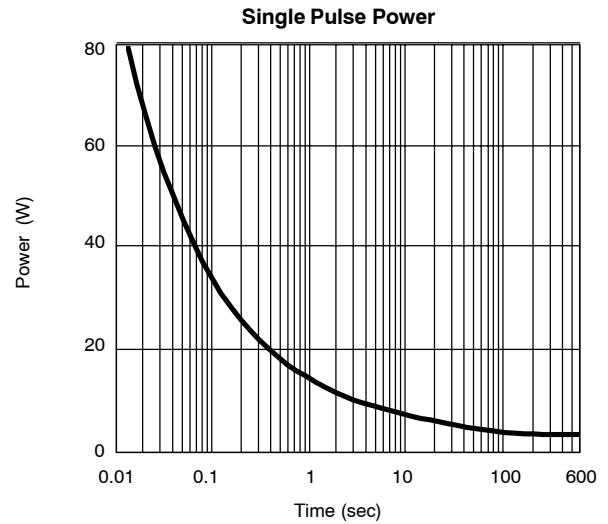
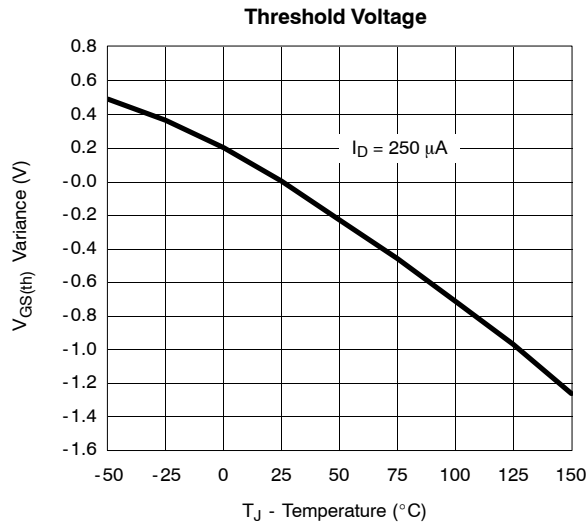
**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

Normalized Thermal Transient Impedance, Junction-to-Case

