

N-Channel 100-V (D-S) MOSFET

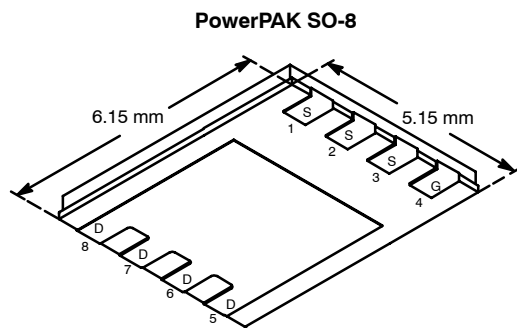
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
100	0.025 @ V _{GS} = 10 V	9.3
	0.028 @ V _{GS} = 6.0 V	8.8

FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100% R_g Tested

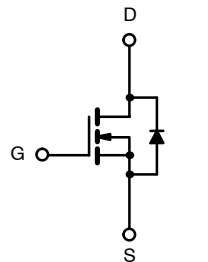
APPLICATIONS

- Primary Side Switch for High Density DC/DC
- Telecom/Server 48-V, Full-/Half-Bridge DC/DC
- Industrial and 42-V Automotive



Bottom View

Ordering Information: Si7456DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	100		V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	9.3	5.7	A
		T _A = 85°C	6.7	4.1	
Pulsed Drain Current	I _{DM}	40			
Avalanche Current	I _{AS}	30			
Single Avalanche Energy (Duty Cycle ≤ 1%)	E _{AS}	L = 0.1 mH	45		mJ
Continuous Source Current (Diode Conduction) ^a			I _S	4.3	
Maximum Power Dissipation ^a	P _D	T _A = 25°C	5.2	1.9	W
		T _A = 85°C	2.7	1.0	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	19	24	°C/W
		Steady State	52	65	
Maximum Junction-to-Case	R _{thJC}	1.5	1.8		

Notes

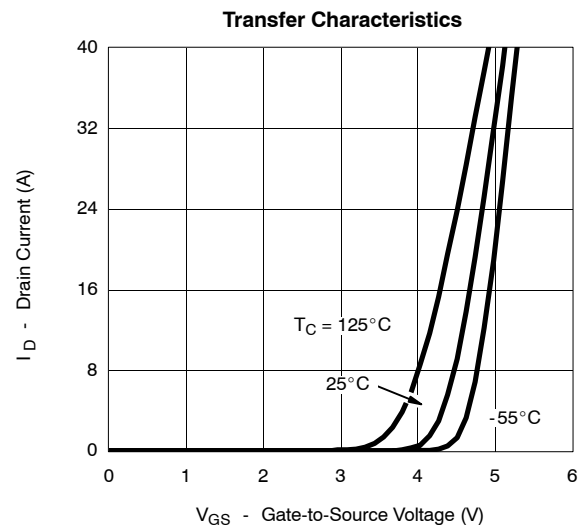
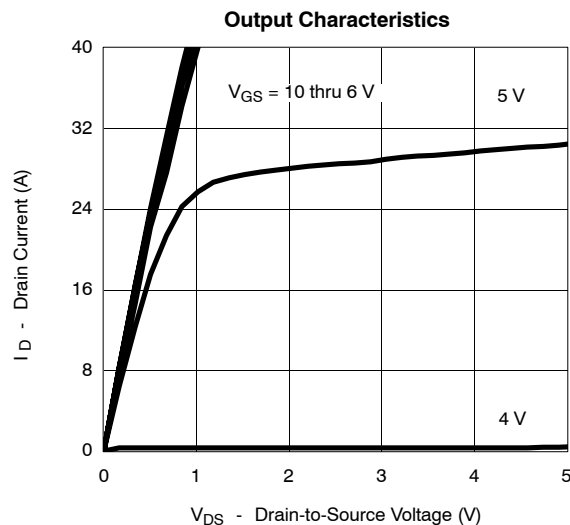
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 85 °C			20	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 9.3 A		0.021	0.025	Ω
		V _{GS} = 6.0 V, I _D = 8.8 A		0.023	0.028	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 9.3 A		35		S
Diode Forward Voltage ^a	V _{SD}	I _S = 4.3 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 9.3 A		36	44	nC
Gate-Source Charge	Q _{gs}			10		
Gate-Drain Charge	Q _{gd}			8.6		
Gate Resistance	R _g		0.5	1.27	2.1	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		20	40	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			46	90	
Fall Time	t _f			26	50	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 4.3 A, di/dt = 100 A/μs		50	80	

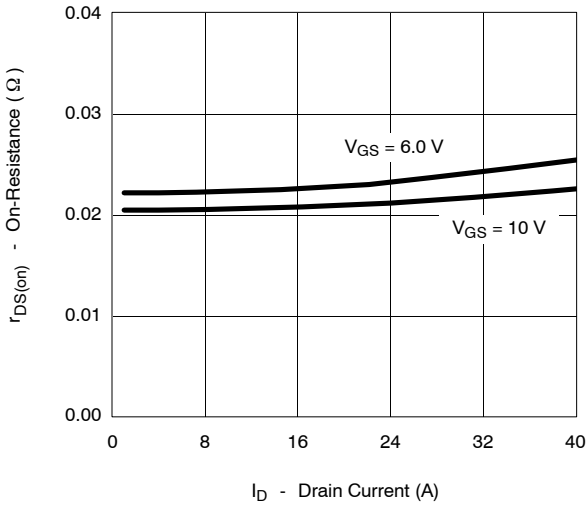
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

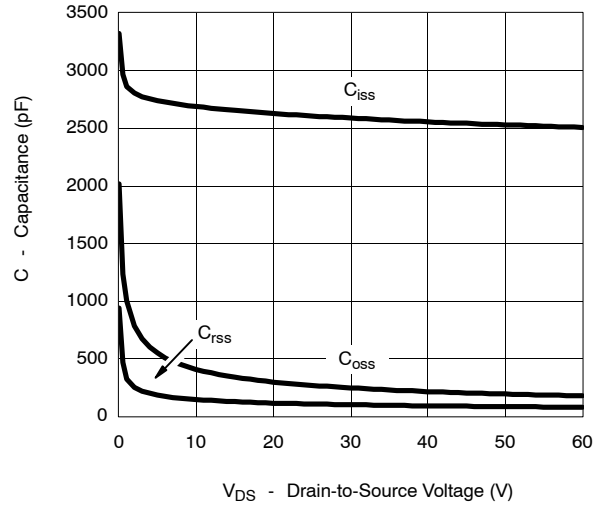
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

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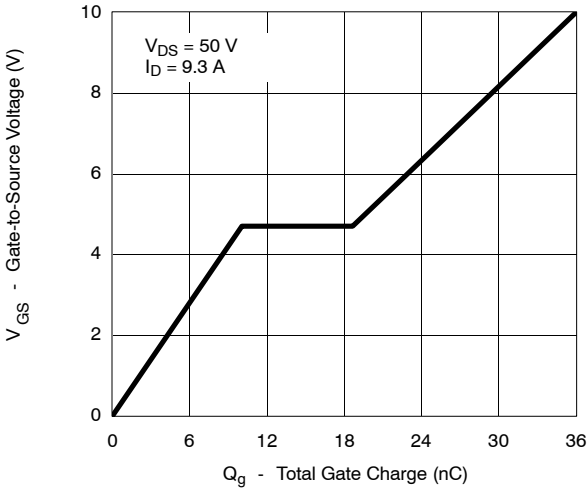
On-Resistance vs. Drain Current



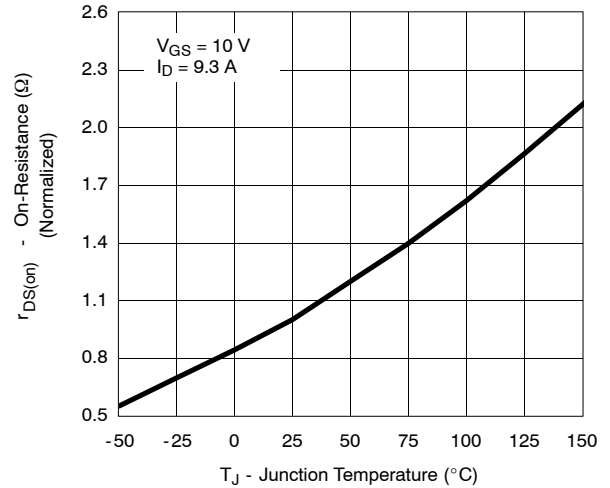
Capacitance



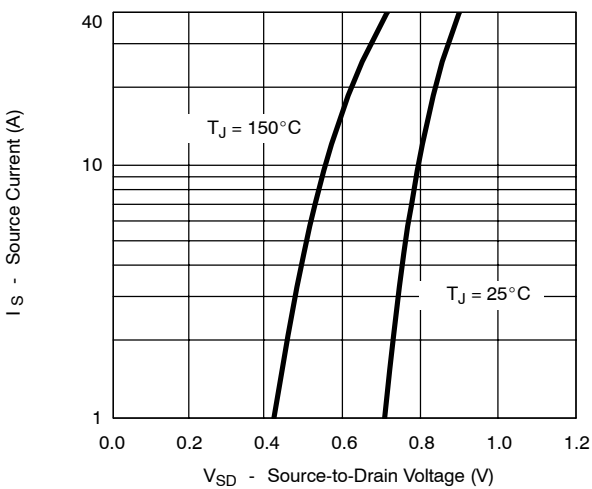
Gate Charge



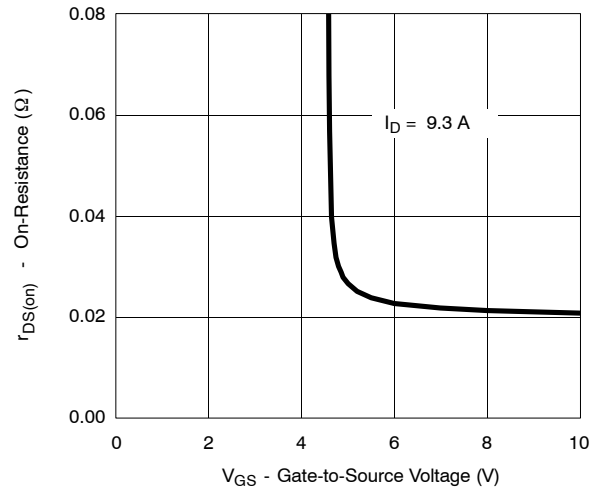
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

