

## P-Channel 12-V (D-S) MOSFET

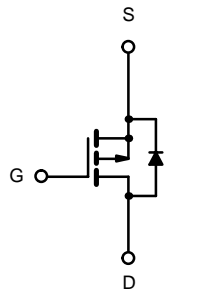
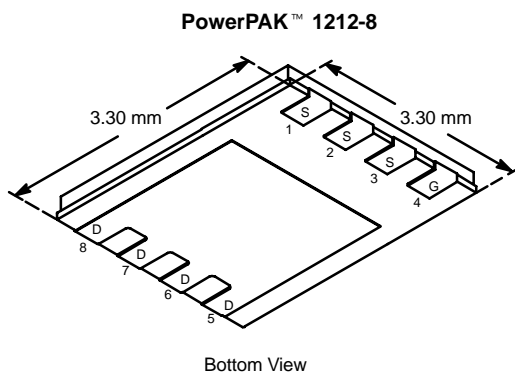
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-12	0.012 @ $V_{GS} = -4.5$ V	-15.6
	0.016 @ $V_{GS} = -2.5$ V	-13.5
	0.024 @ $V_{GS} = -1.8$ V	-11

### FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- Ultra-Low  $r_{DS(on)}$

### APPLICATIONS

- Load Switch
- PA Switch
- Battery Switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	-12		V	
Gate-Source Voltage	$V_{GS}$	$\pm 8$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	-15.6	-9.9	A
		$T_A = 85^\circ\text{C}$	-11.2	-7.2	
Pulsed Drain Current	$I_{DM}$	-30			
continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-3.2	-1.3		
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	3.8	1.5	W
		$T_A = 85^\circ\text{C}$	2.0	0.8	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	26	33	$^\circ\text{C/W}$
		Steady State	65	81	
Maximum Junction-to-Case	$R_{thJC}$	1.9	2.4		

Notes

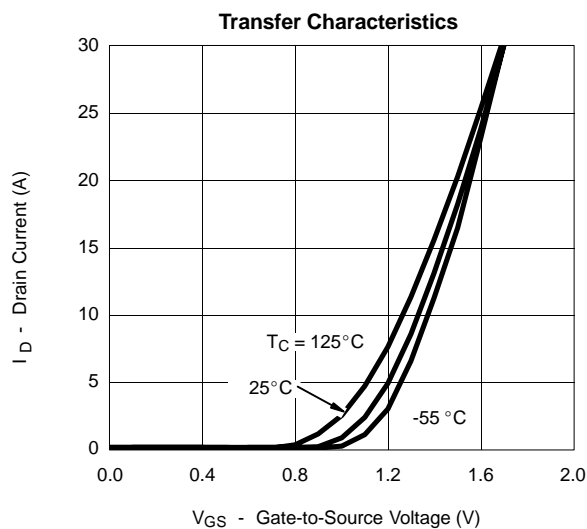
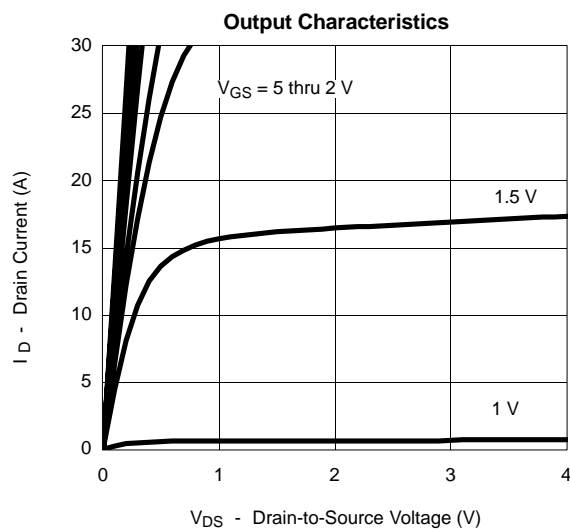
a. Surface Mounted on 1" x 1" FR4 Board.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -400 μA	-0.40		-1.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -9.6 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -9.6 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			-5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	-30			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -15.6 A		0.009	0.012	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -13.5 A		0.013	0.016	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -5 A		0.019	0.024	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -6 V, I <sub>D</sub> = -15.6 A		52		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -3.2 A, V <sub>GS</sub> = 0 V		-0.7	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -15.6 A		39	59	nC
Gate-Source Charge	Q <sub>gs</sub>			6		
Gate-Drain Charge	Q <sub>gd</sub>			11		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -6 V, R <sub>L</sub> = 6 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω		30	45	ns
Rise Time	t <sub>r</sub>			50	75	
Turn-Off Delay Time	t <sub>d(off)</sub>			200	300	
Fall Time	t <sub>f</sub>			165	250	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = -3.2 A, di/dt = 100 A/μs		60	

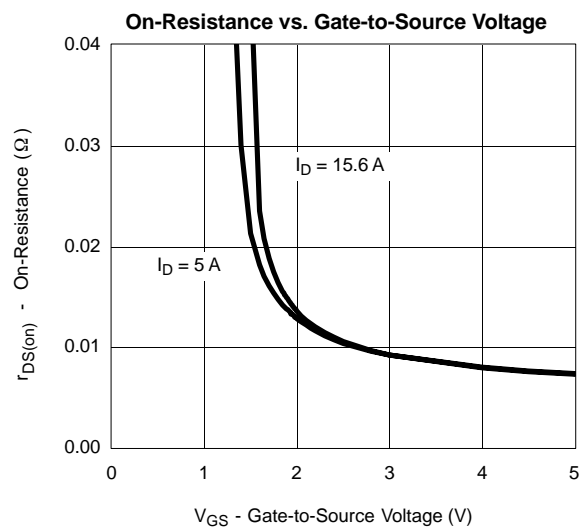
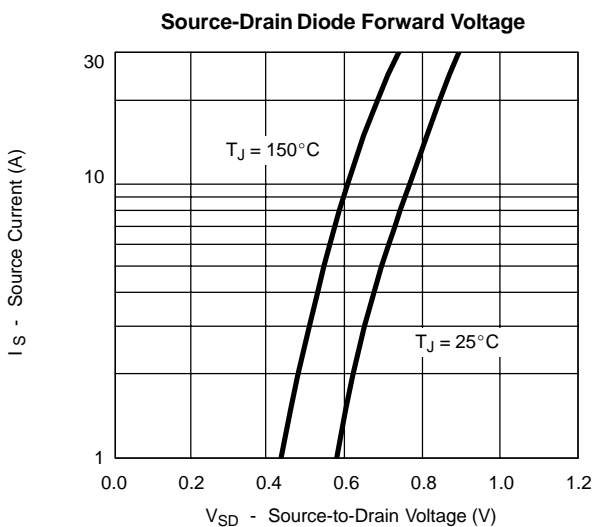
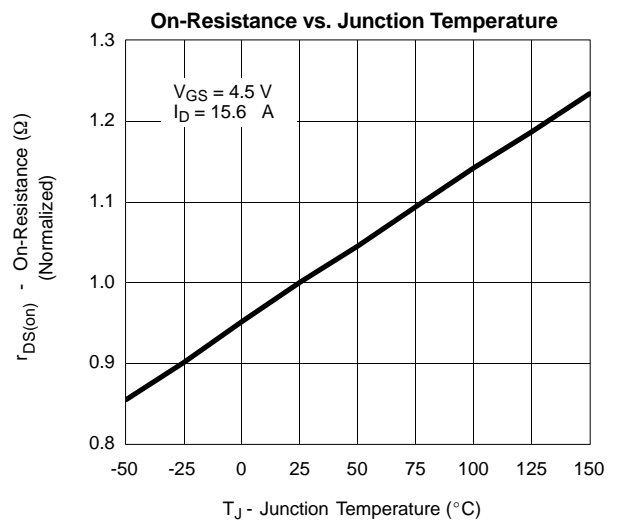
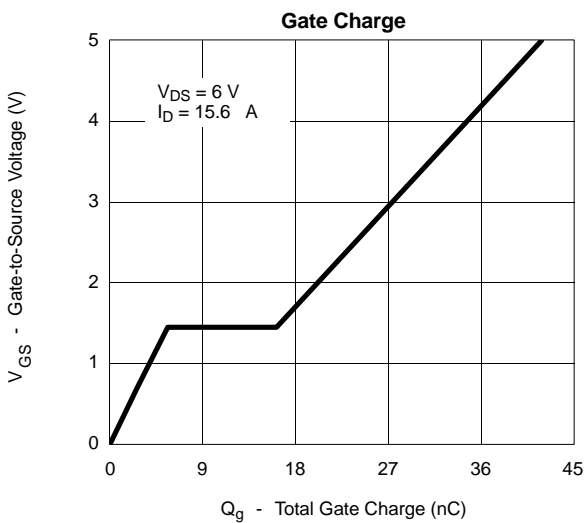
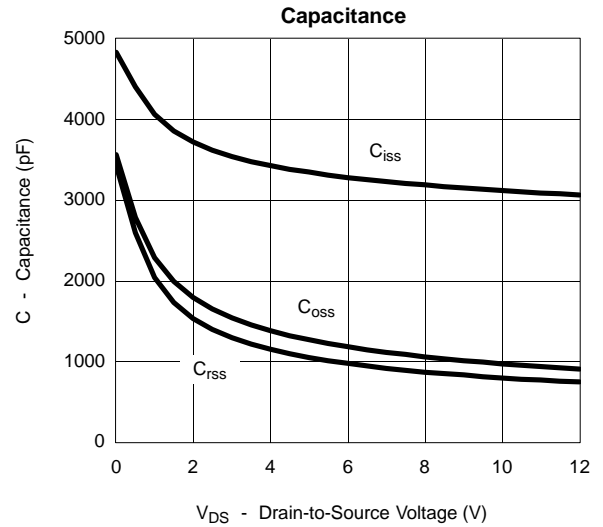
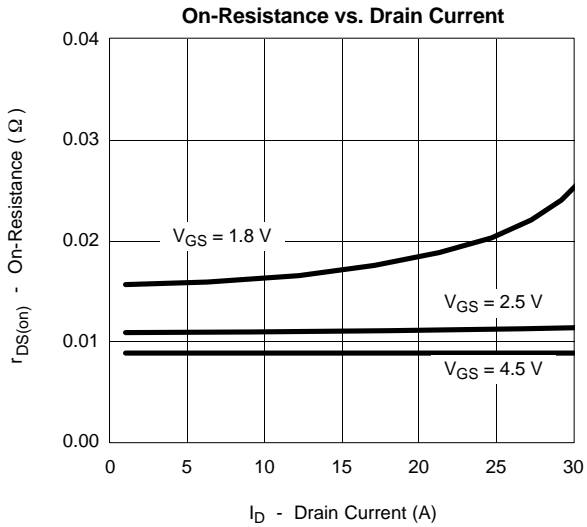
## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

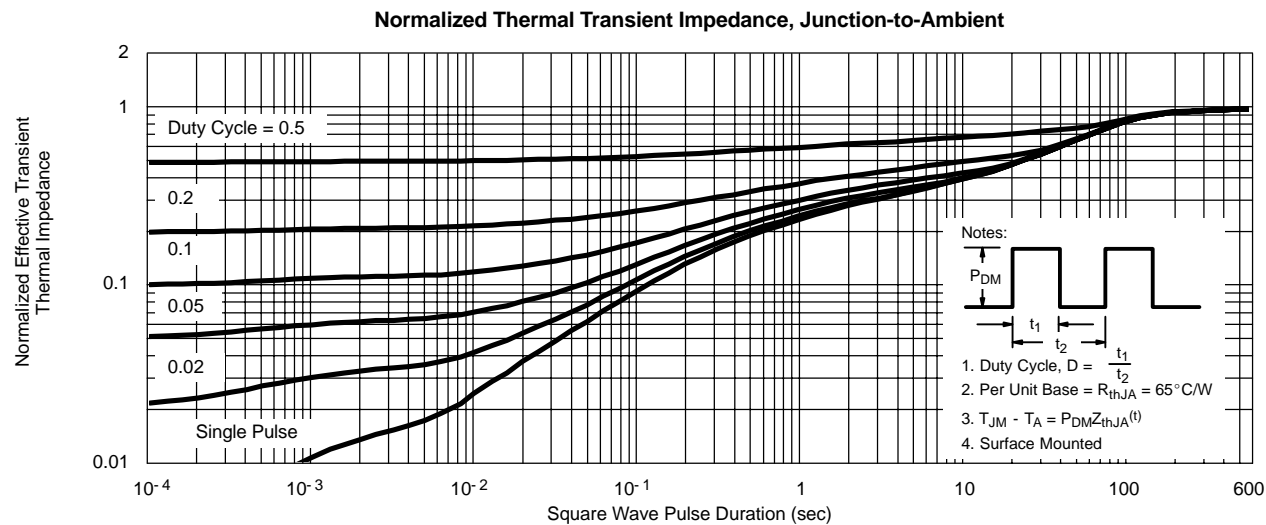
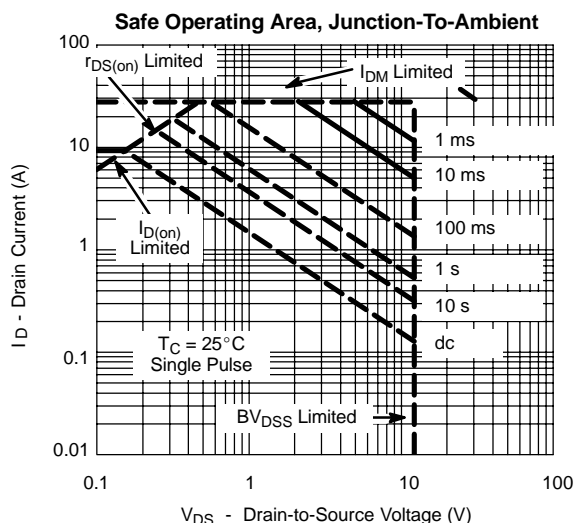
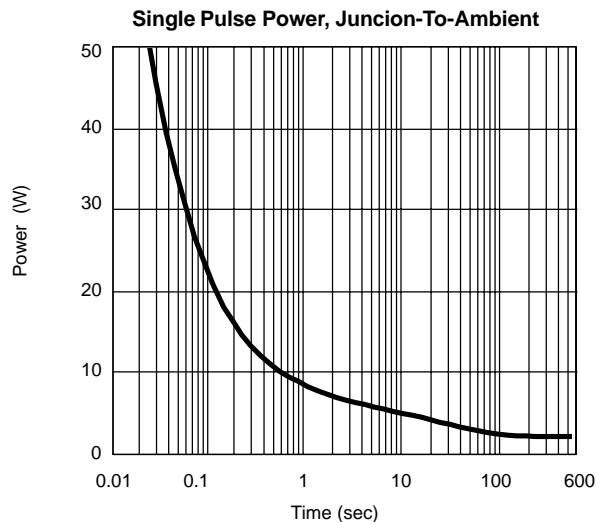
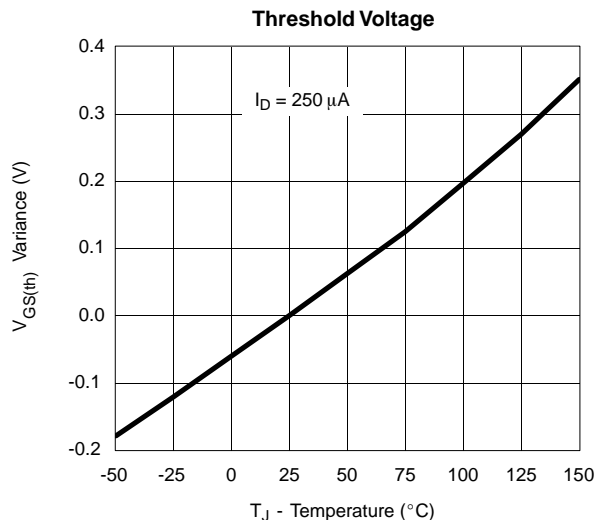
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



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