

## N-Channel 30-V (D-S) MOSFET

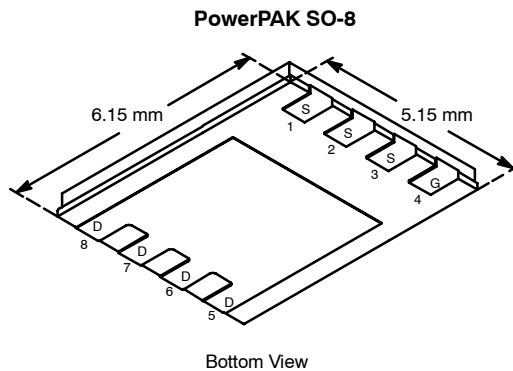
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.00325 @ $V_{GS} = 10$ V	30
	0.0042 @ $V_{GS} = 4.5$ V	27

### FEATURES

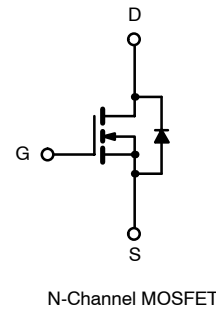
- Ultra-Low On-Resistance Using High Density TrenchFET® Gen II Power MOSFET Technology
- $Q_g$  Optimized
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100%  $R_g$  Tested

### APPLICATIONS

- Low-Side DC/DC Conversion
  - Notebook
  - Server
  - Workstation
- Synchronous Rectifier, POL



Ordering Information: Si7336DP-T1



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	30		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	30	18	A
		$T_A = 70^\circ\text{C}$	25	15	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse Width)	$I_{DM}$	70			
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	4.5	1.8		
Avalanche Current	$I_{AS}$	$L = 1.0$ mH	50		
Maximum Power Dissipation <sup>a</sup>			$T_A = 25^\circ\text{C}$	5.4	1.9
	$T_A = 70^\circ\text{C}$	3.4	1.2		
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	18	23	$^\circ\text{C/W}$
		Steady State	50	65	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.0	1.5		

Notes

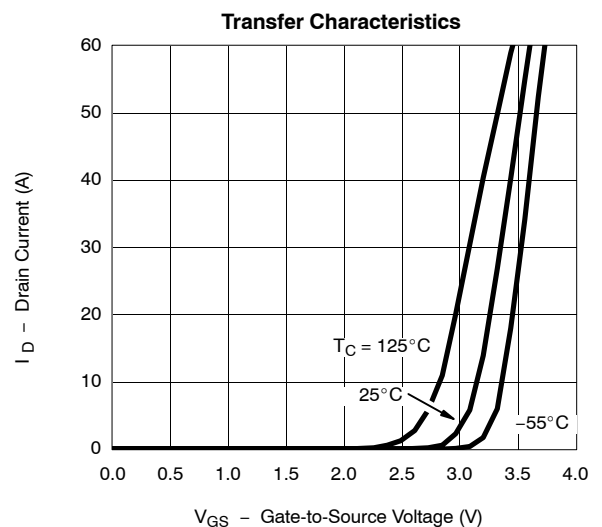
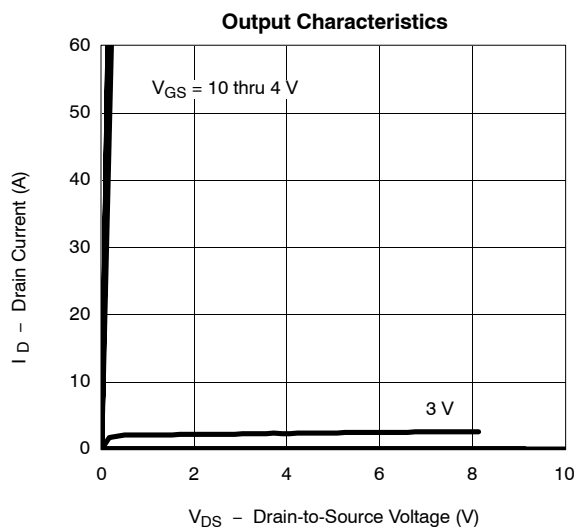
a. Surface Mounted on 1" x 1" FR4 Board.

**MOSFET SPECIFICATIONS ( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

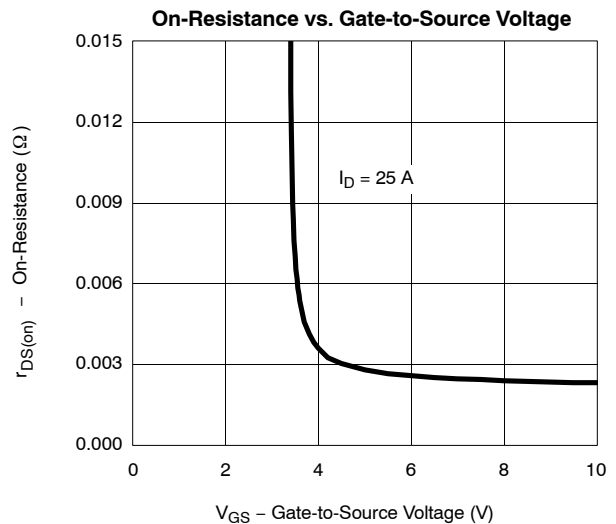
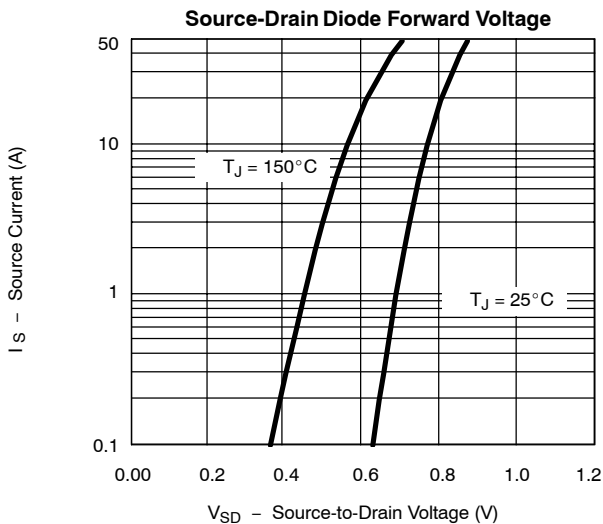
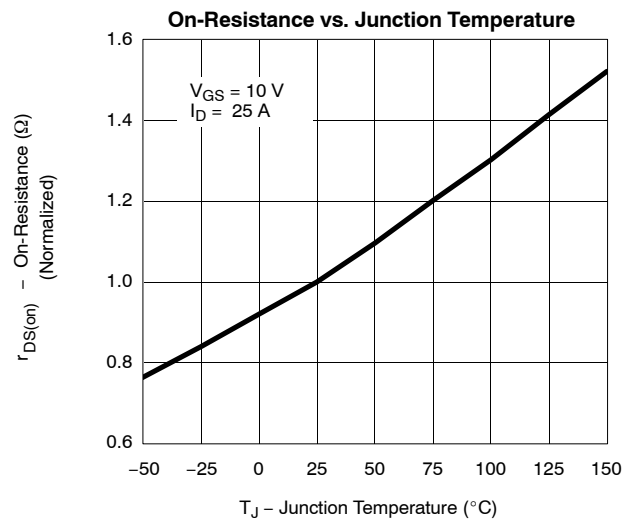
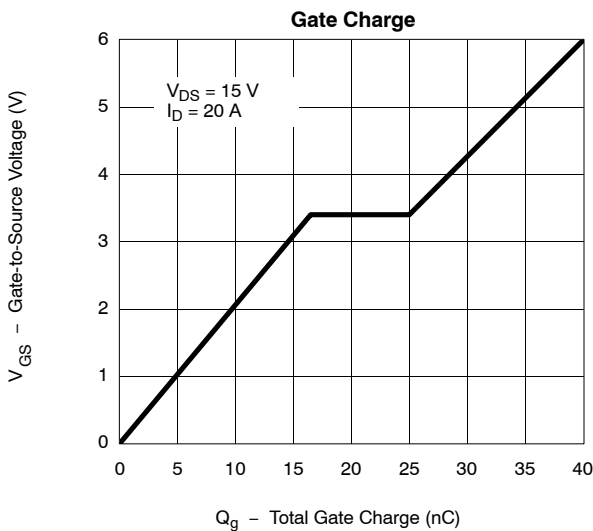
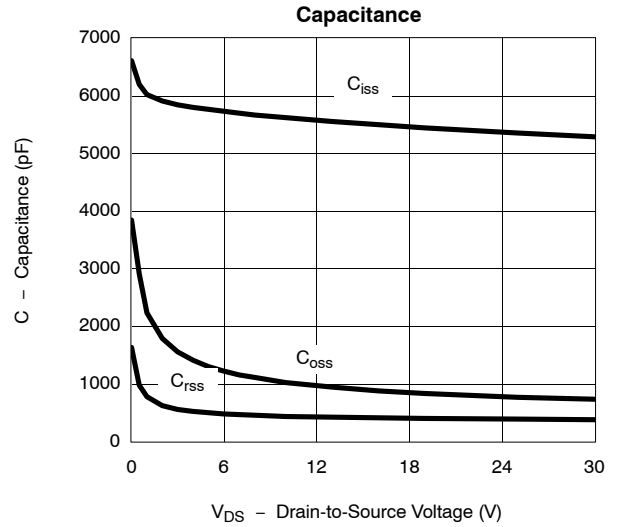
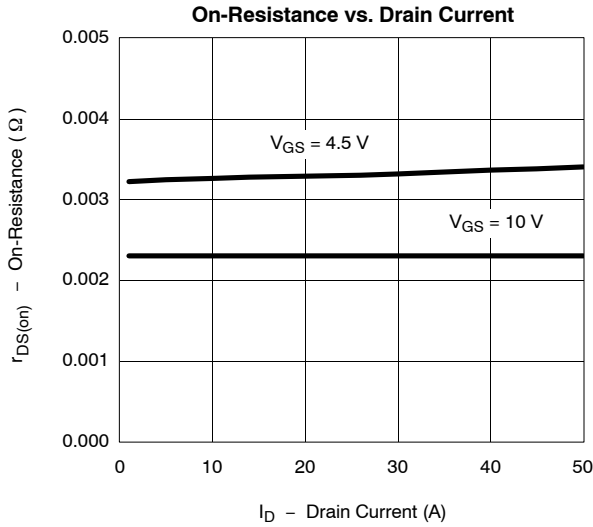
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}$		0.0026	0.00325	$\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 19 \text{ A}$		0.0033	0.0042	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 25 \text{ A}$		110		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.9 \text{ A}, V_{GS} = 0 \text{ V}$		0.72	1.1	V
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		5600		$\text{pF}$
Output Capacitance	$C_{oss}$			860		
Reverse Transfer Capacitance	$C_{rss}$			415		
Total Gate Charge	$Q_g$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		32	50	$\text{nC}$
Gate-Source Charge	$Q_{gs}$			16.5		
Gate-Drain Charge	$Q_{gd}$			8.5		
Gate Resistance	$R_g$		0.8	1.3	2.0	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15 \text{ V}, R_L = 15 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		24	35	$\text{ns}$
Rise Time	$t_r$			16	25	
Turn-Off Delay Time	$t_{d(off)}$			90	140	
Fall Time	$t_f$			32	50	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.9 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		45	70	

## Notes

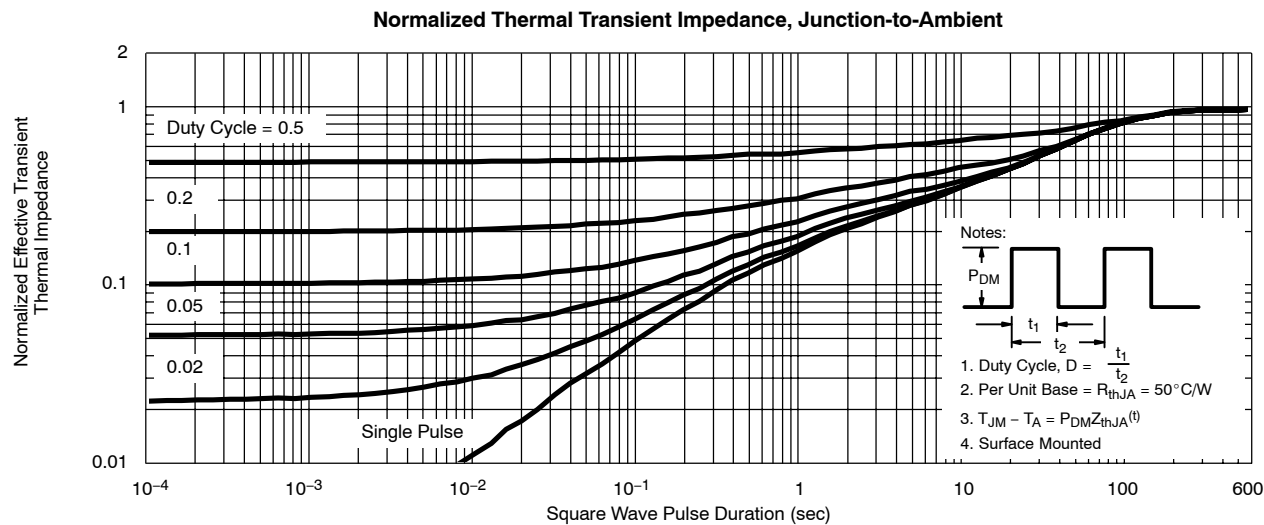
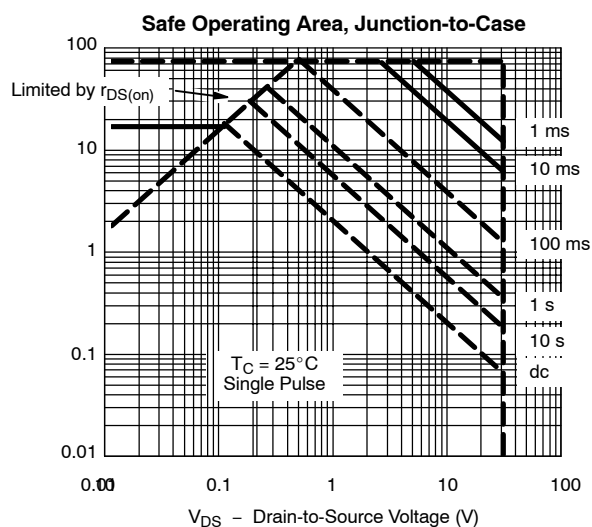
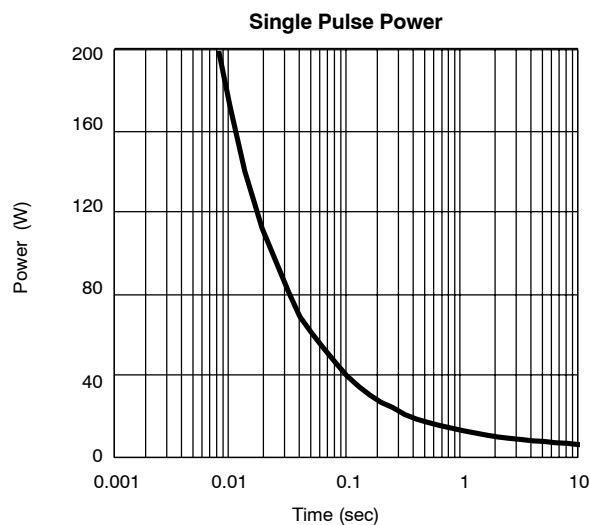
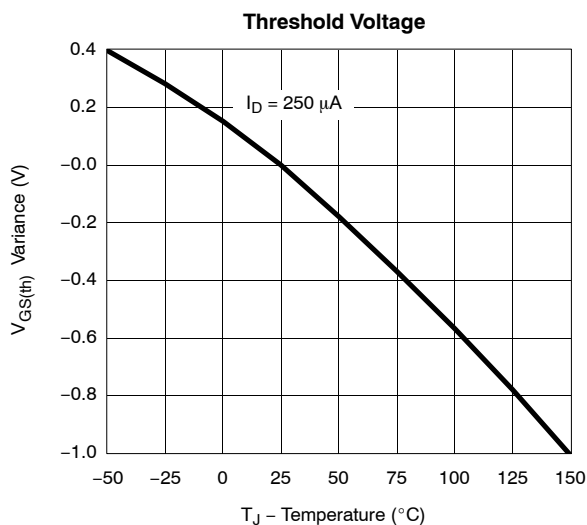
- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS ( $25^\circ\text{C}$  UNLESS NOTED)**

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