



#### **General Description**

The MAX2056 general-purpose, high-performance variable-gain amplifier (VGA) is designed to operate in the 800MHz to 1000MHz frequency range\*. This device features 15.5dB of gain, 4.5dB of noise figure, and an output 1dB compression point of 23.5dBm. The MAX2056 also provides an exceptionally high OIP3 level of 39dBm, which is maintained over the entire attenuation range. In addition, the on-chip analog attenuators yield infinite control and high attenuation accuracy over selectable 22dB or 44dB control ranges. Each of these features makes the MAX2056 an ideal VGA for cellular band GSM, cdma2000®, W-CDMA, and iDEN® transmitter and power amplifier AGC circuits.

The MAX2056 is pin compatible with the MAX2057 1700MHz to 2500MHz VGA, making this family of amplifiers ideal for applications where a common PC board layout is used for both frequency bands.

The MAX2056 operates from a single +5V supply and is available in a compact 36-pin thin QFN package (6mm x 6mm x 0.8mm) with an exposed pad. Electrical performance is guaranteed over the extended -40°C to +85°C temperature range.

#### **Applications**

GSM 850/GSM 900 2G and 2.5G EDGE Base-Station Transmitters and Power Amplifiers

Cellular cdmaOne™, cdma2000, and Integrated Digital Enhanced Network (iDEN) Base-Station Transmitters and Power Amplifiers

W-CDMA 850MHz and Other 3G Base-Station Transmitters and Power Amplifiers

Transmitter Gain Control

Receiver Gain Control

**Broadband Systems** 

Automatic Test Equipment

Digital and Spread-Spectrum Communication Systems

Microwave Terrestrial Links

cdmaOne is a trademark of CDMA Development Group. cdma2000 is a registered trademark of Telecommunications Industry Association.

iDEN is a registered trademark of Motorola, Inc.

#### **Features**

- ♦ 800MHz to 1000MHz RF Frequency Range\*
- ◆ 39dBm Constant OIP3 (Over All Gain Settings)
- ♦ 23.5dBm Output 1dB Compression Point
- ♦ 15.5dB Typical Gain at Maximum Gain Setting
- ♦ 0.15dB Gain Flatness Over 100MHz Bandwidth
- ♦ 4.5dB Noise Figure at Maximum Gain Setting (Using 1 Attenuator)
- ◆ Two Gain-Control Ranges: 22dB and 44dB
- **♦** Analog Gain Control
- ♦ Single +5V Supply Voltage
- ♦ Pin Compatible with MAX2057, 1700MHz to 2500MHz RF VGA
- **♦** External Current-Setting Resistors Provide Option for Operating VGA in Reduced-Power/Reduced-**Performance Mode**
- ♦ Lead-Free Package Available

#### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2056ETX	-40°C to +85°C	36 Thin QFN-EP** 6mm x 6mm	T3666-2
MAX2056ETX-T	-40°C to +85°C	36 Thin QFN-EP** 6mm x 6mm	T3666-2
MAX2056ETX+D	-40°C to +85°C	36 Thin QFN-EP** 6mm x 6mm	T3666-2
MAX2056ETX+TD	-40°C to +85°C	36 Thin QFN-EP** 6mm x 6mm	T3666-2

<sup>\*\*</sup>EP = Exposed paddle.

Pin Configuration/Functional Diagram appears at end of data sheet.

<sup>\*</sup>Note: Operation beyond this range is possible, but has not been characterized.

<sup>+ =</sup> Lead (Pb) free.

D = Drv pack.

T = Tape-and-reel package.

#### ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND	0.3V to +5.5V
VCNTL to GND (with VCC applied)	0 to 4.75V
Current into VCNTL Pin (VCC grounded)	40mA
All Other Pins to GND	-0.3V to (VCC + 0.3V)
RF Input Power (IN, IN_A, ATTN_OUT, OU	T_A)+20dBm
RF Input Power (AMP_IN)	+12dBm
θJA (natural convection)	35°C/W

θ <sub>JA</sub> (1m/s airflow)	31°C/W
θJA (2.5m/s airflow)	29°C/W
θ <sub>JC</sub> (junction to exposed paddle)	10°C/W
Operating Temperature Range	40°C to +85°C
Storage Temperature Range	65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +4.75V \text{ to } +5.25V, \text{ no RF signals applied, all input and output ports terminated with } 50\Omega, T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted.}$ 

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.75	5	5.25	V
Supply Current	$R1 = 1.2k\Omega$ , $R2 = 3.92k\Omega$ (Note 1)		136	167	mA
R <sub>SET1</sub> Current	$R1 = 1.2k\Omega \text{ (Note 1)}$		1		mA
R <sub>SET2</sub> Current	$R2 = 3.92k\Omega \text{ (Note 1)}$		0.33		mA
Gain-Control Voltage Range	(Note 2)	1.0		4.5	V
Gain-Control Pin Input Resistance	V <sub>CNTL</sub> = 1V to 4.5V	250	500		kΩ

#### **AC ELECTRICAL CHARACTERISTICS**

(Typical Operating Circuit with one attenuator connected,  $V_{CC} = +4.75V$  to +5.25V,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{CC} = +5.0V$ ,  $R1 = 1.2k\Omega$ ,  $R2 = 3.92k\Omega$ ,  $P_{OUT} = +5dBm$ ,  $f_{IN} = 900MHz$ ,  $V_{CNTL} = 1V$ ,  $50\Omega$  system impedance, second attenuator is not connected,  $T_A = +25^{\circ}C$ , unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Range			800		1000	MHz
Gain	$T_A = +25^{\circ}C$			15.5		dB
		V <sub>CNTL</sub> = 1V		+0.82		
	$T_A = +25^{\circ}C \text{ to } -40^{\circ}C$	V <sub>CNTL</sub> = 1.8V		+0.26		dB
	1A = +25 C t0 -40 C	$V_{CNTL} = 2.6V$		+0.25		
Mayinguna Cain Variation		$V_{CNTL} = 3.5V$		-0.18		
Maximum Gain Variation	T <sub>A</sub> = +25°C to +85°C	V <sub>CNTL</sub> = 1V		-0.51		
		$V_{CNTL} = 1.8V$		-0.11		
		$V_{CNTL} = 2.6V$		-0.16		
		$V_{CNTL} = 3.5V$		+0.09		
Reverse Isolation				29		dB
Noise Figure	(Note 4)			4.5		dB
Output 1dB Compression Point				+23.5		dBm
Output 2nd-Order Intercept Point	From maximum gain to 15dB attenuation, measured at f <sub>1</sub> + f <sub>2</sub> (Note 5)			+54		dBm
Output 3rd-Order Intercept Point	From maximum gain to 15dB attenuation (Note 5)			+39		dBm

#### **AC ELECTRICAL CHARACTERISTICS (continued)**

(Typical Operating Circuit with one attenuator connected,  $V_{CC}$  = +4.75V to +5.25V,  $T_A$  = -40°C to +85°C, unless otherwise noted. Typical values are at  $V_{CC}$  = +5.0V,  $R_1$  = 1.2k $\Omega$ ,  $R_2$  = 3.92k $\Omega$ ,  $R_2$  = 3.92k $\Omega$ ,  $R_3$  = 0.0MHz,  $R_3$  = 1.2k $R_3$  = 1.2k $R_3$  = 0.0MHz,  $R_3$  = 1.2k $R_3$  = 1

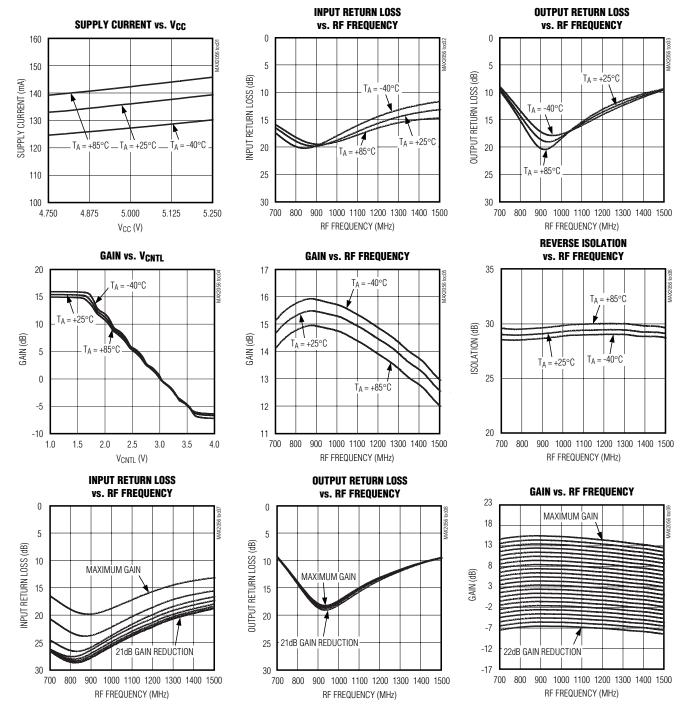
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output 3rd-Order Intercept Point	$T_A = +25^{\circ}C \text{ to } +85^{\circ}C$			-0.46		٩D
Variation Over Temperature	$T_A = +25^{\circ}C \text{ to } -40^{\circ}C$			+1.35		dB
2nd Harmonic	From maximum gain to 15dB attenuation, POUT = +5dBm			-55		dBc
3rd Harmonic	From maximum gain to 15dB attenuation, POUT = +5dBm			-68		dBc
DE Coin Control Dongs	f <sub>RF</sub> = 800MHz to 1000MHz,	One attenuator	18.3	22.3		dB
RF Gain-Control Range	V <sub>CNTL</sub> = 1V to 4.5V	Two attenuators	36.6	44.6		uВ
RF Gain-Control Slope				-10.7		dB/V
Maximum RF Gain-Control Slope	Maximum slope vs. gain-control voltage			-17.2		dB/V
Gain Flatness Over 100MHz Bandwidth	Peak-to-peak for all settings			0.15		dB
Attenuator Switching Time	15dB attenuation change (Note 6)			500		ns
Attenuator Insertion Loss	Second attenuator (IN_A, OUT_A)			1.7		dB
Input Return Loss	Entire band, all gain settings			15		dB
Output Return Loss	Entire band, all gain settings			15		dB
Group Delay	Input/output $50\Omega$ lines de-embedded			600		ps
Group Delay Flatness Over 100MHz Bandwidth	Peak to peak			100		ps
Group Delay Change vs. Gain Control	V <sub>CNTL</sub> = 1V to 4V			100		ps
Insertion Phase Change vs. Gain Control	V <sub>CNTL</sub> = 1V to 4V			20		degrees

- Note 1: Total supply current reduces as R1 and R2 are increased.
- Note 2: Operating outside this range for extended periods may affect device reliability. Limit pin input current to 40mA when V<sub>CC</sub> is not present.
- Note 3: All limits include external component losses, unless otherwise noted.
- Note 4: Noise figure increases by approximately 1dB for every 1dB of gain reduction.
- **Note 5:**  $f_1 = 900MHz$ ,  $f_2 = 901MHz$ , +5dBm/tone at OUT.
- Note 6: Switching time is measured from 50% of the control signal to when the RF output settles to ±1dB.

#### Typical Operating Characteristics

#### **One Attenuator Configuration**

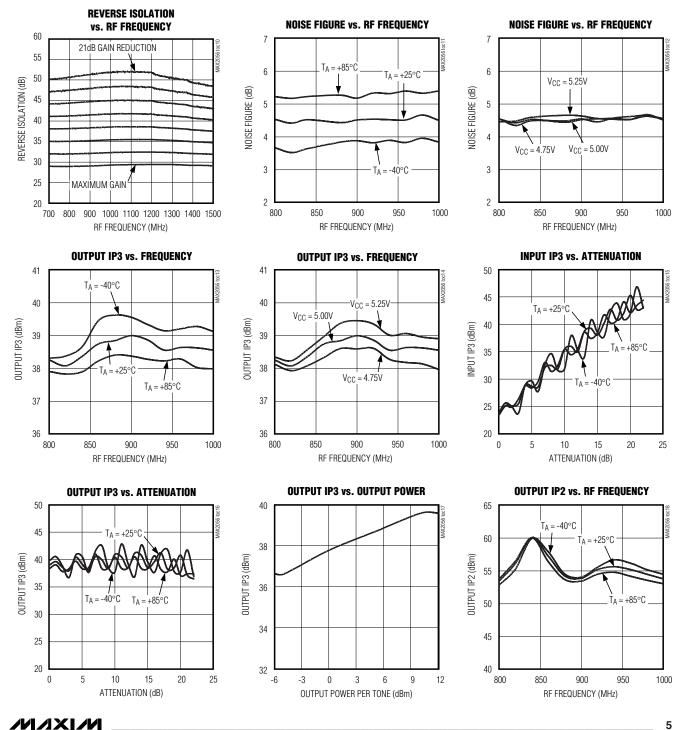
(Typical Application Circuit with **one attenuator** connected,  $V_{CC} = +5.0V$ ,  $R1 = 1.2k\Omega$ ,  $R2 = 3.92k\Omega$ ,  $f_{1N} = 900MHz$  maximum gain setting,  $P_{OUT} = +5dBm$ , linearity measured at  $P_{OUT} = +5dBm$ /tone,  $T_{A} = +25^{\circ}C$ , unless otherwise noted.)



### Typical Operating Characteristics (continued)

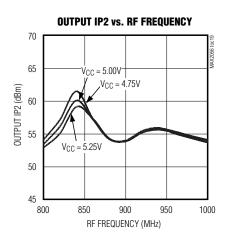
One Attenuator Configuration

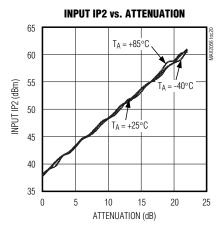
(Typical Application Circuit with **one attenuator** connected,  $V_{CC} = +5.0V$ ,  $R1 = 1.2k\Omega$ ,  $R2 = 3.92k\Omega$ ,  $f_{1N} = 900MHz$  maximum gain setting,  $P_{OUT} = +5dBm$ , linearity measured at  $P_{OUT} = +5dBm/t$ one,  $T_{A} = +25^{\circ}C$ , unless otherwise noted.)

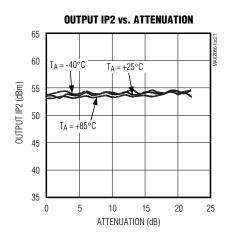


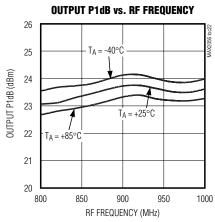
### Typical Operating Characteristics (continued) One Attenuator Configuration

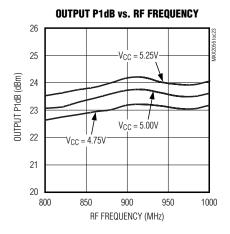
(Typical Application Circuit with **one attenuator** connected,  $V_{CC} = +5.0V$ ,  $R1 = 1.2k\Omega$ ,  $R2 = 3.92k\Omega$ ,  $f_{IN} = 900MHz$  maximum gain setting,  $P_{OUT} = +5dBm$ , linearity measured at  $P_{OUT} = +5dBm$ /tone,  $T_{A} = +25^{\circ}C$ , unless otherwise noted.)







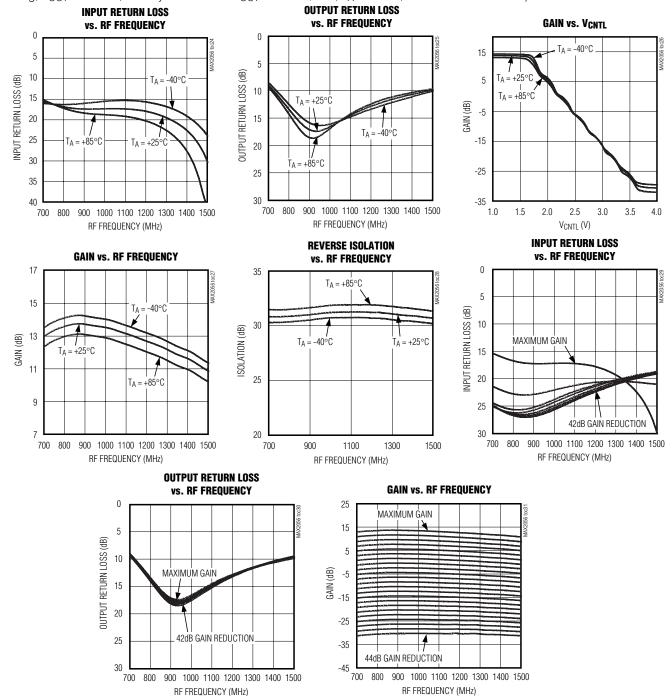




#### **Typical Operating Characteristics**

#### Two Attenuator Configuration

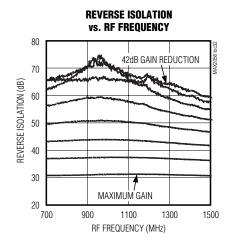
(Typical Application Circuit with **two attenuators** connected,  $V_{CC} = +5.0V$ ,  $R1 = 1.2k\Omega$ ,  $R2 = 3.92k\Omega$ ,  $f_{|N} = 900MHz$  maximum gain setting,  $P_{OUT} = +5dBm$ , linearity measured at  $P_{OUT} = +5dBm/t$ one,  $T_{A} = +25^{\circ}C$ , unless otherwise noted.)

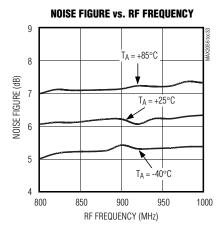


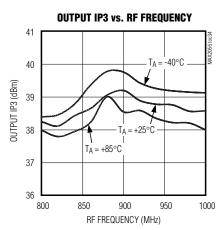
#### Typical Operating Characteristics (continued)

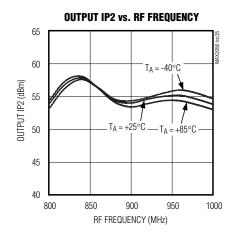
#### **Two Attenuator Configuration**

(Typical Application Circuit with **two attenuators** connected,  $V_{CC} = +5.0V$ ,  $R1 = 1.2k\Omega$ ,  $R2 = 3.92k\Omega$ ,  $f_{IN} = 900MHz$  maximum gain setting,  $P_{OUT} = +5dBm$ , linearity measured at  $P_{OUT} = +5dBm$ /tone,  $T_{A} = +25^{\circ}C$ , unless otherwise noted.)









### Pin Description

PIN	NAME	FUNCTION
1, 3, 4, 6, 7, 9, 10, 12, 14, 18, 19, 21–24, 27, 28, 30, 31, 33, 34, 36	GND	Ground. Connect to the board's ground plane using low-inductance layout techniques.
2	OUT_A	Second-Attenuator Output. Internally matched to $50\Omega$ over the operating frequency band. Connect to IN through a DC-blocking capacitor if greater than 22dB of gain-control range is required. No connection is required if the second attenuator is not used.
5, 13, 16, 25, 32	Vcc	Power Supply. Bypass each pin to GND with capacitors as shown in the <i>Typical Application Circuit</i> . Place capacitors as close to the pin as possible.
8	IN_A	Second-Attenuator Input. Internally matched to $50\Omega$ over the operating frequency band. Connect to a $50\Omega$ RF source through a DC-blocking capacitor if greater than 22dB of gain-control range is required. No connection is required if the second attenuator is not used.
11	VCNTL	Analog Gain-Control Input. Limit voltages applied to this pin to a 1V to 4.5V range when V <sub>CC</sub> is present to ensure device reliability.
15	R <sub>SET1</sub>	First-Stage Amplifier Bias-Current Setting. Connect to GND through a 1.2kΩ resistor.
17	R <sub>SET2</sub>	Second-Stage Amplifier Bias-Current Setting. Connect to GND through a $3.92 k\Omega$ resistor.
20	OUT	RF Output. Internally matched to $50\Omega$ over the operating frequency band. Requires a DC-blocking capacitor.
26	AMP_IN	Amplifier Input. Internally matched to $50\Omega$ over the operating frequency band. Connect to ATTN_OUT through a DC-blocking capacitor.
29	ATTN_OUT	Attenuator Output. Internally matched to $50\Omega$ over the operating frequency band. Connect to AMP_IN through a DC-blocking capacitor.
35	IN	RF Input. Internally matched to $50\Omega$ over the operating frequency band. Connect to a $50\Omega$ RF source through a DC-blocking capacitor if the second attenuator is not used.
Exposed Paddle	GND	Exposed Paddle Ground Plane. This paddle affects RF performance and provides heat dissipation. This paddle <b>MUST</b> be soldered evenly to the board's ground plane for proper operation.

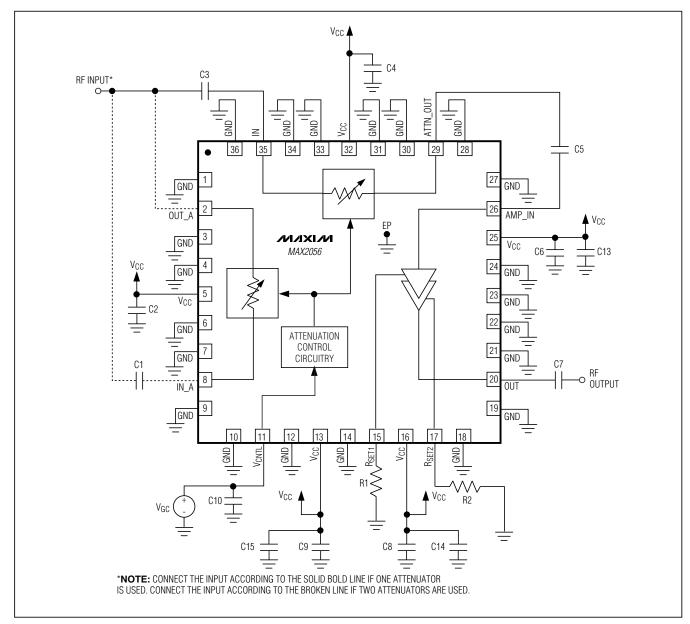


Figure 1. Typical Application Circuit

#### Detailed Description

The MAX2056 general-purpose, high-performance VGA with analog gain control is designed to interface with  $50\Omega$  systems operating in the 800MHz to 1000MHz frequency range.

The MAX2056 integrates two attenuators to provide 22dB or 44dB of precision analog gain control, as well

as a two-stage amplifier that has been optimized to provide high gain, high IP3, low noise figure, and low-power consumption. The bias current of each amplifier stage can be adjusted by individual external resistors to further reduce power consumption for applications that do not require high linearity.

Table 1. Typical Application Circuit Components Values

DESIGNATION	VALUE	TYPE
C1, C3, C5, C10	47pF	Microwave capacitors (0402)
C2, C4, C6, C8, C9	1000pF	Microwave capacitors (0402)
C7	3.9pF	Microwave capacitor (0402)
C13, C14, C15	0.1µF	Microwave capacitors (0603)
R1	1.2kΩ	±1% resistor (0402)
R2	$3.92$ k $\Omega$	±1% resistor (0402)

### Applications Information Analog Attenuation Control

A single input voltage at the V<sub>CNTL</sub> pin adjusts the gain of the MAX2056. Up to 22dB of gain-control range is provided through a single attenuator. At the maximum gain setting, each attenuator's insertion loss is approximately 1.7dB. With the single attenuator at the maximum gain setting, the device provides a nominal 15.5dB of cascaded gain and 4.5dB of cascaded noise figure.

If a larger gain-control range is desired, a second onchip attenuator can be connected in the signal path to provide an additional 22dB of gain-control range. With the second attenuator connected at the maximum gain setting, the device typically exhibits 13.8dB of cascaded gain. Note that the V<sub>CNTL</sub> pin simultaneously adjusts both on-chip attenuators. The VCNTL input voltage drives a high-impedance load (>250k $\Omega$ ). It is suggested that a current-limiting resistor be included in series with this connection to limit the input current to less than 40mA should the control voltage be applied when VCC is not present. A series resistor of greater than  $200\Omega$ will provide complete protection for 5V control voltage ranges. Limit VCNTL input voltages to a 1.0V to 4.5V range when VCC is present to ensure the reliability of the device.

#### **Amplifier Bias Current**

The MAX2056 integrates a two-stage amplifier to simultaneously provide high gain and high IP3. Optimal per-

formance is obtained when R1 and R2 are equal to  $1.2 k\Omega$  and  $3.92 k\Omega$ , respectively. The typical supply current is 136mA and the typical output IP3 is 39dBm under these conditions.

Increasing R1 and R2 from the nominal values of  $1.2k\Omega$  and  $3.92k\Omega$  reduces the bias current of each amplifier stage, which reduces the total power consumption and IP3 of the device. This feature can be utilized to further decrease power consumption for applications that do not require high IP3.

#### **Layout Considerations**

A properly designed PC board is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For best performance, route the ground-pin traces directly to the exposed pad underneath the package. This pad **MUST** be connected to the ground plane of the board by using multiple vias under the device to provide the best RF and thermal conduction path. Solder the exposed pad on the bottom of the device package to a PC board exposed pad.

#### **Power-Supply Bypassing**

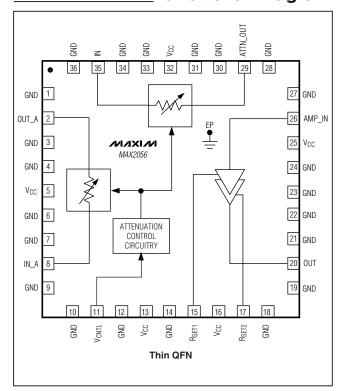
Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each V<sub>CC</sub> pin with capacitors placed as close to the device as possible. Place the smallest capacitor closest to the device. Refer to the MAX2056 evaluation kit data sheet for more details.

### **Exposed Paddle RF and Thermal Considerations**

The EP of the MAX2056's 36-pin thin QFN-EP package provides a low-thermal-resistance path to the die. It is important that the PC board on which the IC is mounted be designed to conduct heat from this contact. In addition, the EP provides a low-inductance RF ground path for the device.

The EP **MUST** be soldered to a ground plane on the PC board either directly or through an array of plated via holes. Soldering the pad to ground is also critical for efficient heat transfer. Use a solid ground plane wherever possible.

#### Pin Configuration/ Functional Diagram



#### \_Chip Information

TRANSISTOR COUNT: 5723

PROCESS: BICMOS

#### Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

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