CDB61318

E1 Long Haul Line Interface Unit

Features

- Socketed CS61318 Line Interface
- All Required Components for CS61318 Evaluation
- LED Status Indications for Alarm Conditions and Operating Status
- Support for Hardware and Host Modes

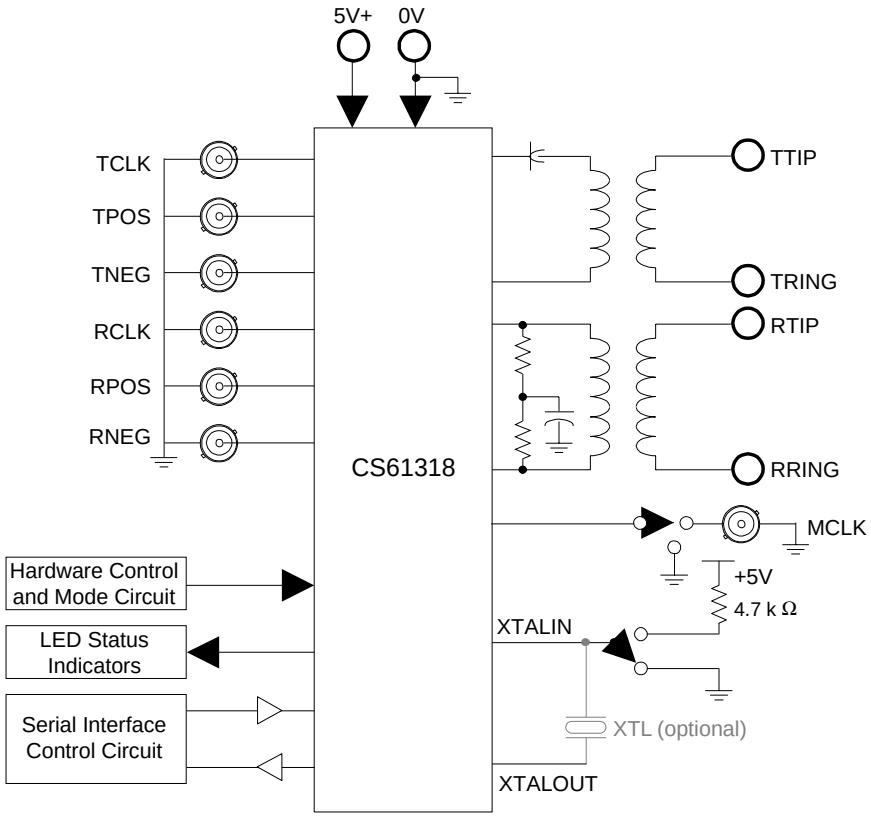
Description

The evaluation board includes a socketed CS61318 line interface device and all support components necessary for evaluation. The board is powered by an external +5 Volt supply.

The board may be configured for 75 Ω coax E1 or 120 Ω twisted-pair E1 operations. Binding posts and bantam jacks are provided for the line interface connections. Several BNC connectors provide clock and data I/O at the system interface. Reference timing may be derived from a quartz crystal or an external reference clock. Four LED indicators monitor device alarm conditions and operating status.

ORDERING INFORMATION

CDB61318



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Contacting Cirrus Logic Support

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1. POWER SUPPLY

As shown on the evaluation board schematic in Figure 1, power is supplied to the board from an external +5 Volt supply connected to the two binding posts labeled V+ and GND. Zener diode Z1 protects the components on the board from reversed supply connections and over-voltage damage. Capacitor C1 provides power supply decoupling and ferrite bead L1 helps isolate the CS61318 and buffer supplies. The 0.1 µF capacitors decouple their respective ICs. Ferrite bead L7 helps isolates the devices U2, U3 and U4.

2. BOARD CONFIGURATION

Slide switch S1 selects hardware, host or hardware-coder mode operation by sliding it into HW, SW or HWCDR positions, respectively.

2.1 Hardware Mode

In Hardware mode operation, the evaluation board is configured using the DIP switch SW1. In this mode, the switch establishes the digital control inputs for both line interface channels. Closing a DIP switch away from the label sets the CS61318 control pin of the same name to a logic 1. The host processor interface J1 should not be used in the Hardware mode.

The CDB61318 switches and functions are listed below:

- TAOS: transmit all ones;
- LLOOP: local loopback;
- RLOOP: remote loopback;
- JASEL: jitter attenuator path selection;

All switch inputs are pulled-high using resistor R13 when the switch is closed.

2.1.1 Network Loopback

NLOOP is enabled in the hardware mode by shorting HDR11 (HW_NLOOP) and then pressing S2. It can also be done by closing the switches RLOOP, LLOOP and TAOS on SW1, pulling them high, and then pulling them back to low by opening the RLOOP, LLOOP and TAOS switches. NLOOP can then be turned on by sending the 1:4 pattern to the receive input RTIP and RRING for five seconds. The NLOOP LED will light up at this point if HDR6 is jumped to NLOOP_LED position. NLOOP can be turned off by sending a 1:2 pattern to RTIP and RRING for five seconds.

2.2 Hardware-Coder Mode

This mode is essentially the same as the Hardware mode with the HDB3 encoder/decoder enabled.

2.3 Host Mode

In Host mode operation, the evaluation board supports serial-port operation over interface port J1 using the printer port of a host PC running the enclosed software. The evaluation board is connected to the host PC using a standard DB-25 male-to-female cable (included). Ferrite beads L2-L6 help reduce incoming noise from the host interface. The SW1 switch must be open to enable serial port operation.

An external microprocessor may also interface to the serial port of the CS61318 through HDR12. HDR6 must be jumpered so the interrupt pin, $\overline{\text{INT}}$, Comes out to HDR12.

3. TRANSMIT CIRCUIT

The transmit clock and data signals are supplied on BNC inputs labeled TCLK, TPOS, and TNEG. In Hardware and Host mode (with coder mode disabled), data is supplied on the TPOS and TNEG BNC inputs. In Host mode with coder mode enabled, data is supplied on the TDATA BNC input.

The transmitter output is transformer coupled to the line through the step-up transformer T2. The signal is available at either the Transmit binding posts (J11, J13) or the Transmit bantam jack. Capacitor C12 prevents output stage imbalances from producing a DC current that may saturate the transformer, thus degrading its performance.

4. RECEIVE CIRCUIT

The receive signal is input at either the Receive binding posts (J4, J10) or the Receive bantam jack. The receive signal is transformer coupled to the CS61318 through the transformer T1.

The receive line is terminated by resistors R1-R2 to provide impedance matching and receiver return loss. They are socketed so the values may be changed according to the application. The evaluation board is supplied from the factory with 60 Ω resistors for terminating 120 Ω twisted-pair lines, and 37.5 Ω resistors for terminating 75 Ω coaxial cables. Capacitor C3 provides an AC ground reference for the differential input.

The recovered clock and data signals are available on BNC outputs labeled RCLK, RPOS, and RNEG. In Hardware and Host mode (with coder mode disabled), data is available on the RPOS and RNEG BNC. With coder mode enabled, data is available on the RDATA BNC output in unipolar format and bipolar violations are reported on the RNEG BNC connector.

5. REFERENCE CLOCK

The CDB61318 requires an E1 reference clock for operation. This clock can be supplied by either a quartz crystal or an external reference. The evaluation board is supplied from the factory with a quartz crystal. In the case that both the external reference and the quartz crystal are applied, the external reference takes precedence.

5.1 Quartz Crystal

A quartz crystal may be inserted at socket Y1. The quartz crystals operate at 4X the frequency of operation: 8.192 MHz.

5.2 External Reference

An external reference of 2.048 MHz may be provided at the REFCLK BNC input. Header HDR7 must be jumpered in the "MCLK" position to provide connectivity to the MCLK pin of the CS61318.

5.3 LED Indicators

The four-LED pack D1 indicates signal states on LATN1, LATN2, LOS and NLOOP. The LOS LED indicator illuminates when the line interface receiver has detected a loss of signal. The NLOOP LED indicates if Network Loopback is in operation. The LATN1/LATN2 LED's indicate the attenuation level of the received signal; reading how much the incoming signal is below the nominal expected signal level. See Table 1 for details.

6. BUFFERING

Buffer U2 provides additional drive capability for the SW1 and Host mode connections. The buffer outputs are filtered with an (optional) RC network (not initially populated) to reduce the transients caused by buffer switching.

7. TRANSFORMER SELECTION

The evaluation board is supplied from the factory with PE-64936 (1:1), PE-65351 (1:2) and T-1229 (1:1.58) transformers by Pulse Engineering. The socket T1 on the board is for receive side transformer and T2 is for the transmit side. Please see Table 2 for details on transformers selection.

LATN1	LATN2	Attenuation Level (dB)
ON	ON	0
OFF	OFF	9.5
ON	OFF	19.5
OFF	ON	28.5

Table 1. LATN Settings

8. PROTOTYPING AREA

An ample prototyping area with power supply and ground connections is provided on the evaluation board. This area can be used to develop and test a variety of additional circuits such as framer devices, system synchronizer PLLs, or specialized interface logic.

9. EVALUATION HINTS

1) The orientation of pin 1 for the CS61318 is marked by a small circle on the top-left side of the socket U1.
2) Component locations R1-R2, R3-R4, Y1, T1 and T2 must have the correct values installed according to the application. All the necessary components are included with the evaluation board.
3) Closing a DIP switch on SW1 away from the label sets the CS61318 control pin of the same name to logic 1.
4) When performing a manual loopback of the recovered signal to the transmit signal at the BNC connectors, the recovered data must be valid on the falling edge of RCLK to properly latch the data in the transmit direction.
5) Jumpers can be placed on header HDR4 to provide a ground reference on TRING for 75 Ω coax E1 applications.

Properly terminate TTIP/TRING when evaluating the transmit output pulse shape. For more information concerning pulse shape evaluation, refer to the Crystal application note entitled "Measurement and Evaluation of Pulse Shapes in T1/E1 Transmission Systems."

Mode	TX Transformer	RX Transformer	R1-R2	R3-R4
E1 (120 Ω)/LH	1:2	1:1	60 Ω	15 Ω
E1 (75 Ω)/SH	1:1.58	1:1	37.5 Ω	15 Ω

Table 2. Transformer and Resistor Options
SH=Short Haul; LH = Long Haul;
* Default setting from the factory

Jumper	Position	Junction Selected
HDR4	IN	Grounds TRING on the line side of the transmit transformer
HDR5	IN	Grounds the line side of RRING through C2
HDR6	INT	Host Mode operation, connects INT pin to the serial interface
	NLOOP_LED	Hardware Mode operation, connects NLOOP pin to the LED
HDR7	GND	Grounds the MCLK pin
	MCLK	Connects the MCLK pin to the BNC
HDR8	IN	Pulls the TNEG pin high, for selecting the coder mode (TCLK has to be present for selecting the coder mode)
HDR9	XTAL-HI	Pulls the pin XTALIN high
	XTAL-GND	Pulls the pin XTALIN to ground
HDR10	X	Don't care (shorted)
HDR11	OUT	Allows S2 to pull RLOOP and LLOOP high for RESET in hardware mode
	IN	Allows S2 to pull RLOOP, LLOOP, and TAOS high for enabling NLOOP in hardware mode
HDR12	X	Provides access to the serial port signals

Table 3. Jumper Selections

10. CDB61318 SOFTWARE

The CDB61318 can be configured in the host/software mode using the application CDB61318.EXE supplied with the board. This application allows the user to access all of the user programmable registers in the device. It runs under Windows 95 and 98.

10.1 Configure PC

This function allows the user to set the address of the PC parallel port. The selection depends on the configuration of the user's PC. The Plug and Play (PnP) function of the operating system determines this address every time the PC is powered up, but it normally won't change the printer port address unless the configuration of the hardware has changed since the PC was last powered up. There are two ways to determine the address of the parallel port: the safe method and the fast method.

The safe method is to double click on the My Computer icon on the desktop, double click on Control panel, then Double click on System. Select the Device Manager tab. Select "View devices by type" in the window that pops up, then double click on "Ports (COM & LPT)". Click on the Printer Port icon that corresponds to the port that is connected to the CDB61318 evaluation board, then select Properties. On the Properties window, select the Resources tab, then read the I/O address in the Input/Output Range field. This is the address range to select for the CDB61318.

The fast method is to use the pull down menu in Configure Part to try the ports one by one, then clicking on the Read Registers button. When the wrong address is selected, the bit fields in this window will read either all zeroes or all ones. The user must be careful when using this method because entering the Configure Part window automatically issues a read command to the device. This will cause unpredictable results if the selected LPT port is connected to some device other than a CDB61318 evaluation board. Before using this method, the user should disconnect all other devices from the LPT ports.

10.2 Configure Part

Clicking on Configure_Part brings up two options: the first is Control Register Configuration, which gives access to the control and status registers, and Transmitter RAM Configuration, which configures the Arbitrary Waveform Generator (AWG). See the CS61318 data sheet for information on programming these registers.

10.3 Control Register Configuration

Selecting Control Register Configuration pulls up the register configuration window and automatically issues a read command to the CDB61318; the user must make sure that the software is configured to use the proper LPT port before this option is selected (see Configure PC above).

The register configuration window is shown in Figure 1. The bits in the Control Registers (CNTL REG 1, CNTL REG 2, CNTL REG 3) are written by checking the box opposite to the individual bits in the "Write" columns, then clicking on the "Write Registers" button. This writes the displayed data to all three control registers, then automatically reads the control and status registers and displays the results in the "Read" columns. Since Control Register 1 is effectively a control register when it is written and a status register when it is read, the read status is decoded and displayed in the Read Status window.

The registers can also be read by clicking on the "Read Registers" button. All five registers are read when this command is selected.

The LATN REG register shows the current setting of the gain-equalizer.

10.4 Transmitter Ram Configuration

When this command is selected, the software pops up a window which displays the contents of the

AWG RAM (see Figure 2). Notice the six buttons along the bottom of this window.

Modify Unit Interval brings up the Transmitter RAM UI Config window, which allows the user to edit the contents of the AWG registers. It is described in the following section.

Read from File reads previously generated data from a file.

Load to File writes the currently displayed data into a file for later recovery using the Read from File command.

Read from RAM reads the current data from the AWG RAM and displays it in the current window.

Write to RAM writes the displayed data to the AWG RAM. This must be done before exiting to write the data to the device.

Exit returns control to the main CDB61318 menu. It does not automatically write the data to the CS61318.

10.5 Modify Unit Interval

The user modifies the data in the AWG RAM using the Transmitter RAM UI Config window (see Figure 3). At the top of this window are three radio buttons used for selecting one of the three unit intervals. After having selected the desired UI, clicking on the Read button will display the contents of the given waveform in the Time Slot fields. These values are displayed in hexadecimal format. The user can modify these values by clicking on the se-

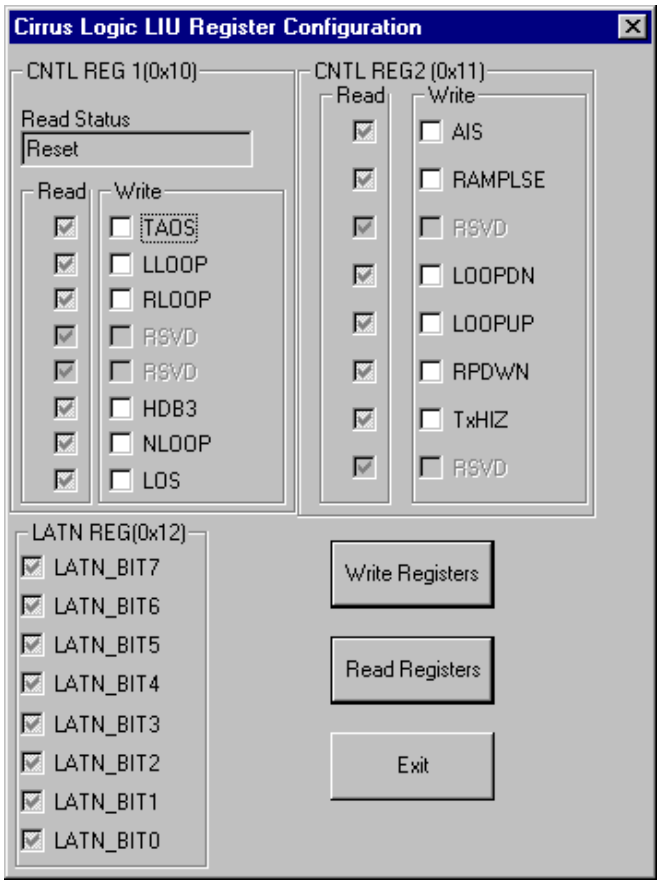


Figure 1. Register Configuration Window

lection arrow and scrolling up and down through the possible values. After making the necessary modifications, the user clicks the “Save to UI” button to save the data for that UI to the PC’s memory. When all three UI’s have been saved, the new values are written to the AWG RAM on the device by going back to the Transmitter RAM Configuration window and clicking on the Write to RAM button.

These settings are reset to the initial state when the window is closed. The Save Screen and Restore Scrn buttons must be used if the user wishes to exit this window and come back to the same setup.

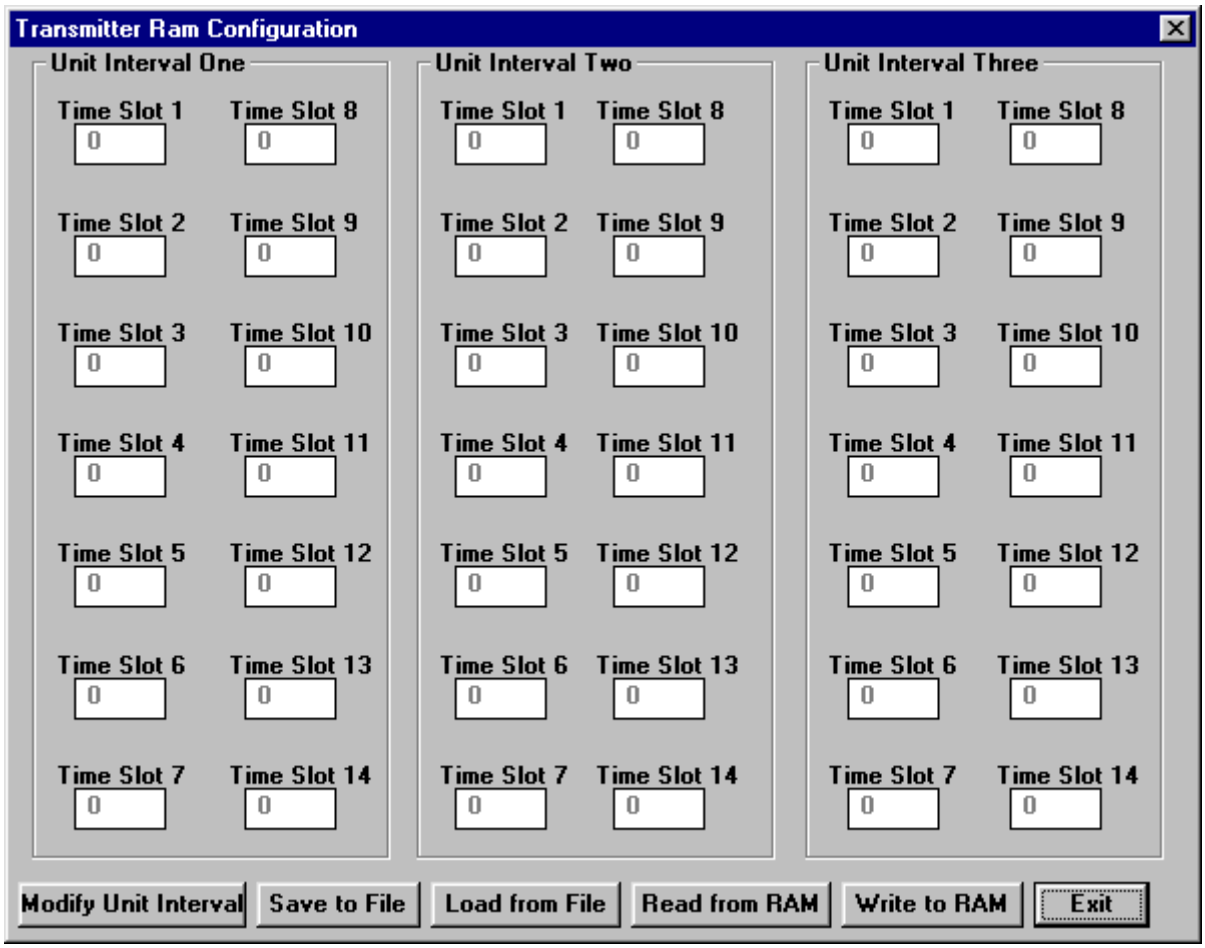


Figure 2. Transmitter RAM Configuration Window

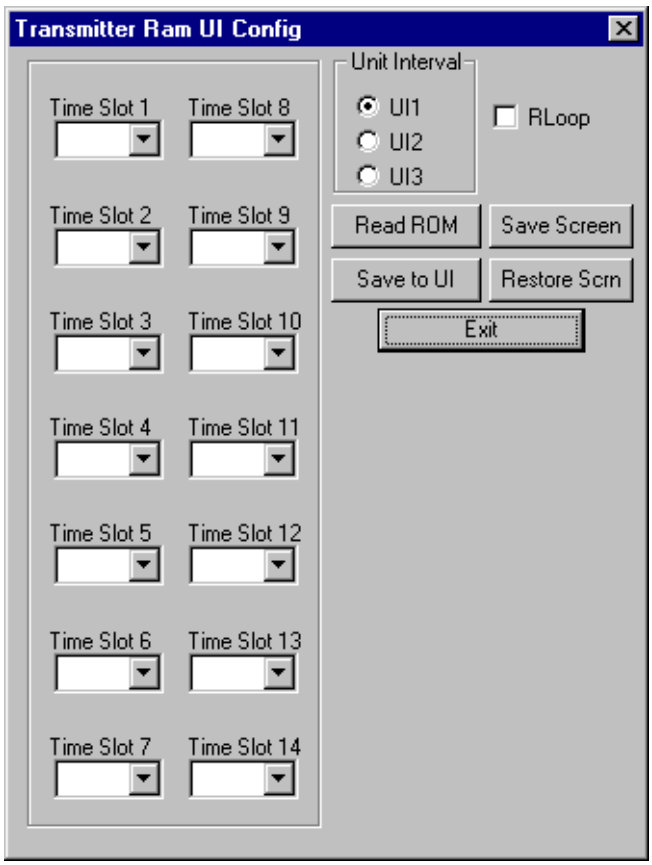


Figure 3. Modify Unit Interval Window

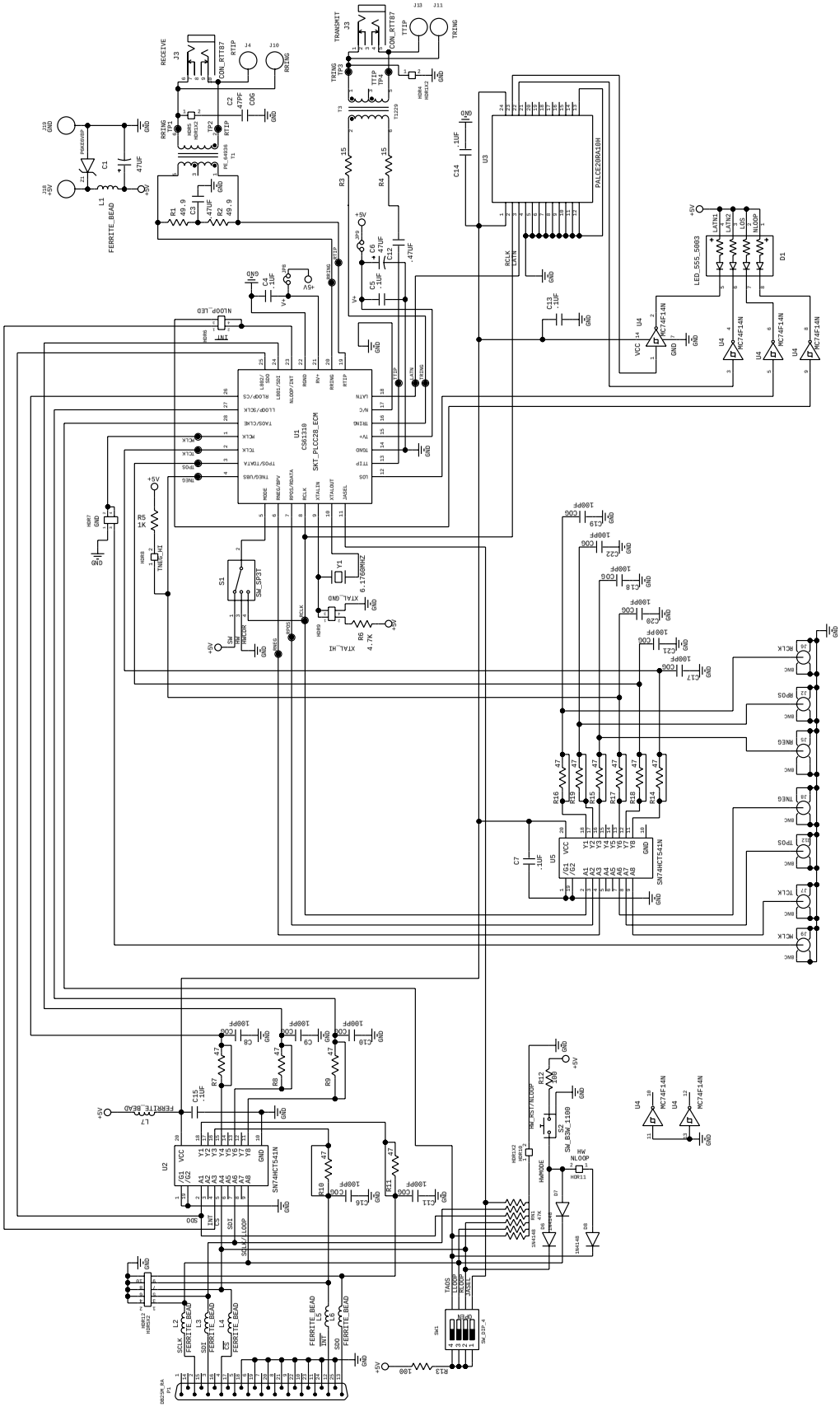


Figure 4. CDB61318 Evaluation Board Schematic

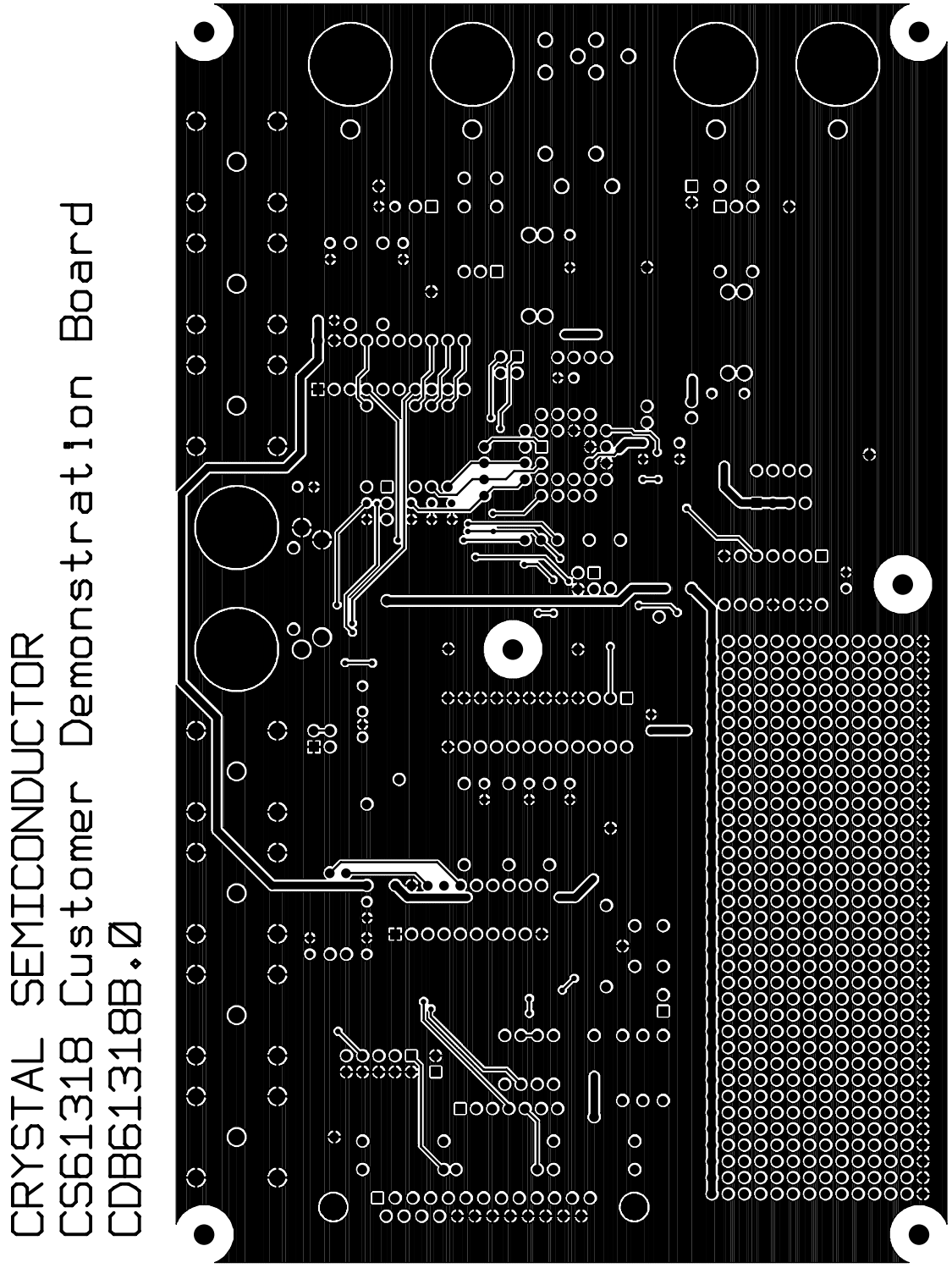


Figure 5. Board Layout - Top Layer

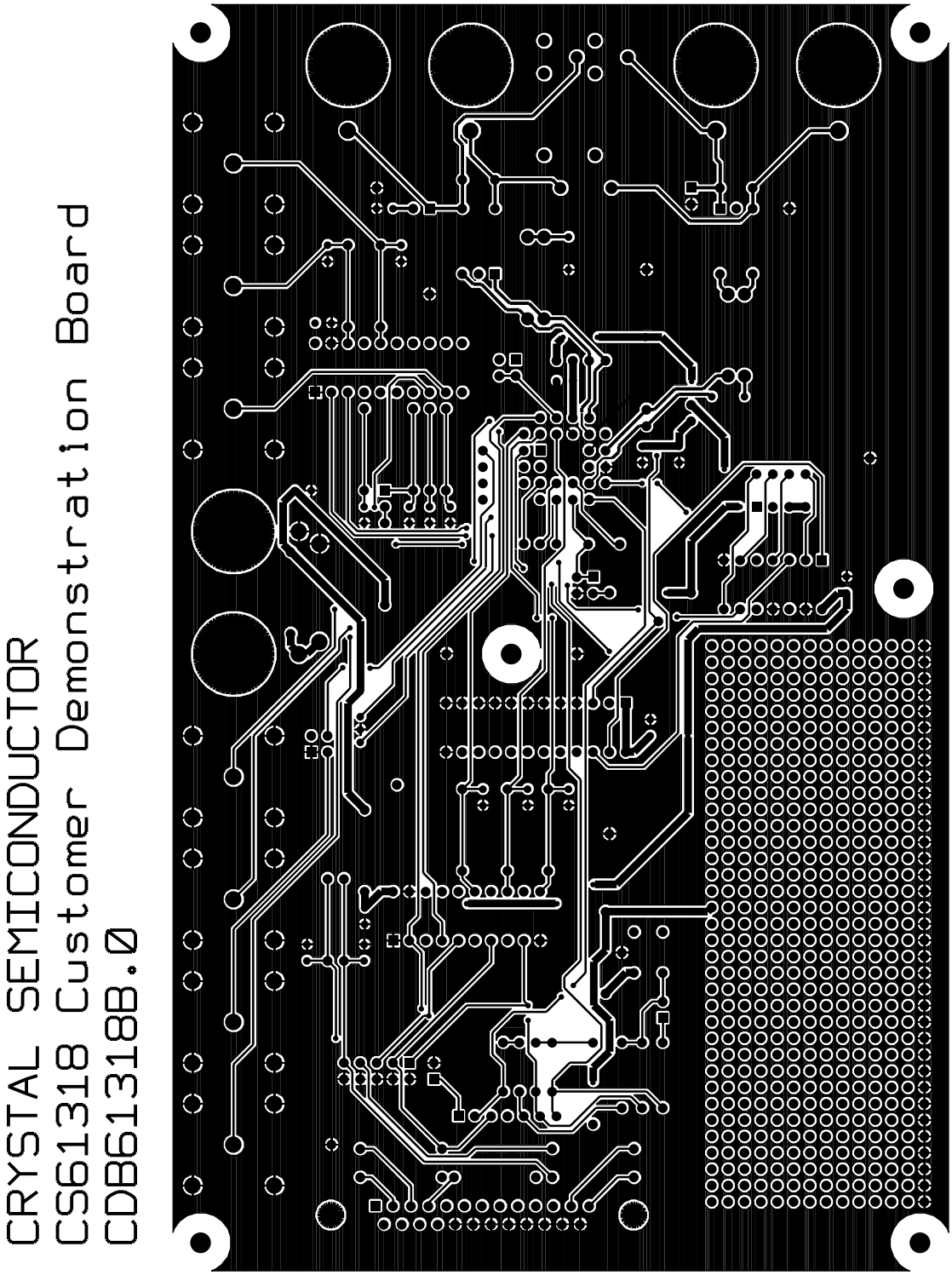
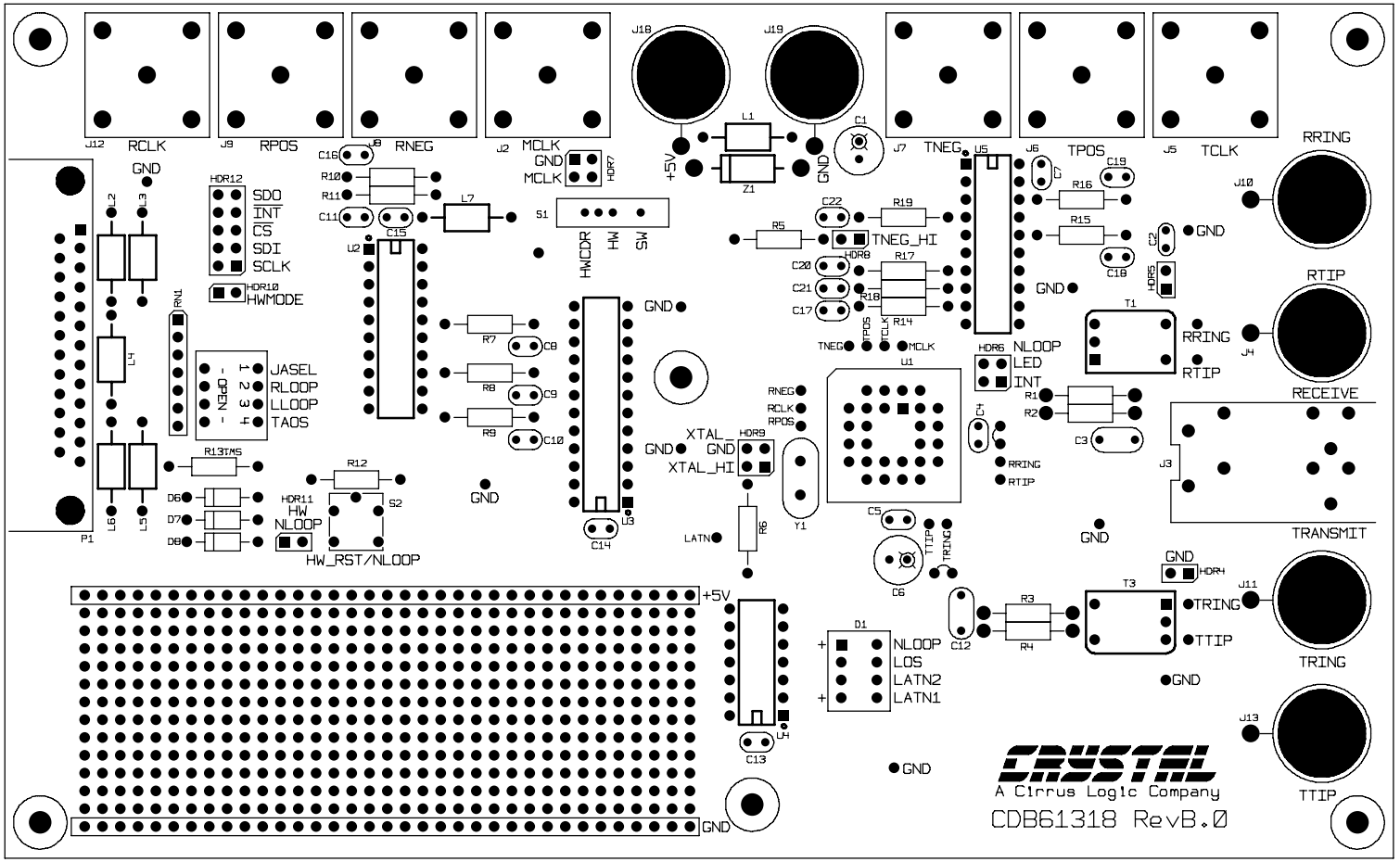


Figure 6 Board Layout - Bottom Layer

CRYSTAL SEMICONDUCTOR
CS61318 Customer Demonstration Board
CDB61318B.Ø



SILKSCREEN – TOP

Figure 7. Evaluation Board Silkscreen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