ADS-230/ADS-231

Low-Power, 12-Bit, 1.0/1.5MHz Sampling A/D Converter

FEATURES

- **12-bit resolution**
- **1.0 and 1.5MHz throughput rates**
- **Small 44-pin Leaded Chip Carrier**
- **Single +5V supply**
- **Low power, 75 and 200mW maximum**
- **Low power "standby" mode**
- **Outstanding dynamic performance**
- **No missing codes over temperature**
- **Built-in sample-and-hold**
- **Optional two-channel input multiplexer**
- **Ideal for both time and frequency-domain applications**

GENERAL DESCRIPTION

The ADS-230 and ADS-231 are 12-bit, high speed CMOS sampling analog-to-digital converters capable of minimum sampling rates of 1.0 and 1.5MHz, respectively. Both models feature excellent dynamic performance including a typical SNR of 72dB for the ADS-230 and 70dB for the ADS-231.

The ADS-230 and ADS-231 are packaged in a small 44-pin plastic Leaded Chip Carrier (LCC). Each model contains a fast-settling sample/hold amplifier, a multipass (three-step flash) A/D converter, timing and control logic, three-state outputs, a two-channel multiplexer, and digital error correction circuitry. Digital input and output levels are TTL.

Requiring only a single +5V supply, the ADS-230 typically dissipates only 60mW and the ADS-231 only 170mW. Both models offer a low-power "standby" mode resulting in typical power dissipations of 100µW and 250µW, respectively. The units offer a maximum unipolar input range of 0 to +5V. The exact value of the input range is determined by an externally applied reference voltage. Both models operate over the extended –40 to +85°C temperature range.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	AGND	44	AV_S
2	V_{BS}	43	BIT 1 (MSB)
3	V_B	42	BIT 2
4	$V_{R/16}$	41	BIT 3
5	V_T	40	BIT 4
6	V_{TS}	39	BIT 5
7	$CH1_{IN}$	38	BIT 6
8	NC	37	BIT 7
9	$CH2_{IN}$	36	BIT 8
10	NC	35	BIT 9
11	MUX OUT	34	NC
12	ANALOG INPUT	33	BIT 10
13	AGND	32	BIT 11
14	AV_S	31	BIT 12 (LSB)
15	DGND C	30	$\overline{EOC}$
16	SEL	29	$\overline{INT}$
17	$\overline{PD}$	28	NC
18	DGND C	27	DGND D
19	MD	26	DGND C
20	$\overline{OE}$	25	DV_S
21	$\overline{RD}$	24	TEST
22	$S/\overline{H}$	23	$\overline{CS}$

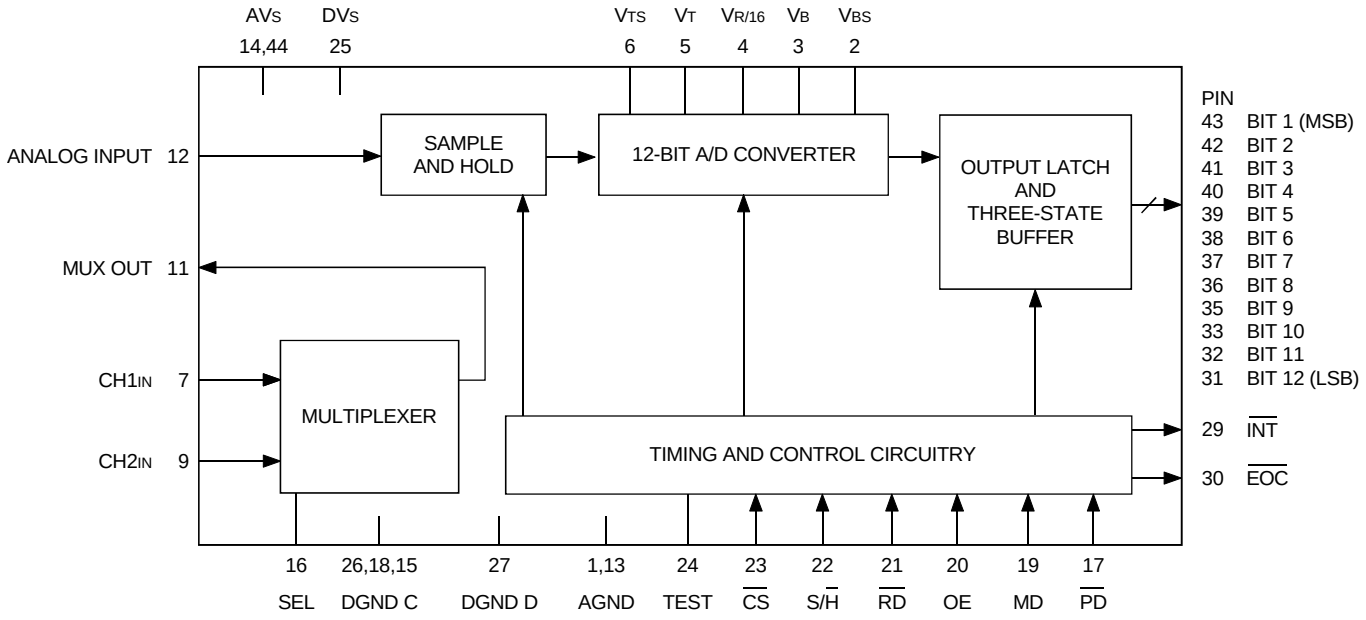

Figure 1. ADS-220/-231 Simplified Block Diagram

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ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
Supply Voltages		
(VS = AVS = DVS)	–0.3 to +6	V
Input or Output Voltage, any pin	–0.3 to VS +0.3	V
Input Current, any pin ①	25	mA
Total Package Input Current, ①	50	mA
Power Dissipation, ②	875	mW
ESD Susceptibilty, ③	2000	V
Soldering, Infrared, 15 seconds	+300	°C

PHYSICAL/ENVIRONMENTAL

PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range TA = TJ	–40	—	+85	°C
Thermal Impedance, θja	—	55	—	°C/Watt
Maximum Junction Temp. TJMAX	—	—	+150	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	44-pin Plastic Leaded Chip Carrier			

FUNCTIONAL SPECIFICATIONS

(The following specifications apply for TA = TJ = 25°C, DVS = AVS = 5.0V, VTS = +4.096V, VBS = AGND, RS = 25ohms and FS = 1.0/1.5MHz for the ADS-230/231 respectively, unless otherwise specified.)

	ADS-230			ADS-231			
	+25°C	–40 to +85°C		+25°C	–40 to +85°C		
ANALOG INPUT	**TYP.**	**MIN.**	**MAX.**	**TYP.**	**MIN.**	**MAX.**	**UNITS**
Input Voltage Range (Pins 7, 9, 12)	—	–0.05	AVS+0.05	—	–0.05	AVS+0.05	V
Input Leakage Current	0.1	—	3	0.1	—	3	µA
Input Capacitance	25	—	—	25	—	—	pF
MUX On/Off-Channel Leakage	0.1	—	3	0.1	—	3	µA
MUX Input Capacitance	7	—	—	7	—	—	pF
MUX Off-Channel Isolation							
FIN = 100kHz, –0dB	92	—	—	92	—	—	dB
REFERENCE INPUT							
Reference Input + (Pin 6), VTS	—	—	AVS	—	—	AVS	V
Reference Input – (Pin 2), VBS	—	0	—	—	0	—	V
Reference Resistance	750	500	1000	750	500	1000	Ohms
DIGITAL INPUT							
Logic Levels							
Logic "1", VS = 5.5V	—	2	—	—	2	—	V
Logic "0", VS = 4.5V	—	—	0.8	—	—	0.8	V
Logic Loading "1"	0.1	—	1	0.1	—	1	µA
Logic Loading "0"	0.1	—	1	0.1	—	1	µA
Digital Input Capacitance	4	—	—	4	—	—	pF
S/H̄ Pulse Width ④, ts/H̄	—	5	550	—	5	400	ns
STATIC PERFORMANCE							
Resolution	12			12			Bits
Integral Nonlinearity	±0.4	—	±1.5	±0.4	—	±1.5	LSB
Differential Nonlinearity Error	±0.4	—	±0.95	±0.4	—	±0.95	LSB
No Missing Codes	—	12	—	—	12	—	Bits
Offset Error	±0.3	—	±2.0	±0.3	—	±2.0	LSB
Gain Error	±0.2	—	±1.5	±0.3	—	±1.5	LSB
Power Supply Sensitivity, (±10%)	—	—	±1.0	—	—	±0.75	LSB
DYNAMIC PERFORMANCE ⑤							
Total Harmonic Distortion (–0dB)							
FIN = 100kHz ⑥	–82	—	–70	–80	—	–70	dB
Signal-to-Noise Ratio							
(wo/distortion, –0dB) FIN = 100kHz	72	69.5	—	70	67.5	—	dB
Signal-to-Noise Ratio ⑦							
(& distortion, –0dB) FIN = 100kHz	71	68	—	70	67	—	dB
Two-Tone Intermodulation Distortion							
FIN = 102.3, 102.7kHz, (–0dB)	–80	—	—	–80	—	—	dB
Aperature Delay Time, (tAD)	20	—	—	20	—	—	ns
A/D Conversion Rate	—	1	—	—	1.5	—	MHz

	ADS-230			ADS-231			
	+25°C	–40 to +85°C		+25°C	–40 to +85°C		
TIMING	**TYP.**	**MIN.**	**MAX.**	**TYP.**	**MIN.**	**MAX.**	**UNITS**
Conversion Time, t_{CONV}	740	600	980	580	510	660	ns
Time for Conversion to Start, t_{EOC}	95	60	125	90	60	125	ns
Access Time, t_{ACC} (C_L = 100pF)	10	—	20	10	—	20	ns
Three-State Control Time, t1H, t0H							
R_L = 1k, C_L = 10pF	25	—	40	25	—	40	ns
Delay Time, $\overline{RD}$ Low to $\overline{INT}$ High							
t_{INTH}, C_L = 100pF	35	—	60	35	—	60	ns
Delay Time, $\overline{EOC}$ High to $\overline{INT}$ Low							
t_{INTL}, C_L = 100pF	25	35	10	25	35	10	ns
$\overline{EOC}$ High to Data Valid, t_{UPDATE}	5	—	15	5	—	15	ns
MUX Address Setup Time, t_{MS}	—	50	—	—	50	—	ns
MUX Address Hold Time, t_{MH}	—	50	—	—	50	—	ns
$\overline{CS}$ Setup Time, t_{CSS}	—	20	—	—	20	—	ns
$\overline{CS}$ Hold Time, t_{CSH}	—	20	—	—	20	—	ns
Wake-up Time, t_{WU}							
$\overline{PD}$ High to First S/$\overline{H}$ Low	1	—	—	1	—	—	µs
DIGITAL OUTPUT							
Logic Levels							
Logic "1" (V_S = 4.5V)	—	2.4	—	—	2.4	—	V
Logic "0", (V_S = 4.5V)	—	—	0.4	—	—	0.4	V
Logic Loading "1"	—	—	–360	—	—	–360	µA
Logic Loading "0"	—	—	1.6	—	—	1.6	mA
Three-State Output Leakage	0.1	—	3	0.1	—	3	µA
Three-State Output Capacitance	5	—	—	5	—	—	pF
Output Coding	Binary			Binary			
POWER REQUIREMENTS							
Power Supply Range							
+5V Supply, V_S = AV_S = DV_S	—	4.5	5.5	—	4.75	5.25	V
Power Supply Current							
DV_S Supply Current, DI_S	2	—	3	2	—	3	mA
AV_S Supply Current, AI_S	10	—	12	32	—	37	mA
Standby Current (AI_S +DI_S, $\overline{PD}$ = 0) ⑧	20	—	—	50	—	—	µA
Power Dissipation	—	—	75	—	—	200	mW

Footnotes:

① When the input voltage at any pin exceeds the power supply rails (below GND or Above V_S) the input current must be limited to ±25mA or less. The package input current limits to two the number of pins that can meet this constant.

② In most cases, the maximum derated power dissipation will be reached only during fault conditions.

③ This is the ESD rating for the human body model, with a 100pF capacitor discharged through a 1.5 kilohm resistor. The ESD rating for the machine model is 200V.

④ For best performance, the rising edge of the S/$\overline{H}$ pulse must not be near either the falling or rising edge of $\overline{EOC}$. The recommended values of $t_{S/\overline{H}}$ are:
ADS-230: 5ns<$t_{S/\overline{H}}$<40ns, or 150ns<$t_{S/\overline{H}}$<550ns
ADS-231: 5ns<$t_{S/\overline{H}}$<40ns, or 150ns<$t_{S/\overline{H}}$<400ns

⑤ The MUX inputs $CH1_{IN}$ and $CH2_{IN}$ are not used during dynamic testing of these models. The internal multiplexer adds harmonic distortion at high input frequencies. See the Typical Performance Curves for THD with and without the MUX.

⑥ The contributions from the first nine harmonics are used in the calculation of THD.

⑦ Effective bits is equal to:

$$\frac{(SNR + Distortion - 1.76 + [20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}}])}{6.02}$$

⑧ Some units may have higher standby currents than the typical indicated. Production testing of standby current is prohibitive due to the 10 second delay time on DI_S after $\overline{PD}$ is pulled low.

PIN DESCRIPTIONS

AV_S, DV_S	These are the analog and digital power supply input pins. They should all be connected to the same voltage source. Both AV_S pins should be bypassed to AGND and the DV_S pin to DGNDD. Bypass using a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor.
AGND, DGNDC, DGNDD	These are the analog and digital ground pins. All of the ground pins should be returned to the same potential and connected to a stable, noise-free system ground. AGND is the analog ground. DGNDC is the ground for the digital control lines. DGNDD is the digital ground for the output data bus.
BIT 1 – BIT 12	These are the three-state data output pins. Output is enabled by $\overline{RD}$, $\overline{CS}$, and OE.
$CH1_{IN}$, $CH2_{IN}$	These are the analog input pins to the internal input multiplexer.
MUX OUT	This is the output of the internal multiplexer,
ANALOG INPUT	This is the direct input to the sampling A to D converter.
SEL	This is the multiplexer channel select pin. The input is selected based on the state of SEL when $\overline{EOC}$ transitions low. A low selects channel one and a high selects channel two. See Table 1.
MD	Connect to DGNDC
TEST	Connect to DV_S.
$\overline{CS}$	This is the Chip Select control input. When low, this pin enables the $\overline{RD}$, S/$\overline{H}$ and OE inputs. This pin can be tied low.
$\overline{INT}$	This is the Interrupt output pin. When using the Interrupt Interface Mode, this output goes low when a conversion is completed and indicates that the data is available in the output latches. This output is always high when $\overline{RD}$ is held low. Refer to the Timing Diagrams.
$\overline{EOC}$	This is the End of Conversion output pin. $\overline{EOC}$ is low during a conversion.
$\overline{RD}$	This is the Read control input pin. When $\overline{RD}$ and $\overline{CS}$ are low, the $\overline{INT}$ output is reset and, if $\overline{EOC}$ is high, data appears on the data bus. This pin can be tied low.
OE	This is the Output Enable control input pin. The data output pins are in the high impedance state when OE is low. Data appears when OE is high and $\overline{CS}$ and $\overline{RD}$ are both low. This pin can be tied high.
S/$\overline{H}$	This is the Sample and Hold control input pin. When $\overline{CS}$ is low a new conversion is initiated by the falling edge of this input.
$\overline{PD}$	This is the Power Down control input pin. This pin is held high for normal operation. When the input is low, the A to D converter goes into power standby mode.
$V_{R/16}$	Bypass this pin to AGND using a 0.1µF ceramic capacitor.
VT, VB	These are the positive (top) and negative (bottom) voltage reference force input pins, respectively.
VTS, VBS	These are the positive (top) and negative (bottom) voltage reference sense pins, respectively.

TECHNICAL NOTES

The Analog Input

For maximum performance, the source impedance driving the input of the ADS-230/-231 should be as low as possible. A source impedance of less than 100 ohms is recommended. See the Typical Performance Curves.

If the signal source has high output impedance, the output should be buffered with an op-amp capable of driving a switched 25pF/100ohm load. Any ringing or instability of the op-amp during the sampling period can cause conversion errors.

Using a high-speed buffer also improves the THD performance when using the internal MUX. The MUX on-resistance is non-linear over the range of the input voltage; this causes the RC time constant of the equivalent circuit shown in Figure 2 to vary with input voltage. This results in harmonic distortion with increasing frequency. Inserting a buffer between the MUX OUT and ANALOG INPUT terminals will eliminate the loading on R_{MUX} and significantly reduce THD.

The analog input of the ADS-230/-231 can be modeled as shown in Figure 2. The S/$\overline{H}$ switch is closed during the sample period, and open during hold. The hold capacitor (C_H) has to be charged to the input voltage by the source within the sample period. The source impedance (R_S) will directly effect the charge time. If R_S is too large, the voltage across C_H will not settle to within ½ LSB's of the source voltage before conversion begins. This will result in conversion errors.

The combination of R_S, R_{MUX}, R_{SW} and C_H form a low-pass filter. Therefore, minimizing R_S will increase the frequency response of the converter.

The settling time to n bits is:

$$t_{SETTLE} = (R_S + R_{MUX} + R_{SW}) * C_H * n * \ln(2)$$

The bandwidth of the input circuit is:

$$F\ (-3dB) = 1/[2 * 3.14 * (R_S + R_{MUX} + R_{SW}) * C_H]$$

Internal Multiplexer

Both the ADS-230 and ADS-231 have an internal multiplexer that is controlled by the logic level on the SEL pin when $\overline{EOC}$ goes low. See the timing diagrams. The MUX setup and hold times can be determined from the following:

$t_{MS(wrt\ S/H)} = t_{MS} - t_{EOC\ (min)}$
$t_{MS(wrt\ S/H)} = 50 - 60$
$t_{MS(wrt\ S/H)} = -10ns$

$t_{MH(wrt\ S/H)} = t_{MH} + t_{EOC\ (max)}$
$t_{MH(wrt\ S/H)} = 50 + 125$
$t_{MH(wrt\ S/H)} = 175ns$

Note that the –10ns indicates that data on SEL must be valid within 10ns of the S/$\overline{H}$ pulse going low in order to meet the setup time requirements. SEL must be valid for the length of time determined by the following equation:

$$(t_{MS} + t_{EOC(max)}) - (t_{MS} - t_{EOC\ (min)}) = 185ns$$

Table 1 shows the coding for MUX channel selection.

The output of the MUX is available at the MUX OUT pin. This output allows the user to perform additional signal processing, such as buffering, filtering or gain, before the signal is brought to the ANALOG INPUT pin. If signal processing is not required connect the MUX OUT pin directly to the ANALOG INPUT pin.

Table 1. Internal Multiplexer Programming

SEL	Channel
0	CH1IN
1	CH2IN

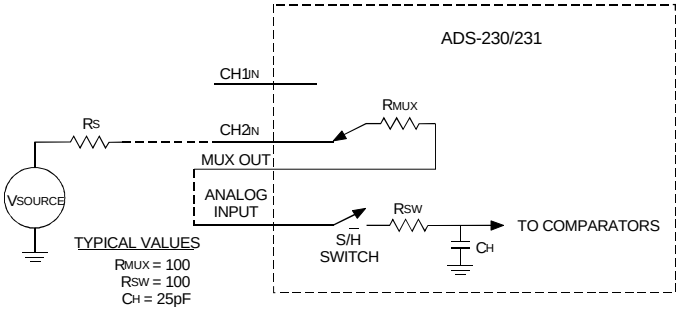


Figure 2. ADS-230/-231 Input Stage Model

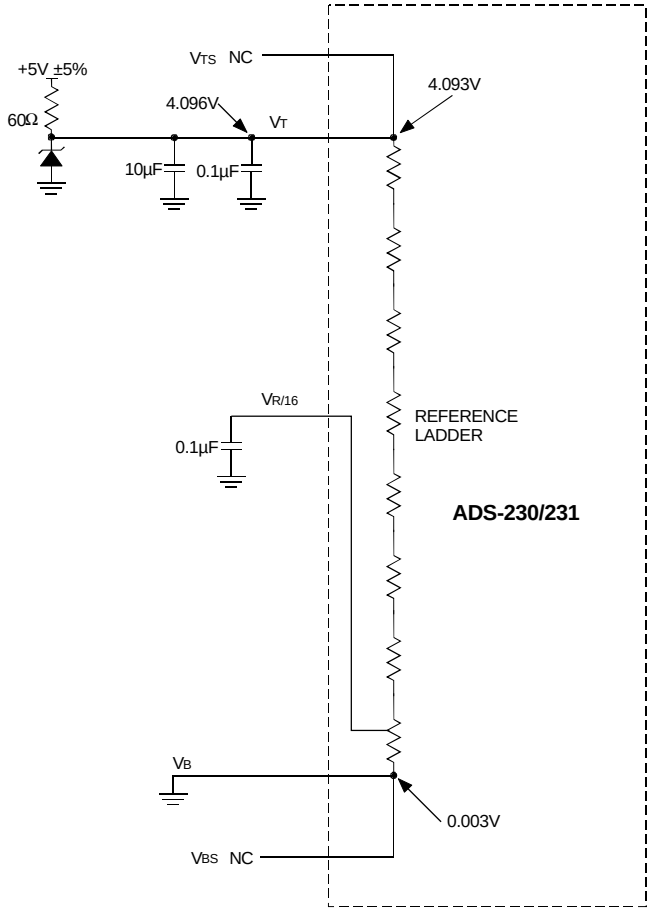


Figure 3. Reference Force Input Only

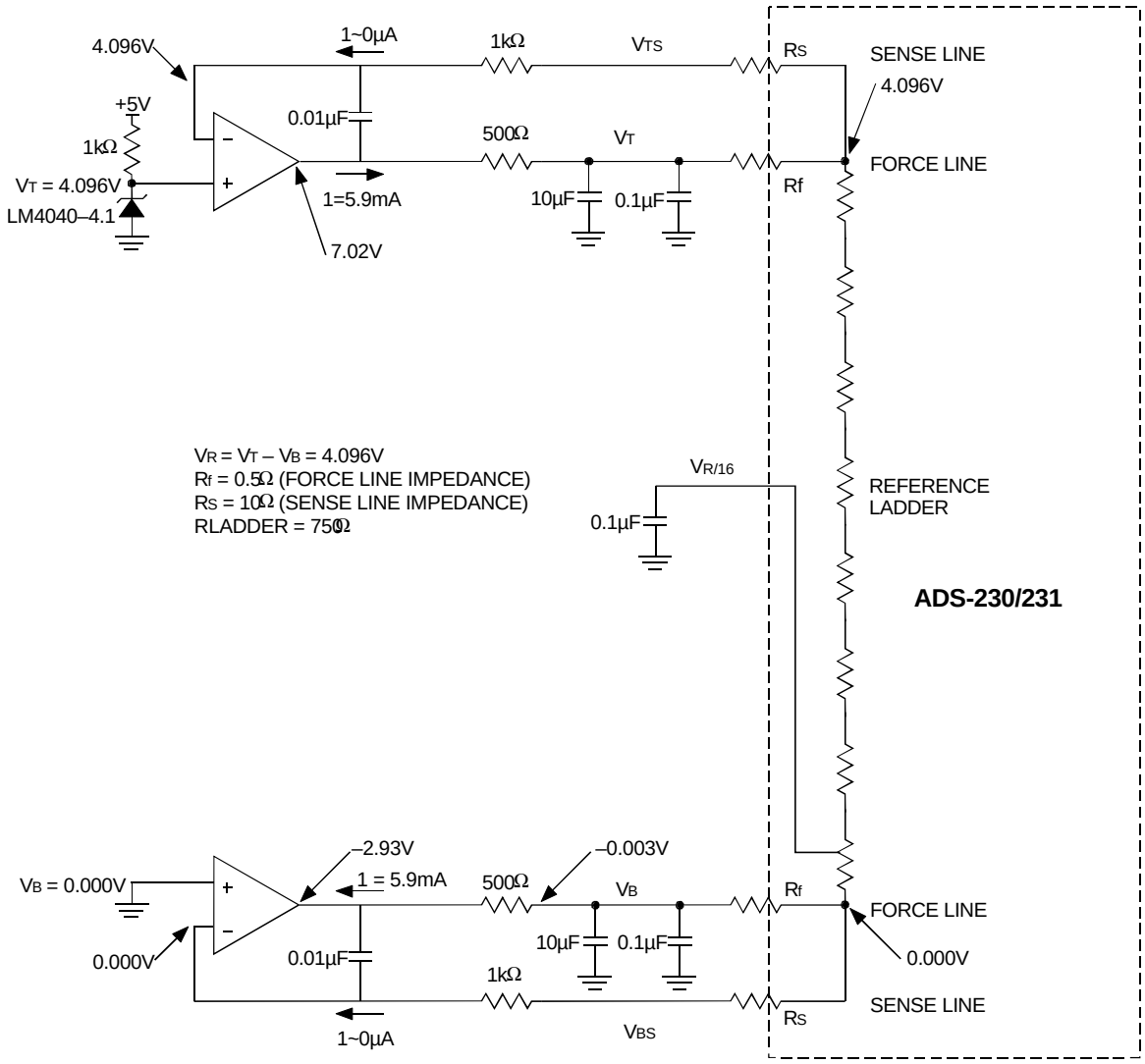


Figure 4. Ladder Reference Force and Sense Inputs

Reference Inputs

Reference voltages are applied to the fully differential V_T and V_B reference input pins. The resistance of the reference ladder network is typically 750 ohms. Additional parasitic resistances are added by the package leads, wire bonds, conductor traces, etc. These parasitic resistances can introduce voltage drops causing gain and offset errors as large as 6 LSB's at the 12-bit level. These IR drops can be compensated for by sensing the reference voltages at the V_{TS} and V_{BS} reference sense pins and forcing the reference voltage an exact value as shown in Figure 4.

Since there is essentially zero current flowing through the sense line there is negligible voltage drop to the inverting input of the op-amp. The voltage at the inverting input of the op-amp, therefore, accurately represents the voltage at the top or bottom of the reference ladder network. The op-amp drives the force input and forces the voltages at the ends of the reference ladder network to equal the voltage at the op-amps non-inverting input, plus or minus the op-amps input offset voltage. When using this reference configuration with a low offset voltage op-amp, gain and offset errors below 0.5 LSB are readily obtainable.

The 0.1 and 10µF capacitors on the force inputs provide high frequency decoupling of the reference ladder network. The 500Ω force resistors isolate the op-amp from the large capacitive load. The 0.01µF and 1kΩ network ensures stability at high frequencies. The VR/16 output should be bypassed to analog ground with a 0.1µF ceramic capacitor. All bypass capacitors should be located as close to the pins as possible to minimize noise on the reference ladder.

If the ADS-230/-231 is used in a frequency domain application then the circuit shown in Figure 3 maybe used. This circuit will introduce several LSB's of gain and offset error, but the dynamic performance will be unaffected.

The reference inputs are fully differential and define the full-scale range of the input signal. The maximum range can be up to 5 volts, or when required any span within the 0 to 5V limit may be used. When using lower voltage spans the noise performance will degrade. See the Typical Performance Curves.

Timing

The ADS-230/-231 has two modes of operation as shown in Figure 5, 6, 7 and 8.

In the Interrupt Interface mode, as shown in Figure 5, the falling edge of S/$\overline{H}$ holds the input voltage and initiates a conversion when $\overline{CS}$ is held low. At the end of conversion, the $\overline{EOC}$ output goes high and the $\overline{INT}$ output goes low, indicating that the conversion results are latched and may be read by pulling $\overline{RD}$ low. The falling edge of $\overline{RD}$ resets the $\overline{INT}$ line.

The High Speed Interface mode is shown in Figure 6. In this mode the output data is always present, and the $\overline{INT}$ to $\overline{RD}$ delay is eliminated.

The control logic decoding section is shown in Figure 8.

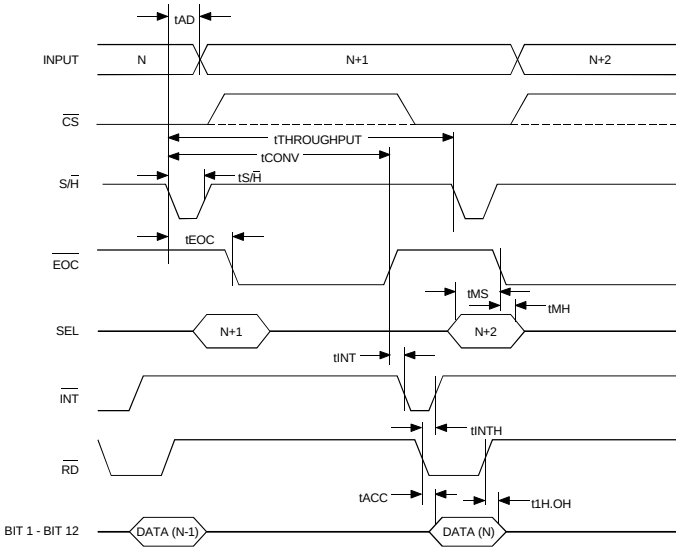


Figure 5. Interrupt Interface Timing (MD = 0, OE = 1)

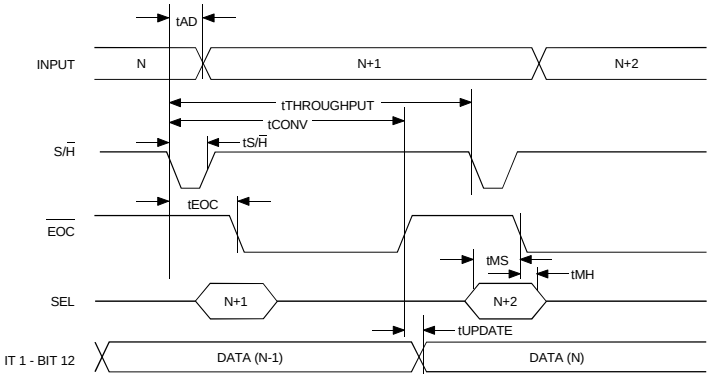


Figure 6. High-speed Interface Timing (MD = 0, OE = 1, $\overline{CS}$ = 0, $\overline{RD}$ = 0)

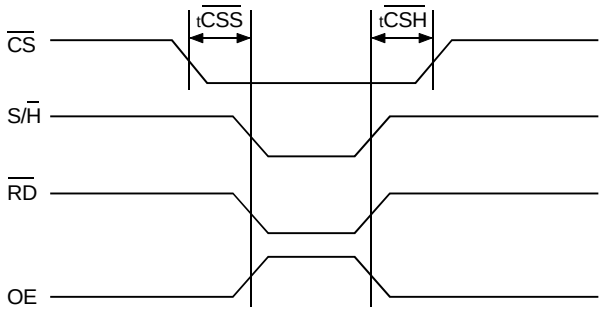


Figure 7. $\overline{CS}$ Setup & Hold Timing for S/$\overline{H}$, $\overline{RD}$ and OE

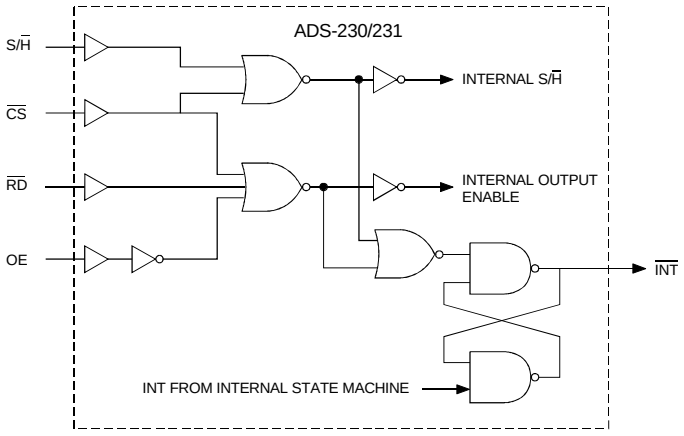


Figure 8. ADS Control Logic

Power Supply

The ADS-230 and ADS-231 are designed to operate off a single +5V supply. To guarantee proper operation of the converters, only one power supply should be used. If separate analog and digital supplies are used, then the converter must be powered up with the analog supply. The absolute maximum ratings states that all inputs must be between GND –300mV and VS +300mV. When the converter power supply is turned off the maximum input becomes ±300mV, which in turn requires that the devices connected to the converter have power removed before power to the converter is removed.

There are two analog pins AVS and one digital supply pin DVS. This allows for separate bypassing of the analog and digital sections of the circuit. Both AVS pins should be bypassed to ground with 0.1µF ceramic capacitors. At least one of the AVS pins should be bypassed with a 10µF tantalum capacitor. The DVS input should be bypassed with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor. All bypass capacitor should be located as close to the converter as possible.

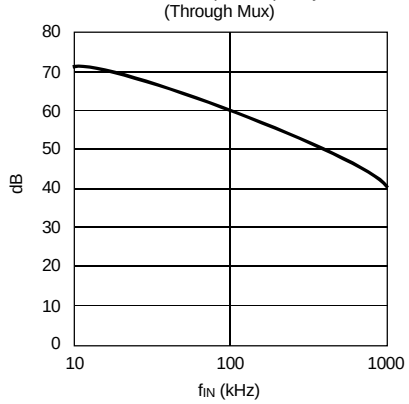
There are two analog ground pins (AGND), three digital ground pins for the control inputs (DGNDC), and one digital ground pin for the data output lines (DGNDD). Separating the analog section from the digital sections reduces digital interference in the analog circuitry thereby improving the dynamic performance of the converter. When driving a high capacitance digital data bus buffering the output data lines maybe necessary to minimize the DVS and DGND current spikes generated each conversion to charge the data bus capacitance.

These large current spikes will couple back to the analog circuitry increasing the converter noise level. Separating the digital outputs from the digital inputs reduces the possibility of ground bounce from the data lines causing jitter on the S/H input. The digital ground planes should be tied together at the digital ground pins. The analog ground plane should be tied to the DGNDD ground plane at the ground return strap for the power supply.

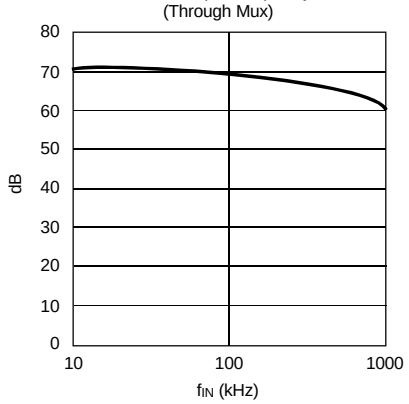
S/H Input

The clock source driving the S/H input must be free of jitter. For best performance, a crystal oscillator is recommended. For the ADS-230 and ADS-231, a 1.0 and 1.5Mhz square wave will provide a good signal for the respective S/$\overline{H}$ inputs. In both cases, as long as the duty cycle is near 50%, the S/$\overline{H}$ pulse widths fall under the maximum allowed. When operating the ADS-230 below 910kHz or the ADS-231 below 1.25MHz, the S/$\overline{H}$ pulse widths must be less than half the respective sample periods.

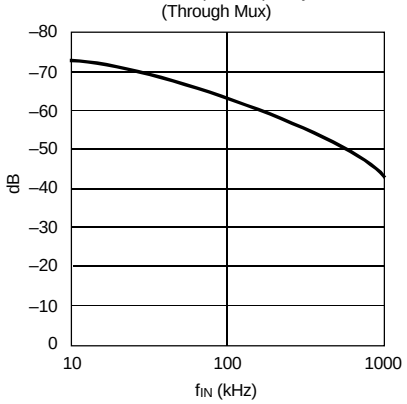
SINAD vs. Input Frequency
(Through Mux)



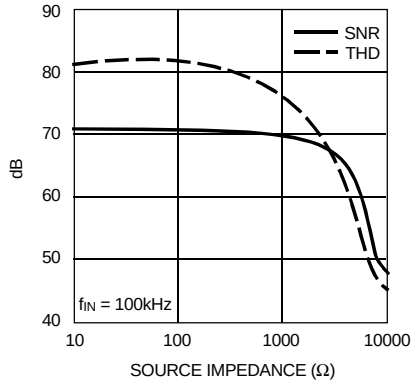
SNR vs. Input Frequency
(Through Mux)



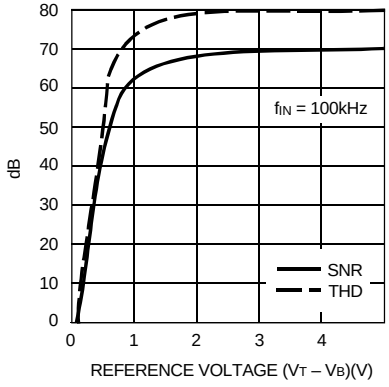
THD vs. Input Frequency
(Through Mux)



SNR and THD
vs. Source Impedance



SNR and THD
vs. Reference Voltage



Note: Unless otherwise stated, the following conditions apply:

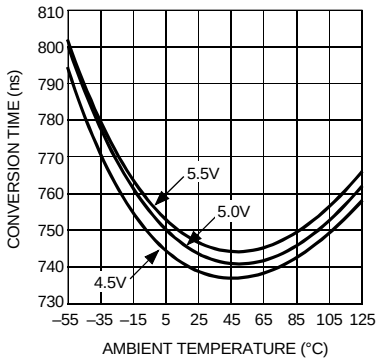
$DV_S = AV_S = 5.0V$

$T_A = 25°C$

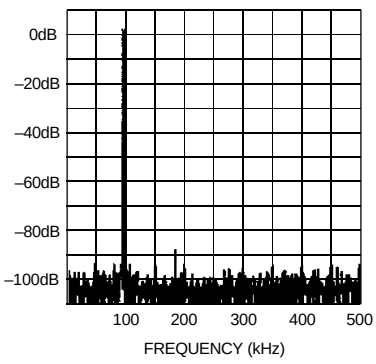
$f_S = 1.0MHz$

f_{IN} = 0dB from full scale

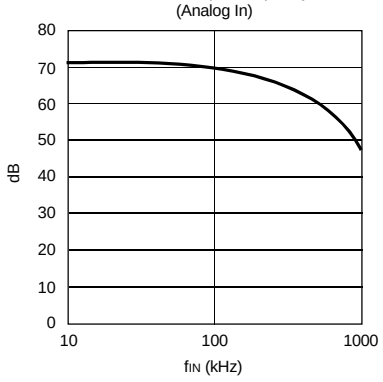
Conversion Time
vs. Temperature



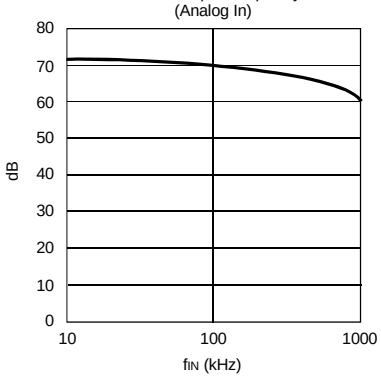
FFT



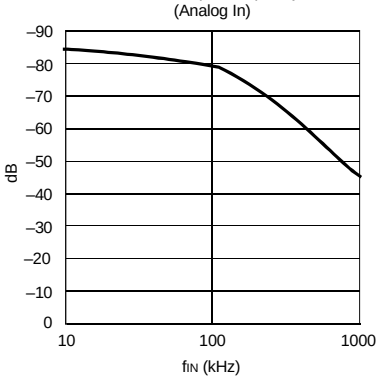
SINAD vs. Input Frequency
(Analog In)



SNR vs. Input Frequency
(Analog In)

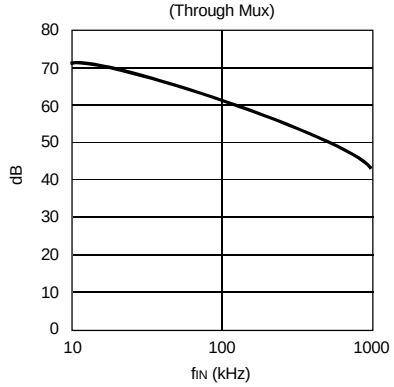


THD vs. Input Frequency
(Analog In)

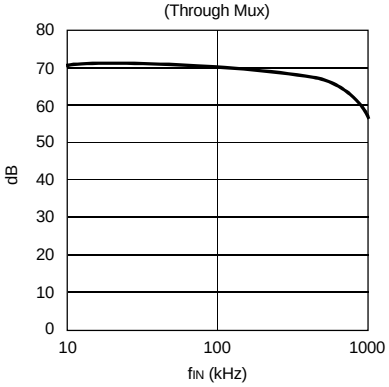


Typical Performance Curves for ADS-230

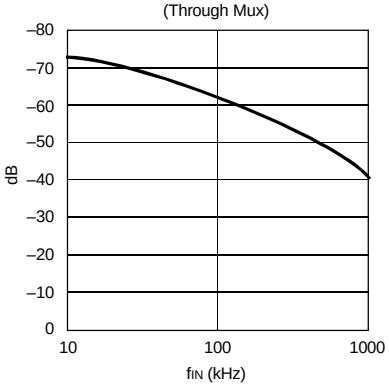
SINAD vs. Input Frequency
(Through Mux)



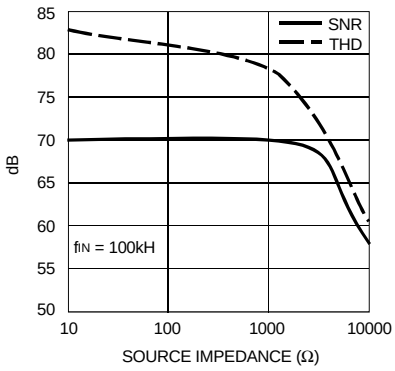
SNR vs. Input Frequency
(Through Mux)



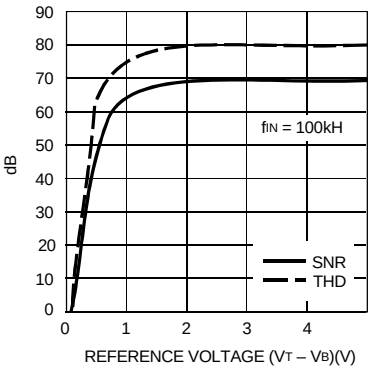
THD vs. Input Frequency
(Through Mux)



SNR and THD
vs. Source Impedance



SNR and THD
vs. Reference Voltage



Note: Unless otherwise stated, the following conditions apply:

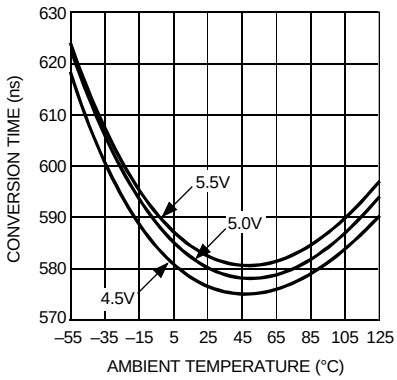
$DV_S = AV_S = 5.0V$

$T_A = 25°C$

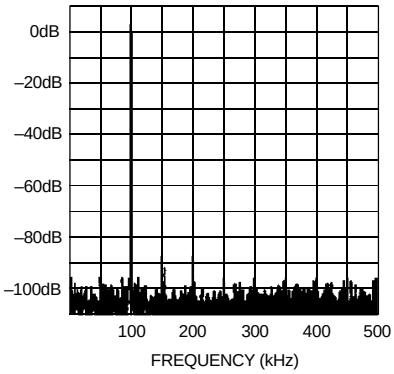
$f_S = 1.5MHz$

f_{IN} = 0dB from full scale

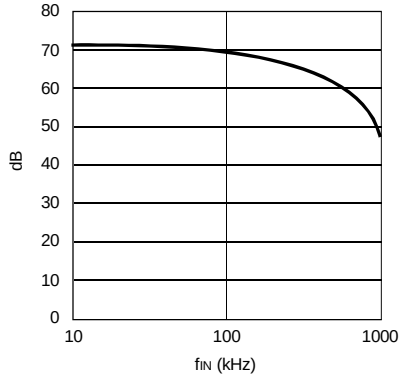
Conversion Time
vs. Temperature



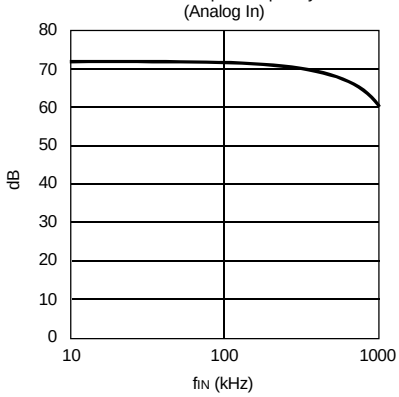
FFT



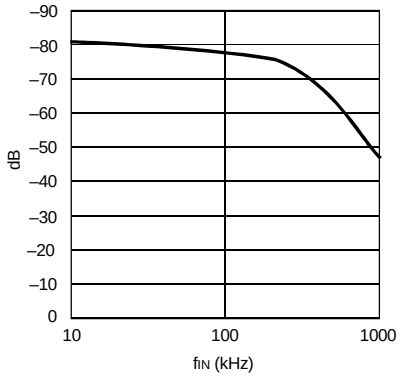
SINAD vs. Input Frequency
(Analog In)



SNR vs. Input Frequency
(Analog In)

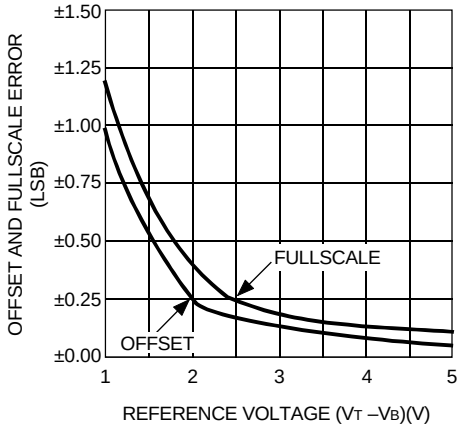


THD vs. Input Frequency
(Analog In)

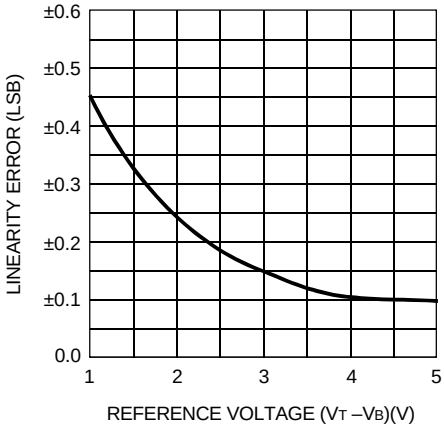


Typical Performance Curves for ADS-231

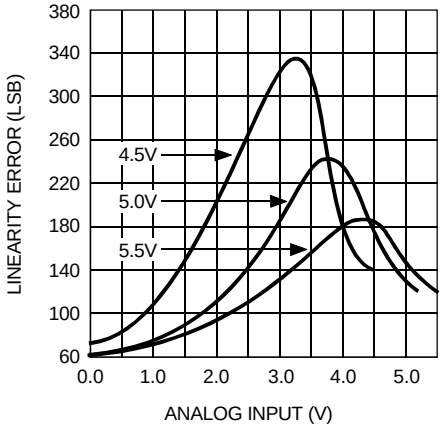
Offset and Fullscale Error
vs. Reference Voltage



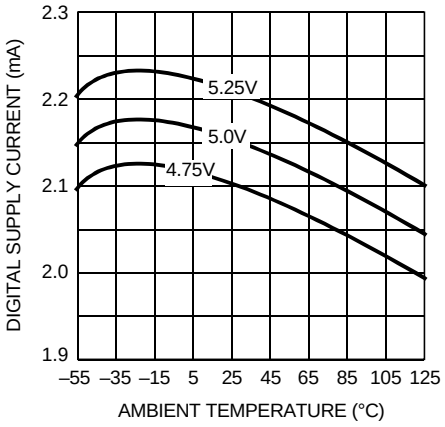
Linearity Error
vs. Reference Voltage



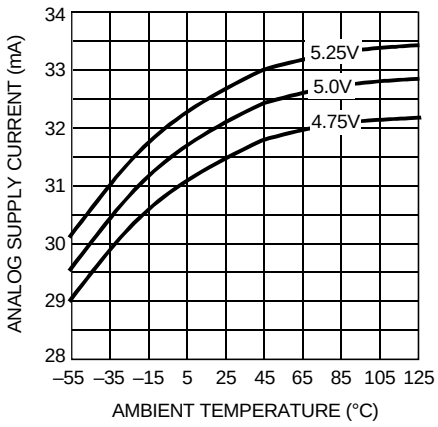
Mux ON Resistance
vs. Analog Input vs. VS



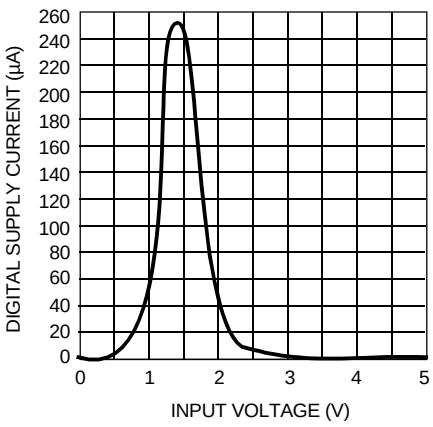
Digital Supply Current
vs. Temperature vs. DVS



Analog Supply Current
vs. Temperature vs. AVS



Current Consumption in Standby Mode
vs. Voltage on Digital Input Pins

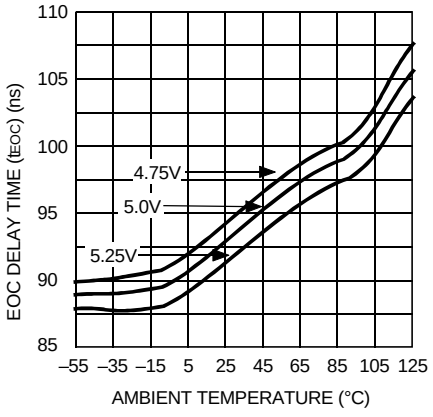


Note: Unless otherwise stated, the following conditions apply:

$DV_S = AV_S = 5.0V$

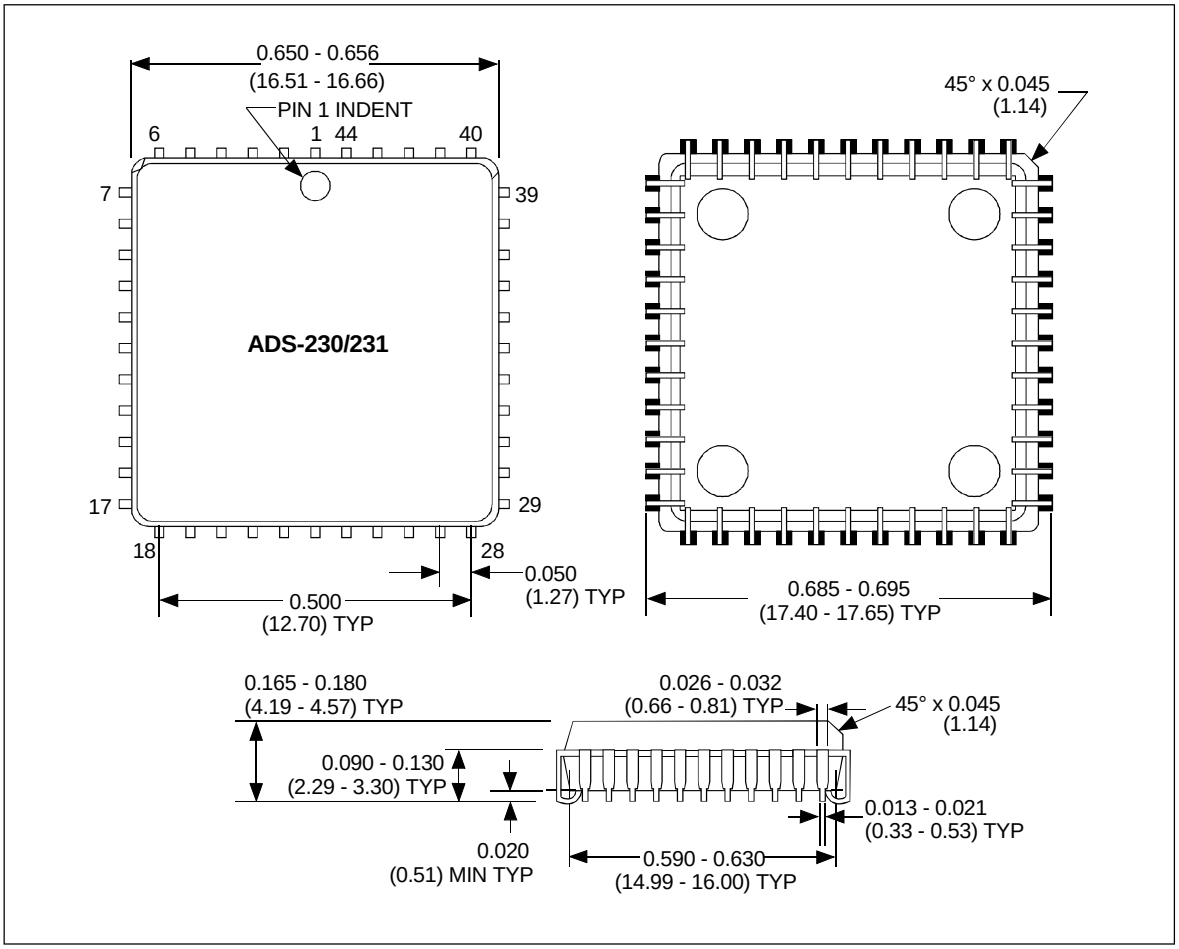
$T_A = 25°C$

EOC Delay Time (t_{EOC})
vs. Temperature vs. VS



Typical Performance Curves, ADS-230/-231

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

Model	Throughput Rate	Operating Temperature Range
ADS-230	1.0MHz	–40°C to +85°C
ADS-231	1.5MHz	–40°C to +85°C

INNOVATION and EXCELLENCE

ISO 9001
REGISTERED

DS-0301 03/97

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