19-4577; Rev 0; 4/09

EVALUATION KIT AVAILABLE

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

General Description

The MAX17030/MAX17036 are 3/2-phase interleaved Quick-PWM™ step-down VID power-supply controllers for IMVP-6.5 notebook CPUs. Two integrated drivers and the option to drive a third phase using an external driver such as the MAX8791 allow for a flexible 3/2-phase configuration depending on the CPU being supported.

True out-of-phase operation reduces input ripple-current requirements and output-voltage ripple while easing component selection and layout difficulties. The Quick-PWM control provides instantaneous response to fast load-current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX17030/MAX17036 are intended for bucking down the battery directly to create the core voltage. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency.

A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection. An output current monitor provides an analog current output proportional to the sum of the inductor currents, which in steady state is the same as the current consumed by the CPU.

Applications

IMVP-6.5 SV and XE Core Power Supplies

High-Current Voltage-Positioned Step-Down Converters

3 to 4 Li+ Cells Battery to CPU Core Supply Converters

Notebooks/Desktops/Servers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17030GTL+	-40°C to +105°C	40 TQFN-EP*
MAX17036GTL+	-40°C to +105°C	40 TQFN-EP*

+Denotes a lead-free(Pb)/RoHS-compliant package.

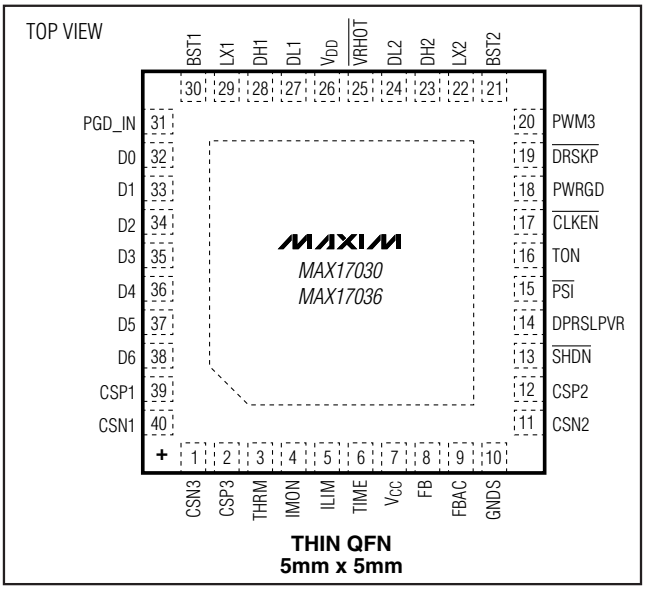
**EP = Exposed pad.*

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- **Triple/Dual-Phase Quick-PWM Controllers**
- **2 Internal Drivers + 1 External Driver**
- **±0.5% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **7-Bit IMVP-6.5 DAC**
- **Dynamic Phase Selection Optimizes Active/Sleep Efficiency**
- **Transient Phase Overlap Reduces Output Capacitance**
- **Transient Suppression Feature (MAX17036 Only)**
- **Integrated Boost Switches**
- **Active Voltage Positioning with Adjustable Gain**
- **Accurate Lossless Current Balance and Current Limit**
- **Remote Output and Ground Sense**
- **Adjustable Output Slew-Rate Control**
- **Power-Good (IMVPOK), Clock Enable ($\overline{CLKEN}$), and Thermal-Fault (VRHOT) Outputs**
- **IMVP-6.5 Power Sequencing and Timing Compliant**
- **Output Current Monitor (IMON)**
- **Drives Large Synchronous Rectifier FETs**
- **7V to 26V Battery Input Range**
- **Adjustable Switching Frequency (600kHz max)**
- **Undervoltage, Overvoltage, and Thermal-Fault Protection**

Pin Configuration



THIN QFN
5mm x 5mm

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC}, V_{DD} to GND .....-0.3V to +6V
D0–D6, PGD_IN, $\overline{PSI}$, DPRSLPVR to GND .....-0.3V to +6V
CSP_, CSN_, THRM, ILIM to GND.....-0.3V to +6V
PWRGD, $\overline{CLKEN}$, $\overline{VR\_HOT}$ to GND.....-0.3V to +6V
FB, FBAC, IMON, TIME to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$ to GND (Note 2).....-0.3V to +30V
TON to GND .....-0.3V to +30V
GNDS to GND .....-0.3V to +0.3V
DL1, DL2, PWM3, $\overline{DRSKP}$ to GND .....-0.3V to (V_{DD} + 0.3V)
BST1, BST2 to GND .....-0.3V to +36V
BST1, BST2 to V_{DD}.....-0.3V to +30V
LX1 to BST1.....-6V to +0.3V
LX2 to BST2.....-6V to +0.3V
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
Continuous Power Dissipation (40-pin, 5mm x 5mm TQFN)
Up to +70°C 1778mW
Derating above +70°C .....22.2mW/°C
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Absolute Maximum Ratings valid using 20MHz bandwidth limit.

Note 2: $\overline{SHDN}$ might be forced to 12V for the purpose of debugging prototype breadboards using the no-fault test mode. Internal BST switches are disabled as well. Use external BST diodes when $\overline{SHDN}$ is forced to 12V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V_{IN}		7		26	
FB Output Voltage Accuracy	V_{FB}	Measured at FB with respect to GNDS; includes load-regulation error (Note 3)	DAC codes from 0.8125V to 1.5000V	-0.5		+0.5	%
			DAC codes from 0.3750V to 0.8000V	-7		+7	mV
			DAC codes from 0 to 0.3625V	-20		+20	
Boot Voltage	V_{BOOT}			1.094	1.100	1.106	V
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
FB Input Bias Current		T_A = +25°C		-0.1		+0.1	µA
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	1.00	1.03	V/V
GNDS Input Bias Current	I_{GNDS}	T_A = +25°C		-0.5		+0.5	µA
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 147kΩ		1.985	2.000	2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 147kΩ (6.08mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)		-20		+20	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, measured at DH1, DH2, and PWM3 (Note 4)	R_{TON} = 96.75kΩ (600kHz per phase), 167ns nominal	-15		+15	%
			R_{TON} = 200kΩ (300kHz per phase), 333ns nominal	-10		+10	
			R_{TON} = 303.25kΩ (200kHz per phase), 500ns nominal	-15		+15	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH1, DH2, and PWM3 (Note 4)			300	375	ns
TON Shutdown Input Current	$I_{TON,SDN}$	$\overline{SHDN}$ = GND, V_{IN} = 26V, V_{CC} = V_{DD} = 0 or 5V, T_A = +25°C			0.01	0.1	µA
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point			3.5	7	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, $V_{DPRSLPVR}$ = 0, FB forced above the regulation point, T_A = +25°C			0.02	1	µA
Shutdown Supply Current (V_{CC})	$I_{CC,SDN}$	Measured at V_{CC}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (V_{DD})	$I_{DD,SDN}$	Measured at V_{DD}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to the voltage target set by the VID code (see Table 4)		250	300	350	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB		1.45	1.50	1.55	V
		Minimum OVP threshold; measured at FB			0.8		
Output Overvoltage-Propagation Delay	t_{OVP}	FB forced 25mV above trip threshold			10		µs
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code (see Table 4)		-450	-400	-350	mV
Output Undervoltage-Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold			10		µs
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 3)		20	60	100	µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3	6.5	10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code (see Table 4), 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
$\overline{CLKEN}$ and PWRGD Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs
$\overline{CLKEN}$ and PWRGD Transition Blanking Time (VID Transitions)	t_{BLANK}	Measured from the time when FB reaches the target voltage (Note 3)			20		µs
$\overline{CLKEN}$, PWRGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$, PWRGD Leakage Current		High-Z state, pin forced to 5V, T_A = +25°C				1	µA
CSN1 Pulldown Resistance in UVLO and Shutdown		$\overline{SHDN}$ = GND, measured after soft-shutdown completed (DL = low)			8		Ω
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.05	4.27	4.48	V
THERMAL PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}; falling edge, typical hysteresis = 75mV		29	30	31	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold, falling edge			10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state			2	8	Ω
$\overline{VRHOT}$ Leakage Current		High-Z state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C				1	µA
THRM Input Leakage	I_{THRM}	V_{THRM} = 0 to 5V, T_A = +25°C		-0.1		+0.1	µA
Thermal-Shutdown Threshold	T_{SHDN}	Typical hysteresis = 15°C			+160		°C
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7	10	13	mV
			V_{TIME} - V_{ILIM} = 500mV	45	50	55	
			ILIM = V_{CC}	20	22.5	25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZX}	V_{GND} - $V_{LX\_}$, $V_{DPRSLPVR}$ = 5V			0		mV
CSP_, CSN_ Common-Mode Input Range				0		2	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Phases 2, 3 Disable Threshold		Measured at CSP2, CSP3		3	V_{CC} - 1	V_{CC} - 0.4	V
CSP_, CSN_ Input Current	I_{CSP}, I_{CSN}	T_A = +25°C		-0.2		+0.2	µA
ILIM Input Current	I_{ILIM}	T_A = +25°C		-0.1		+0.1	µA
Droop Amplifier Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3	T_A = +25°C	-0.5		+0.5	mV/ phase
			T_A = 0°C to +85°C	-0.75		+0.75	
Droop Amplifier Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, V_{FBAC} = $V_{CSN\_}$ = 0.45V to 1.5V		393	400	406	µS
Current-Monitor Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{IMON} = 0, Σ indicates summation over all power-up enabled phases from 1 to N, N = 3		-1.1		+1	mV/ phase
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, $V_{CSN\_}$ = 0.45V to 1.5V		1.552	1.6	1.648	mS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$		High state (pullup)		0.7	2	Ω
			Low state (pulldown)		0.25	0.7	
DH_ Gate-Driver Source Current	$I_{DH(SOURCE)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DH_ Gate-Driver Sink Current	$I_{DH(SINK)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.7		A
DL_ Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V			8		A
DL_ Transition Time		DL_ falling, $C_{DL\_}$ = 3nF			20		ns
		DL rising, $C_{DL\_}$ = 3nF			20		
DH_ Transition Time		DH_ falling, $C_{DH\_}$ = 3nF			20		ns
		DH_ rising, $C_{DH\_}$ = 3nF			20		
Internal BST_ Switch On-Resistance	$R_{ON(BST)}$	$I_{BST\_}$ = 10mA			10	20	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM3, $\overline{DRSKP}$ OUTPUTS						
PWM3, $\overline{DRSKP}$ Output High Voltages		I_{SOURCE} = 3mA	V_{DD} - 0.4V			V
PWM3, $\overline{DRSKP}$ Output Low Voltages		I_{SINK} = 3mA			0.4	V
LOGIC AND I/O						
Logic-Input High Voltage	V_{IH}	$\overline{SHDN}$, PGD_IN	2.3			V
Logic-Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGD_IN			1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, DPRSLPVR	0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, DPRSLPVR			0.33	V
Logic Input Current		T_A = +25°C; $\overline{SHDN}$, DPRSLPVR, PGD_IN, $\overline{PSI}$, D0–D6 = 0 or 5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = -40ºC to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V_{IN}		7		26	
FB Output-Voltage Accuracy	V_{FB}	Measured at FB with respect to GNDS, includes load-regulation error (Note 3)	DAC codes from 0.8125V to 1.5000V	-0.75		+0.75	%
			DAC codes from 0.3750V to 0.8000V	-10		+10	mV
			DAC codes from 0 to 0.3625V	-25		+25	
Boot Voltage	V_{BOOT}			1.085		1.115	V
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.95		1.05	V/V
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 147kΩ		1.985		2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 147kΩ (6.08mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)		-20		+20	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, measured at DH1, DH2, and PWM3 (Note 4)	R_{TON} = 96.75kΩ (600kHz per phase), 167ns nominal	-15		+15	%
			R_{TON} = 200kΩ (300kHz per phase), 333ns nominal	-10		+10	
			R_{TON} = 303.25kΩ (200kHz per phase), 500ns nominal	-15		+15	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH1, DH2, and PWM3 (Note 4)				400	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, DPRSLPVR = 5V, FB forced above the regulation point				7	mA
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to the voltage target set by the VID code (see Table 4)		250		350	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB		1.45		1.55	V
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code (see Table 4)		-450		-350	mV
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 3)		20		100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3		10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code (see Table 4), 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	
$\overline{CLKEN}$, PWRGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.05		4.5	V
THERMAL PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}, falling edge, typical hysteresis = 75mV		29		31	%
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state				8	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7		13	mV
			V_{TIME} - V_{ILIM} = 500mV	45		55	
			ILIM = V_{CC}	20		25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
CSP_, CSN_ Common-Mode Input Range				0		2	V
Phases 2, 3 Disable Threshold		Measured at CSP2, CSP3		3		V_{CC} - 0.4	V
Droop Amplifier Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3		-1		+1	mV/ phase
Droop Amplifier Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, V_{FBAC} = $V_{CSN\_}$ = 0.45V to 1.5V		390		407	µS
Current-Monitor Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3		-1.5		+1.5	mV/ phase
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, $V_{CSN\_}$ = 0.45V to 1.5V		1.536		1.664	mS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ – LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				2	Ω
		Low state (pulldown)				0.7	
Internal BST_ Switch On-Resistance	$R_{ON(BST)}$	I_{BST-} = 10mA				20	Ω
PWM3, $\overline{DRSKP}$ OUTPUTS							
PWM3, $\overline{DRSKP}$ Output High Voltages		I_{SOURCE} = 3mA		V_{DD} - 0.4V			V
PWM3, $\overline{DRSKP}$ Output Low Voltages		I_{SINK} = 3mA				0.4	V
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	$\overline{SHDN}$, PGD_IN		2.3			V
Logic-Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGD_IN				1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, DPRSLPVR		0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, DPRSLPVR				0.33	V

ELECTRICAL CHARACTERISTICS (continued)

Note 3: The equation for the target voltage V_{TARGET} is:
V_{TARGET} = The slew-rate-controlled version of V_{DAC}, where V_{DAC} = 0 for shutdown
V_{DAC} = V_{BOOT} during IMVP-6.5 startup
V_{DAC} = V_{VID} otherwise (the V_{VID} voltages for all possible VID codes are given in Table 4).
In pulse-skipping mode, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

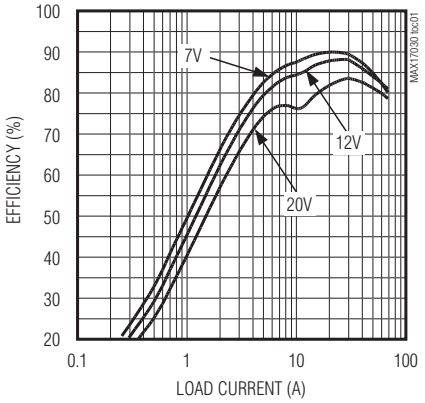
Note 4: On-time and minimum off-time specifications are measured from 50% to 50% at the DH_ pin, with LX_ forced to 0V, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.

Note 5: Specifications to -40°C and +105°C are guaranteed by design, not production tested.

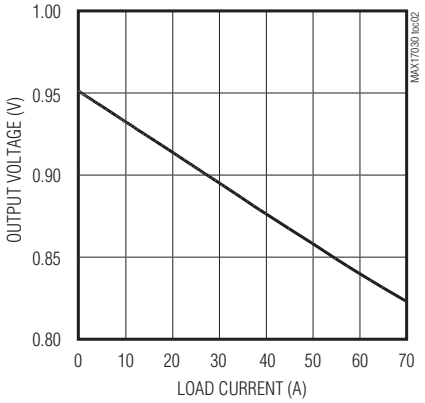
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 0.95V, T_A = +25°C, unless otherwise specified.)

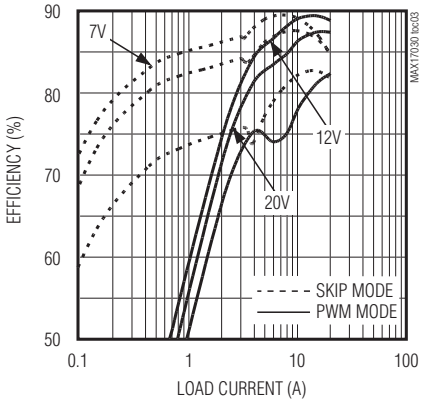
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 0.95V)



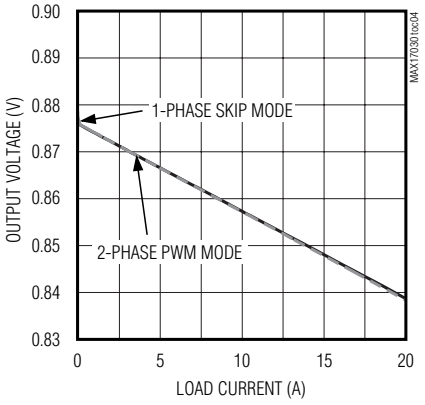
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 0.95V)



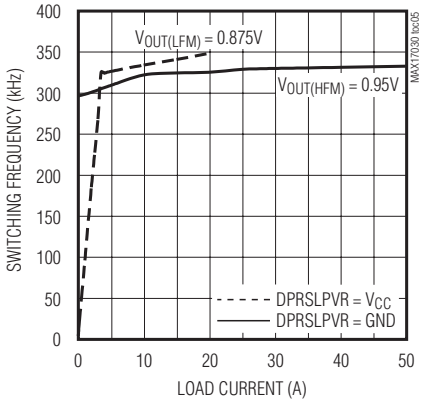
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



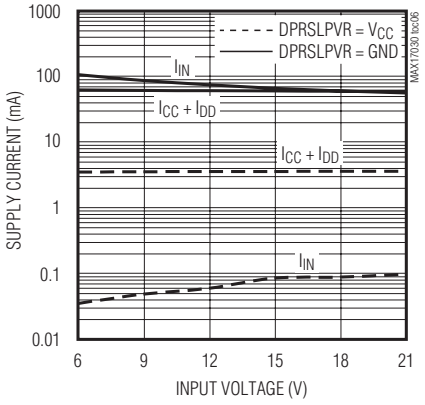
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



SWITCHING FREQUENCY vs. LOAD CURRENT



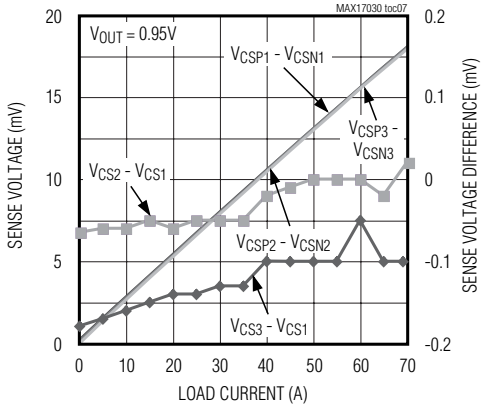
$V_{OUT(HFM)}$ = 0.95V NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



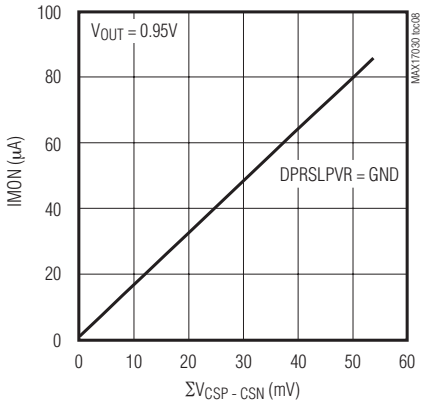
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 0.95V, T_A = +25°C, unless otherwise specified.)

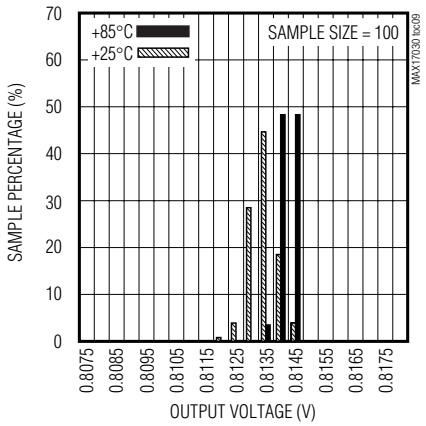
CURRENT BALANCE vs. LOAD CURRENT



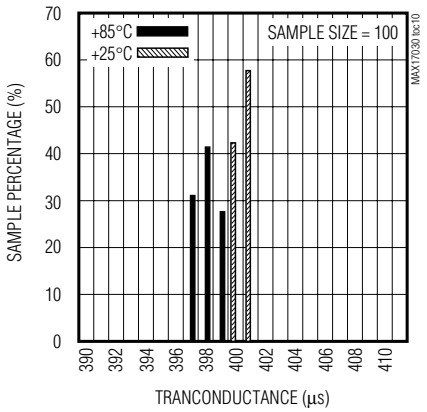
I_{IMON} vs. LOAD CURRENT



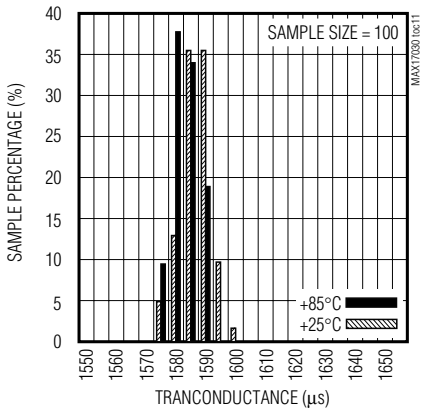
0.8125V OUTPUT VOLTAGE DISTRIBUTION



$G_{m(FB)}$ TRANSCONDUCTANCE DISTRIBUTION



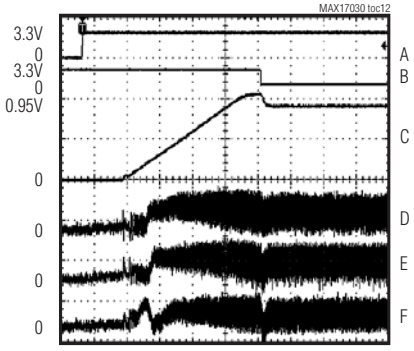
$G_{m(IMON)}$ TRANSCONDUCTANCE DISTRIBUTION



Typical Operating Characteristics (continued)

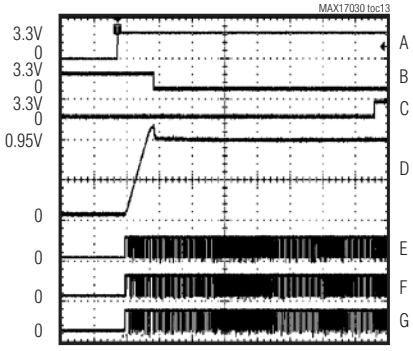
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 0.95V, T_A = +25°C, unless otherwise specified.)

SOFT-START WAVEFORM (UP TO $\overline{CLKEN}$)



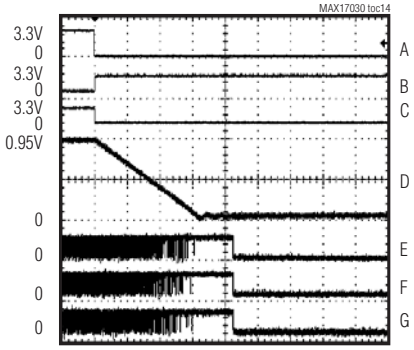
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 10V/div
C. V_{OUT}, 500mV/div
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div
F. I_{LX3}, 10A/div
I_{OUT}, 15A

SOFT-START WAVEFORM (UP TO PWRGD)



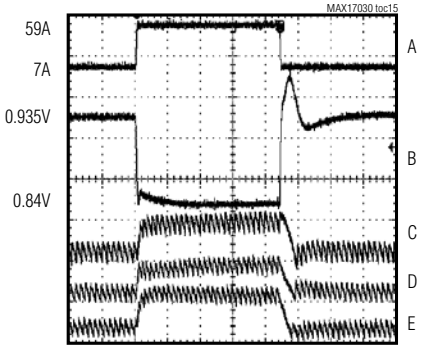
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 6.6V/div
C. PWRGD, 10V/div
D. V_{OUT}, 1V/div
E. DL1, 10V/div
F. DL2, 10V/div
G. DL3, 10V/div
I_{OUT}, 15A

SHUTDOWN WAVEFORM



A. $\overline{SHDN}$, 5V/div
B. PWRGD, 10V/div
C. $\overline{CLKEN}$, 10V/div
D. V_{OUT}, 500mV/div
E. DL1, 10V/div
F. DL2, 10V/div
G. DL3, 10V/div

LOAD-TRANSIENT RESPONSE (HFM MODE)



A. I_{OUT} = 7A - 59A
B. V_{OUT}, 50mV/div
C. I_{LX1}, 20A/div
D. I_{LX2}, 20A/div
E. I_{LX3}, 20A/div

Pin Description

PIN	NAME	FUNCTION
1	CSN3	Negative Input of the Output Current Sense of Phase 3. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
2	CSP3	Positive Input of the Output Current Sense of Phase 3. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. To disable phase 3, connect CSP3 to V_{CC} and CSN3 to GND.
3	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components such that the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
4	IMON	Current Monitor Output Pin. The output current at this pin is: $I_{IMON} = G_{M(IMON)} \times \Sigma V(CSP\_,CSN\_)$ where $G_{M(IMON)}$ = 1.6mS typical and Σ denotes summation over all enabled phases. An external resistor R_{IMON} between IMON and GNDS sets the current-monitor output voltage: $V_{IMON} = I_{LOAD} \times R_{SENSE} \times G_{M(IMON)} \times R_{IMON}$ where R_{SENSE} is the value of the effective current-sense resistance. Choose R_{IMON} such that V_{IMON} does not exceed 900mV at the maximum expected load current I_{MAX}. IMON is high impedance when the MAX17030/MAX17036 are in shutdown.
5	ILIM	Current-Limit Adjust Input. The valley positive current-limit threshold voltages at V(CSP_,CSN_) are precisely 1/10 the differential voltage V(TIME,ILIM) over a 0.1V to 0.5V range of V(TIME,ILIM). The valley negative current-limit thresholds are typically -125% of the corresponding valley positive current-limit thresholds. Connect ILIM to V_{CC} to get the default current-limit threshold setting of 22.5mV typ.
6	TIME	Slew-Rate Adjustment Pin. The total resistance R_{TIME} from TIME to GND sets the internal slew rate: Slew rate = (12.5mV/µs) x (71.5kΩ/R_{TIME}) where R_{TIME} is between 35.7kΩ and 178kΩ. This “normal” slew rate applies to transitions into and out of the low-power pulse-skipping modes and to the transition from boot mode to VID. The slew rate for startup and for entering shutdown is always 1/4 of normal. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the normal slew rate defined above.
7	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum.
8	FB	Feedback Voltage Input. The voltage at the FB pin is compared with the slew-rate-controlled target voltage by the error comparator (fast regulation loop), as well as by the internal voltage integrator (slow, accurate regulation loop). Having sufficient ripple signal at FB that is in phase with the sum of the inductor currents is essential for cycle-by-cycle stability. The external connections and compensation at FB depend on the desired DC and transient (AC) droop values. If DC droop = AC droop, then short FB to FBAC. To disable DC droop, connect FB to the remote-sensed output voltage through a resistor R and feed forward the FBAC ripple to FB through capacitor C, where the R x C time constant should be at least 3x the switching period per phase.

Pin Description (continued)

PIN	NAME	FUNCTION
9	FBAC	Output of the Voltage-Positioning Transconductance Amplifier. Connect a resistor R_{FBAC} between FBAC and the positive side of the feedback remote sense to set the transient (AC) droop based on the stability, load-transient response, and voltage-positioning gain requirements: $R_{FBAC} = R_{DROOP,AC}/[R_{SENSE} \times G_{m(FBAC)}]$ where $R_{DROOP,AC}$ is the transient (AC) voltage-positioning slope that provides an acceptable tradeoff between stability and load-transient response, $G_{m(FBAC)}$ = 400µS typ, and R_{SENSE} is the effective current-sense resistance that is used to provide the (CSP_, CSN_) current-sense voltages. A minimum $R_{DROOP,AC}$ value is required for stability, but if there are no ceramic output capacitors used, then the minimum requirement applies to $R_{ESR} + R_{DROOP,AC}$, where R_{ESR} is the effective ESR of the output capacitors. If lossless sensing (inductor DCR sensing) is used, use a thermistor-resistor network to minimize the temperature dependence of the voltage-positioning slope. FBAC is high impedance in shutdown.
10	GNDS	Feedback Remote-Sense Input, Negative Side. Normally connected to GND directly at the load. GNDS internally connects to a transconductance amplifier that fine tunes the output voltage compensating for voltage drops from the regulator ground to the load ground.
11	CSN2	Negative Input of the Output Current Sense of Phase 2. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
12	CSP2	Positive Input of the Output Current Sense of Phase 2. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. To disable phase 2, connect CSP2 to V_{CC} and CSN2 to GND.
13	$\overline{SHDN}$	Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to ground to put the IC into the 1µA (max at T_A = +25°C) shutdown state. During startup, the output voltage is ramped up at 1/4 the slew rate set by the TIME resistor to the boot voltage or to the target voltage. During the transition from normal operation to shutdown, the output voltage is ramped down at 1/6 the slew rate set by the TIME resistor. Forcing $\overline{SHDN}$ to 11V~13V to enter no-fault test mode clears the fault latches, disables transient phase overlap, and turns off the internal BST_-to-V_{DD} switches. However, internal diodes still exist between BST_ and V_{DD} in this state.
14	DPRSLPVR	Deeper Sleep VR Control Input. This low-voltage logic input indicates power usage and sets the operating mode together with $\overline{PSI}$ as shown in the truth table below. When DPRSLPVR is forced high, the controller is immediately set to 1-phase automatic pulse-skipping mode. The controller returns to forced-PWM mode when DPRSLPVR is forced low and the output is in regulation. The PWRGD upper threshold is blanked during any downward output-voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. During this blanking period, the overvoltage fault threshold is changed from a tracking [VID + 300mV] threshold to a fixed 1.5V threshold. The controller is in N-phase skip mode during startup including boot mode, but is in N-phase forced-PWM mode during the transition from boot mode to VID mode, during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phases 2 and 3 are disabled by connecting CSP2, CSP3 to V_{CC}, then only phase 1 is active in the above modes.

DPRSLPVR	$\overline{PSI}$	MODE
1	X	Very low current (1-phase skip)
0	0	Intermediate power potential (N-1-phase PWM)
0	1	Max power potential (full-phase PWM: N-phase or 1 phase as set by user at CSP2, CSP3)

Pin Description (continued)

PIN	NAME	FUNCTION
15	$\overline{PSI}$	This low-voltage logic input indicates power usage and sets the operating mode together with DPRSLPVR as shown in the truth table below. While DPRSLPVR is low, if $\overline{PSI}$ is forced low, the controller is immediately set to (N-1)-phase forced-PWM mode. The controller returns to N-phase forced-PWM mode when $\overline{PSI}$ is forced high. The controller is in N-phase skip mode during startup including boot mode, but is in N-phase forced-PWM mode during the transition from boot mode to VID mode, during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phases 2 and 3 are disabled by connecting CSP2, CSP3 to VCC, then only phase 1 is active in the above modes.
		DPRSLPVR / **$\overline{PSI}$** / **MODE** 1 / X / Very low current (1-phase skip) 0 / 0 / Intermediate power potential (N-1-phase PWM) 0 / 1 / Max power potential (full-phase PWM: N-phase or 1 phase as set by user at CSP2, CSP3)
16	TON	Switching Frequency Setting Input. An external resistor between the input power source and this pin sets the switching frequency according to the following equation: $f_{SW} = 1/(C_{TON} \times (R_{TON} + 6.5k\Omega))$ where C_{TON} = 16.26pF. The external resistor must also satisfy the requirement $[V_{IN(MIN)}/R_{TON}] \geq 10\mu A$ where $V_{IN(MIN)}$ is the minimum V_{IN} value expected in the application. TON is high impedance in shutdown.
17	$\overline{CLKEN}$	Clock Enable CMOS Push-Pull Logic Output Powered by V_{3P3}. This inverted logic output indicates when the output voltage sensed at FB is in regulation. $\overline{CLKEN}$ is forced high in shutdown and during soft-start and soft-stop transitions. $\overline{CLKEN}$ is forced low during dynamic VID transitions and for an additional 20µs after the transition is completed. $\overline{CLKEN}$ is the inverse of PWRGD, except for the 5ms PWRGD startup delay period after $\overline{CLKEN}$ is pulled low. See the startup timing diagram (Figure 9). The $\overline{CLKEN}$ upper threshold is blanked during any downward output-voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation.
18	PWRGD	Open-Drain Power-Good Output. After output-voltage transitions, except during power-up and power-down, if FB is in regulation, then PWRGD is high impedance. PWRGD is low during startup, continues to be low while the output is at the boot voltage, and stays low until 5ms (typ) after $\overline{CLKEN}$ goes low, after which it starts monitoring the FB voltage and goes high if FB is within the PWRGD threshold window. PWRGD is forced low during soft-shutdown and while in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions), and continues to be forced high impedance for an additional 20µs after the transition is completed. The PWRGD upper threshold is blanked during any downward output-voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. A pullup resistor on PWRGD causes additional finite shutdown current.
19	$\overline{DRSKP}$	Driver Skip Control Output. Push/pull logic output that controls the operating mode of the skip-mode driver IC. $\overline{DRSKP}$ swings from V_{DD} to GND. When $\overline{DRSKP}$ is high, the driver ICs operate in forced-PWM mode. When $\overline{DRSKP}$ is low, the driver ICs enable their zero-crossing comparators and operate in pulse-skipping mode. $\overline{DRSKP}$ goes low at the end of the soft-shutdown sequence, instructing the external drivers to shut down.

Pin Description (continued)

PIN	NAME	FUNCTION
20	PWM3	PWM Signal Output for Phase 3. Swings from GND to V_{DD}. Three-state whenever phase 3 is disabled (in shutdown, when CSP3 is connected to V_{CC}, and when operating with fewer than all phases).
21	BST2	Phase 2 Boost Flying Capacitor Connection. BST2 is the internal upper supply rail for the DH2 high-side gate driver. An internal switch between V_{DD} and BST2 charges the BST2-LX2 flying capacitor while the low-side MOSFET is on (DL2 pulled high).
22	LX2	Phase 2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to phase 2's zero-crossing comparator.
23	DH2	Phase 2 High-Side Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
24	DL2	Phase 2 Low-Side Gate-Driver Output. DL2 swings from GND to V_{DD}. DL2 is forced low in shutdown. DL2 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL2 is forced low in skip mode after detecting an inductor current zero crossing.
25	$\overline{VRHOT}$	Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{VRHOT}$ is high impedance in shutdown.
26	V_{DD}	Supply Voltage Input for the DL_ Drivers. V_{DD} is also the supply voltage used to internally recharge the BST_-LX_ flying capacitor during the times the respective DL_s are high. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to GND with a 1µF or greater ceramic capacitor.
27	DL1	Phase 1 Low-Side Gate-Driver Output. DL1 swings from GND to V_{DD}. DL1 is forced low in shutdown. DL1 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL1 is forced low in skip mode after detecting an inductor current zero crossing.
28	DH1	Phase 1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
29	LX1	Phase 1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to phase 1's zero-crossing comparator.
30	BST1	Phase 1 Boost Flying Capacitor Connection. BST1 is the internal upper supply rail for the DH1 high-side gate driver. An internal switch between V_{DD} and BST1 charges the BST1-LX1 flying capacitor while the low-side MOSFET is on (DL1 pulled high).
31	PGD_IN	Power-Good Logic Input Pin that Indicates the Power Status of Other System Rails and Used for Supply Sequencing. During startup, after soft-starting to the boot voltage, the output voltage remains at V_{BOOT}, and the $\overline{CLKEN}$ and PWRGD outputs remain high and low, respectively, as long as the PGD_IN input stays low. When PGD_IN later goes high, the output is allowed to transition to the voltage set by the VID code, and $\overline{CLKEN}$ is allowed to go low. During normal operation, if PGD_IN goes low, the controller immediately forces $\overline{CLKEN}$ high and PWRGD low, and slews the output to the boot voltage while in skip mode at 1/4 the normal slew rate set by the TIME resistor. The output then stays at the boot voltage until the controller is turned off or power cycled, or until PGD_IN goes high again.
32–38	D0–D6	Low-Voltage (1.0V Logic) VID DAC Code Inputs. The D0–D6 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic-level voltages on D0–D6 (see Table 4). The 1111111 code corresponds to a shutdown mode. When this code is detected, The MAX17030/MAX17036 initiate a soft-shutdown transition identical to the shutdown transition for a $\overline{SHDN}$ falling edge. After slewing the output to 0V, it forces DH_, DL_, and $\overline{DRSKP}$ low, and three-states PWM3. The IC remains active and its V_{CC} quiescent current consumption stays the same as in normal operation. If D6–D0 is changed from 1111111 to a different code, the MAX17030/MAX17036 initiate a startup sequence identical to the startup sequence for a $\overline{SHDN}$ rising edge.
39	CSP1	Positive Input of the Output Current Sense of Phase 1. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

Pin Description (continued)

PIN	NAME	FUNCTION
40	CSN1	Negative Input of the Output Current Sense of Phase 1. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. A 10Ω discharge FET is turned on in UVLO event or thermal shutdown, or at the end of soft-shutdown.
—	PAD (GND)	Exposed Backplate (Pad) of Package. Internally connected to both analog ground and power (driver) grounds. Connect to the ground plane through a thermally enhanced via.

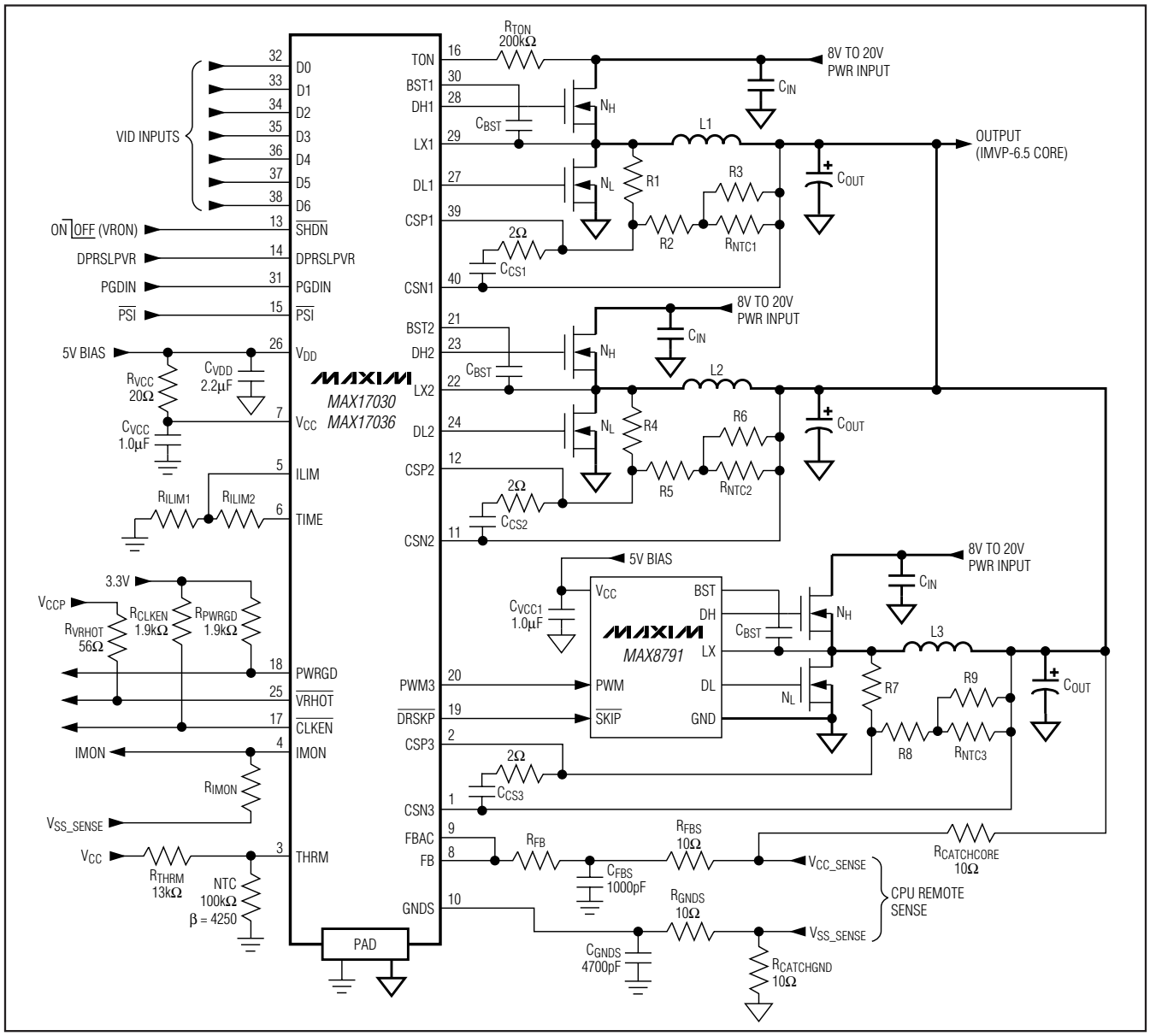


Figure 1. Standard 3-Phase IMVP-6.5 Application Circuit

Table 1. Component Selection for Standard Applications

DESIGN PARAMETERS	IMVP-6.5 XE CORE 3-PHASE	IMVP-6.5 SV CORE 3-PHASE	IMVP-6.5 SV CORE 2-PHASE
Circuit	Figure 1	Figure 1	Figure 2
Input Voltage Range	8V to 20V	8V to 20V	8V to 20V
Maximum Load Current	65A (48A TDC)	52A (38A TDC)	52A (38A TDC)
Transient Load Current	49A (100A/µs)	39A (100A/µs)	39A (100A/µs)
Load Line	-1.9mV/A	-1.9mV/A	-1.9mV/A
POC Setting	110	101	101
TON Resistance (R_{TON})	200kΩ (f_{SW} = 300kHz)	200kΩ (f_{SW} = 300kHz)	200kΩ (f_{SW} = 300kHz)
Inductance (L)	0.36µH, 36A, 0.82mΩ (10mm x 10mm) Panasonic ETQP4LR36ZFC	0.42µH, 20A, 1.55mΩ (7mm x 7mm) NEC/TOKIN MPC0740LR42C	0.36µH, 36A, 0.82mΩ (10mm x 10mm) Panasonic ETQP4LR36ZFC
High-Side MOSFET (N_H)	Fairchildsemi 1x FDS6298 9.4mΩ/12mΩ (typ/max) Toshiba 1x TPCA8030-H 9.6mΩ/13.4mΩ (typ/max)	Fairchildsemi 1x FDS6298 9.4mΩ/12mΩ (typ/max) Toshiba 1x TPCA8030-H 9.6mΩ/13.4mΩ (typ/max	Fairchildsemi 1x FDS6298 9.4mΩ/12mΩ (typ/max) Toshiba 1x TPCA8030-H 9.6mΩ/13.4mΩ (typ/max)
Low-Side MOSFET (N_L)	Fairchildsemi 2x FDS8670 4.2mΩ/5mΩ (typ/max) Toshiba 2x TPCA8019-H	Fairchildsemi 1x FDS8670 4.2mΩ/5mΩ (typ/max) Toshiba 1x TPCA8019-H	Fairchildsemi 2x FDS8670 4.2mΩ/5mΩ (typ/max) Toshiba 2x TPCA8019-H
Output Capacitors (C_{OUT}) (MAX17030 Only) **Contact Maxim for MAX17036 reference design**	4x 330µF, 2V, 4.5mΩ Panasonic EEFSXOD331E4 or NEC/Tokin PSGVOE337M4.5 27x 22µF, 6.3V X5R ceramic capacitor (0805)	3x 330µF, 2V, 4.5mΩ Panasonic EEFSXOD331E4 or NEC/Tokin PSGVOE337M4.5 27x 22µF, 6.3V X5R ceramic capacitor (0805)	4x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)
Input Capacitors (C_{IN})	6x 10µF 25V ceramic (1210)	4x 10µF 25V ceramic (1210)	4x 10µF 25V ceramic (1210)
TIME-ILIM Resistance (R_{ILIM2})	14kΩ	14kΩ	16.9kΩ
ILIM-GND Resistance (R_{ILIM1})	137kΩ	137kΩ	133kΩ
FB Resistance (R_{FB})	6.04kΩ	453kΩ	6.04kΩ
IMON Resistance (R_{IMON})	12.1kΩ	10.2kΩ	14kΩ
LX-CSP Resistance	2.21kΩ (R1, R4, R7)	1.4kΩ (R1, R4, R7)	2.21kΩ (R1, R7)
CSP-CSN Resistance	3.24kΩ (R2, R5, R8) 40.2kΩ (R3, R6, R9)	2kΩ (R2, R5, R8) 40.2kΩ (R3, R6, R9)	3.24kΩ (R2, R8) 40.2kΩ (R3, R9)
DCR Sense NTC (R_{NTC})	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F
DCR Sense Capacitance (C_{SENSE})	0.22µF, 6V ceramic (0805)	0.22µF, 6V ceramic (0805)	0.22µF, 6V ceramic (0805)

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corp.	www.avxcorp.com
Fairchild Semiconductor	www.fairchildsemi.com
NEC/TOKIN America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com
SANYO Electric Co., Ltd.	www.sanyodevice.com

MANUFACTURER	WEBSITE
Siliconix (Vishay)	www.vishay.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Toshiba America Electronic Components, Inc.	www.toshiba.com/taec

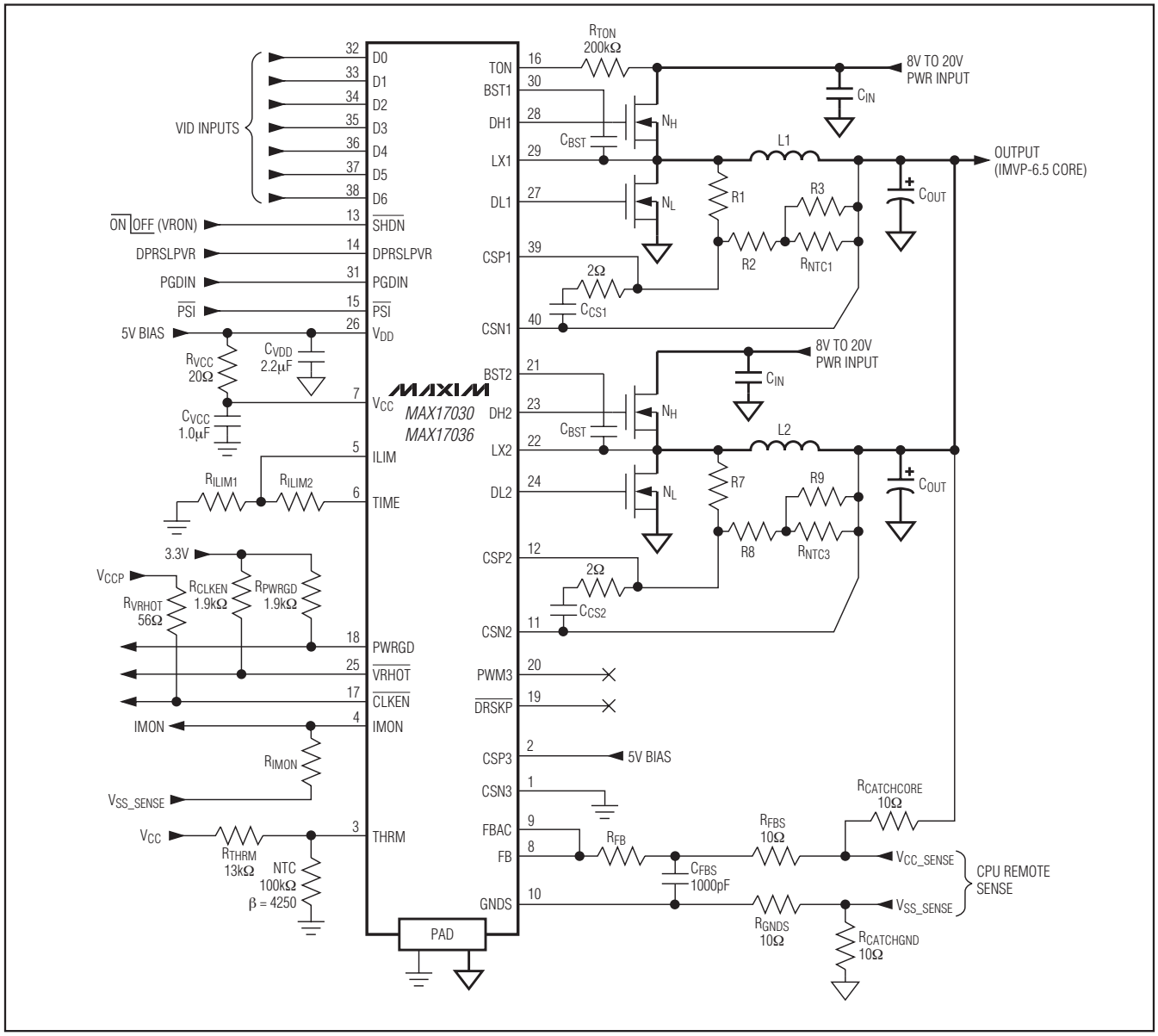


Figure 2. Standard 2-Phase IMVP-6.5 Application Circuit

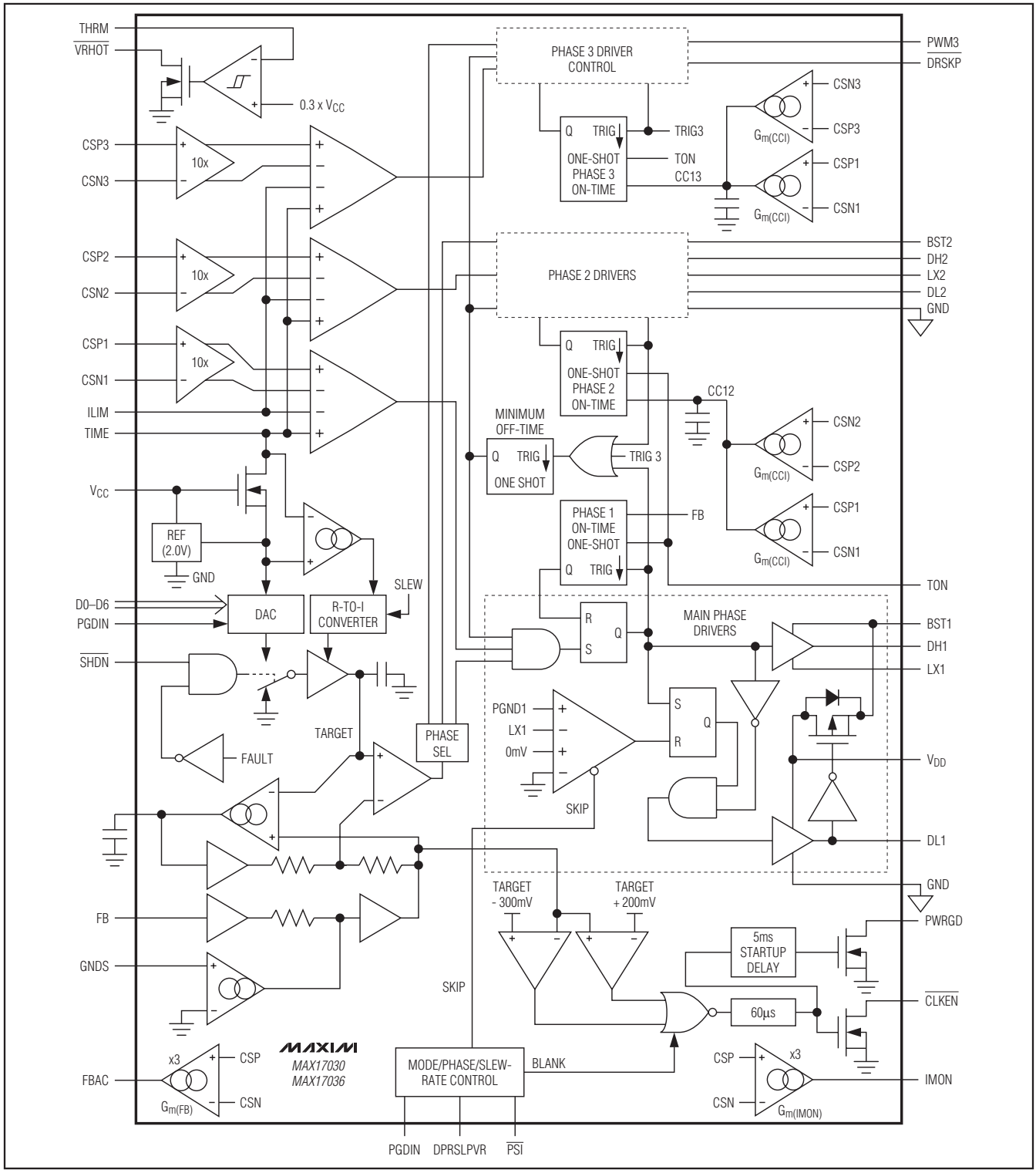


Figure 3. Functional Diagram

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

Detailed Description

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 3). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 120° out-of-phase operation by alternately triggering the three phases after the error comparator drops below the output-voltage set point.

Triple 120° Out-of-Phase Operation

The three phases in the MAX17030/MAX17036 operate 120° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX17030/MAX17036 ideal for high-power, cost-sensitive applications.

The MAX17030/MAX17036 share the current between three phases that operate 120° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of each phase is effectively reduced, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance can be achieved with fewer or less-expensive input capacitors.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}\left(Q_{G(LOW)} + Q_{G(HIGH)}\right)$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be connected together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON)

Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period $T_{SW} = 1/f_{SW}$, per phase:

$$T_{SW} = 16.26pF \times (R_{TON} + 6.5k\Omega)$$

A 96.75kΩ to 303.25kΩ corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

TON Open-Circuit Protection

The TON input includes open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The MAX17030/MAX17036 detect an open-circuit fault if the TON current drops below 10µA for any reason—the TON resistor (R_{TON}) is unpopulated, a high resistance value is used, the input voltage is low, etc. Under these conditions, the MAX17030/MAX17036 stop switching (DH and DL pulled low) and immediately set the fault latch. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

On-Time One-Shot

The MAX17030/MAX17036 contain a fast, low-jitter, adjustable one-shot that sets the high-side MOSFETs on-time. It is shared among the three phases. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V+ input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON} = \frac{T_{SW}\left(V_{FB} + 0.075V\right)}{V_{IN}}$$

The one-shot for the second phase and third phase varies the on-time in response to the input voltage and the difference between the main and the other inductor currents. Two identical transconductance amplifiers integrate the difference between the master and each slave's current-sense signals. The summed output is connected to an internal integrator for each master-slave pair, which serves as the input to the respective slave's high-side MOSFET TON timer.

When the main and other phase current-sense signals ($V_{CM} = V_{CMP} - V_{CMN}$ and $V_{CS} = V_{CSP} - V_{CSM}$) become unbalanced, the transconductance amplifiers adjust the other phase's on-time, which increases or decreases the phase inductor current until the current-sense signals are properly balanced:

$$t_{ON(SEC)} = T_{SW}\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$
$$= T_{SW}\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + T_{SW}\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$
$$= (\text{Main On-time}) + (\text{Secondary Current Balance Correction})$$

where V_{CCI} is the internal integrator node for each slave's current-balance integrator, and Z_{CCI} is the effective impedance at that node.

During phase overlap, t_{ON} is calculated based on phase 1's on-time requirements, but reduced by 33% when operating with three phases.

For a 3-phase regulator, each phase cannot be enabled until the other 2 phases have completed their on-time and the minimum off-times have expired. As such, the minimum period is limited by 3 x (t_{ON} + $t_{OFF(MIN)}$). Maximum t_{ON} is dependent on minimum V_{IN} and maximum output voltage:

$$T_{SW(MIN)} = N_{PH} \times (t_{ON(MAX)} + t_{OFF(MIN)})$$

where:

$$t_{ON(MAX)} = V_{FB(MAX)}/V_{IN(MIN} \times T_{SW(MIN)}$$

so:

$$T_{SW(MIN)} = t_{OFF(MIN)}/[1/N_{PH} - V_{IN(MAX)}/V_{IN(MIN)}]$$

Hence, for a 7V input and 1.1V output, 500kHz is the maximum switching frequency. Running at this limit is not desirable as there is no room to allow the regulator to make adjustments without triggering phase overlap. For a 3-phase, high-current application with minimum 8V input, the practical switching frequency is 300kHz.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by parasitics in the conduction paths and propagation delays. For loads above the critical conduction point, where the dead-time effect (LX flying high and conducting through the high-side FET body diode) is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DIS})}{t_{ON}(V_{IN} + V_{DIS} - V_{CHG})}$$

where V_{DIS} and V_{CHG} are the sum of the parasitic voltage drops in the inductor discharge and charge paths, including MOSFET, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as determined above.

Current Sense

The MAX17030/MAX17036 sense the output current of each phase allowing the use of current-sense resistors on inductor DCR as the current-sense element. Low-offset amplifiers are used for current balance, voltage-positioning gain, and current limit.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. The initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and current monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 4). The RC network should match the inductor's time constant (L/R_{DCR}):

$$R_{CS} = \left(\frac{R2}{R1 + R2}\right)R_{DCR}$$

and:

$$R_{CS} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the typical inductance and R_{DCR} values provided by the inductor manufacturer. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1//R2 to be less than 2kΩ and use the above equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 4). The ESL induced voltage step might affect the average current-sense voltage. The RC filter's time constant should match the L_{ESL}/R_{SENSE} time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R_{EQ}$$

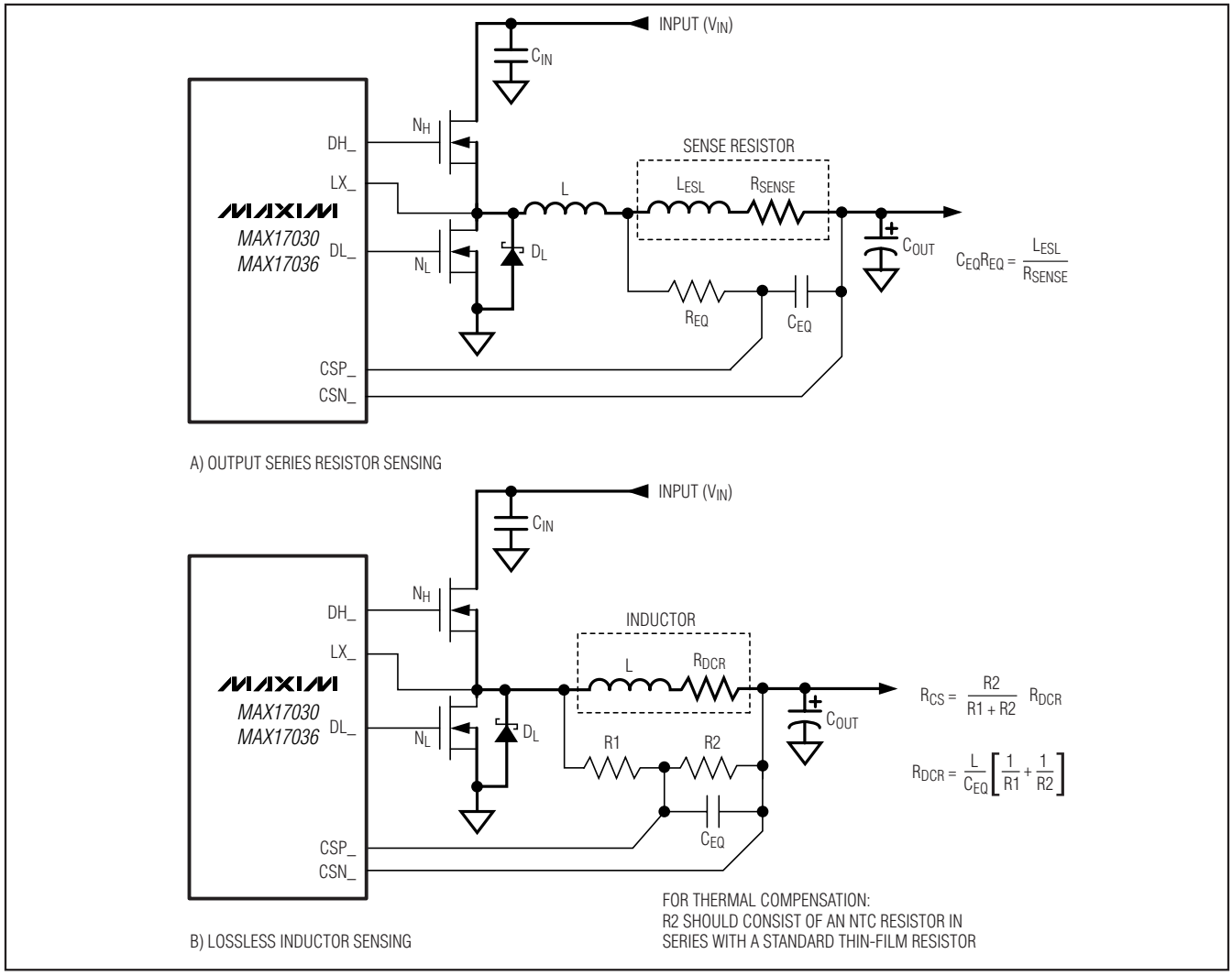


Figure 4. Current-Sense Methods

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, and C_{EQ} and R_{EQ} are the time-constant matching components.

Current Balance

The MAX17030/MAX17036 integrate the difference between the current-sense voltages and adjust the on-time of the secondary phase to maintain current balance. The current balance relies on the accuracy of the current-sense signals across the current-sense resistor or inductor DCR. With active current balancing, the current mismatch is determined by the current-sense resistor or inductor DCR values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where $R_{SENSE} = R_{CM} = R_{CS}$ and $V_{OS(IBAL)}$ is the current balance offset specification in the *Electrical Characteristics* table.

The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches resulting in different di/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the voltage across the current-sense resistors or inductor DCR at the current-sense inputs (CSP_ to CSN_). If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current of the selected phase drops below the valley current-limit threshold. When any one phase exceeds the current limit, all phases are effectively current limited since the interleaved controller does not initiate a cycle with the next phase.

Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage.

The positive valley current-limit threshold voltage at CSP to CSN equals precisely 1/10 of the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). Connect ILIM directly to V_{CC} to set the default current-limit threshold setting of 22.5mV (typ).

The negative current-limit threshold (forced-PWM mode only) is nominally -125% of the corresponding valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off, and DH turns on—allowing the inductor current to remain above the negative current threshold.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_).

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State Droop)

The MAX17030/MAX17036 include a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by summing the current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output Voltage Selection* section, and the FB amplifier's output current (I_{FB}) is determined by the sum of the current-sense voltages:

$$I_{FB} = G_{m(FB)} \sum_{X=1}^{\eta_{PH}} V_{CSX}$$

where $V_{CSX} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{m(FB)}$ is typically 400µS as defined in the *Electrical Characteristics*.

Differential Remote Sense

The MAX17030/MAX17036 include differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor (R_{FB}). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor (R_{FB}) and ground sense (GNDS) input directly to the processor's remote sense outputs as shown in Figure 1.

Integrator Amplifier

An internal integrator amplifier forces the DC average of the FB voltage to equal the target voltage, allowing accurate DC output-voltage regulation regardless of the output ripple voltage.

The MAX17030/MAX17036 disable the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (DPRSLPVR = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Transient Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 120° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. In order to provide fast transient response, the MAX17030/MAX17036 support a phase overlap mode, which allows the triple regulators to operate in-phase when heavy load transients are detected, effectively reducing the response time. After any high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on all high-side MOSFETs with the same on-time during the next on-time cycle. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum

off-time expires. The on-time for each phase is based on the input voltage to FB ratio (i.e., follows the master on-time), but reduced by 33% in a 3-phase configuration, and not reduced in a 2-phase configuration. This maximizes the total inductor current slew rate.

After the phase-overlap mode ends, the controller automatically begins with the next phase. For example, if phase 2 provided the last on-time pulse before overlap operation began, the controller starts switching with phase 3 when overlap operation ends.

Nominal Output Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected VID voltage. On startup, the MAX17030/MAX17036 slew the target voltage from ground to the preset boot voltage. Table 3 is the operating mode truth table.

DAC Inputs (D0–D6)

The digital-to-analog converter (DAC) programs the output voltage using the D0–D6 inputs. D0–D6 are low-voltage (1.0V) logic inputs, designed to interface directly with the CPU. Do not leave D0–D6 unconnected. Changing D0–D6 initiates a transition to a new output-voltage level. Change D0–D6 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings might cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the IMVP-6.5 (Table 4) specifications.

OFF Code

VID = 1111111 is defined as an OFF code. When the OFF code is set, the MAX17030/MAX17036 go through the same shutdown sequence as though $\overline{SHDN}$ has been pulled low—output discharged to zero, $\overline{CLKEN}$ high, and PWRGD low. Only the IC supply currents remain at the operating levels rather than the shutdown level. When exiting from the OFF code, the MAX17030/MAX17036 go through the boot sequence, similar to the sequence when $\overline{SHDN}$ is first pulled high.

Table 3. Operating Mode Truth Table

INPUTS			PHASE OPERATION*	OPERATING MODE
$\overline{SHDN}$	DPRSLPVR	$\overline{PSI}$		
GND	X	X	Disabled	Low-Power Shutdown Mode. DL1 and DL2 forced low, and the controller is disabled. The supply current drops to 1µA (max).
Rising	X	X	Multiphase Pulse Skipping 1/4 R_{TIME} Slew Rate	Startup/Boot. When $\overline{SHDN}$ is pulled high, the MAX17030/MAX17036 begin the startup sequence. Once the REF is above 1.84V, the controller enables the PWM controller and ramps the output voltage up to the boot voltage. See Figure 9.
High	Low	High	Multiphase Forced-PWM Nominal R_{TIME} Slew Rate	Full Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4).
High	Low	Low	(N-1)-Phase Forced-PWM Nominal R_{TIME} Slew Rate	Intermediate Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When $\overline{PSI}$ is pulled low, the MAX17030/MAX17036 immediately disable phase 3, PWM3 is three-state, and $\overline{DRSKP}$ is low.
High	High	X	1-Phase Pulse Skipping Nominal R_{TIME} Slew Rate	Deeper Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When DPRSLPVR is pulled high, the MAX17030/MAX17036 immediately enter 1-phase pulse-skipping operation allowing automatic PWM/PFM switchover under light loads. The PWRGD and $\overline{CLKEN}$ upper thresholds are blanked. DH2 and DL2 are pulled low, PWM3 is three-state and $\overline{DRSKP}$ is low.

**Multiphase operation = All enabled phases active.*

Table 3. Operating Mode Truth Table (continued)

INPUTS			PHASE OPERATION*	OPERATING MODE
$\overline{SHDN}$	DPRSLPVR	$\overline{PSI}$		
Falling	X	X	Multiphase Forced-PWM 1/4 R_{TIME} Slew Rate	Shutdown. When $\overline{SHDN}$ is pulled low, the MAX17030/MAX17036 immediately pull PWRGD low, $\overline{CLKEN}$ becomes high impedance, all enabled phases are activated, and the output voltage is ramped down to 12.5mV; then DH and DL are pulled low and CSNI discharge FET is turned on.
High	X	X	Disabled	Fault Mode. The fault latch has been set by the MAX17030/MAX17036 UVP or thermal-shutdown protection, or by the OVP protection. The controller remains in fault mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

**Multiphase operation = All enabled phases active.*

Table 4. IMVP-6.5 Output Voltage VID DAC Codes

D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)		D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	0	0	1.5000		1	0	0	0	0	0	0	0.7000
0	0	0	0	0	0	1	1.4875		1	0	0	0	0	0	1	0.6875
0	0	0	0	0	1	0	1.4750		1	0	0	0	0	1	0	0.6750
0	0	0	0	0	1	1	1.4625		1	0	0	0	0	1	1	0.6625
0	0	0	0	1	0	0	1.4500		1	0	0	0	1	0	0	0.6500
0	0	0	0	1	0	1	1.4375		1	0	0	0	1	0	1	0.6375
0	0	0	0	1	1	0	1.4250		1	0	0	0	1	1	0	0.6250
0	0	0	0	1	1	1	1.4125		1	0	0	0	1	1	1	0.6125
0	0	0	1	0	0	0	1.4000		1	0	0	1	0	0	0	0.6000
0	0	0	1	0	0	1	1.3875		1	0	0	1	0	0	1	0.5875
0	0	0	1	0	1	0	1.3750		1	0	0	1	0	1	0	0.5750
0	0	0	1	0	1	1	1.3625		1	0	0	1	0	1	1	0.5625
0	0	0	1	1	0	0	1.3500		1	0	0	1	1	0	0	0.5500
0	0	0	1	1	0	1	1.3375		1	0	0	1	1	0	1	0.5375
0	0	0	1	1	1	0	1.3250		1	0	0	1	1	1	0	0.5250
0	0	0	1	1	1	1	1.3125		1	0	0	1	1	1	1	0.5125
0	0	1	0	0	0	0	1.3000		1	0	1	0	0	0	0	0.5000
0	0	1	0	0	0	1	1.2875		1	0	1	0	0	0	1	0.4875
0	0	1	0	0	1	0	1.2750		1	0	1	0	0	1	0	0.4750
0	0	1	0	0	1	1	1.2625		1	0	1	0	0	1	1	0.4625
0	0	1	0	1	0	0	1.2500		1	0	1	0	1	0	0	0.4500
0	0	1	0	1	0	1	1.2375		1	0	1	0	1	0	1	0.4375
0	0	1	0	1	1	0	1.2250		1	0	1	0	1	1	0	0.4250
0	0	1	0	1	1	1	1.2125		1	0	1	0	1	1	1	0.4125
0	0	1	1	0	0	0	1.2000		1	0	1	1	0	0	0	0.4000
0	0	1	1	0	0	1	1.1875		1	0	1	1	0	0	1	0.3875

Table 4. IMVP-6.5 Output Voltage VID DAC Codes (continued)

D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	1	1	0	1	0	1.1750	1	0	1	1	0	1	0	0.3750
0	0	1	1	0	1	1	1.1625	1	0	1	1	0	1	1	0.3625
0	0	1	1	1	0	0	1.1500	1	0	1	1	1	0	0	0.3500
0	0	1	1	1	0	1	1.1375	1	0	1	1	1	0	1	0.3375
0	0	1	1	1	1	0	1.1250	1	0	1	1	1	1	0	0.3250
0	0	1	1	1	1	1	1.1125	1	0	1	1	1	1	1	0.3125
0	1	0	0	0	0	0	1.1000	1	1	0	0	0	0	0	0.3000
0	1	0	0	0	0	1	1.0875	1	1	0	0	0	0	1	0.2875
0	1	0	0	0	1	0	1.0750	1	1	0	0	0	1	0	0.2750
0	1	0	0	0	1	1	1.0625	1	1	0	0	0	1	1	0.2625
0	1	0	0	1	0	0	1.0500	1	1	0	0	1	0	0	0.2500
0	1	0	0	1	0	1	1.0375	1	1	0	0	1	0	1	0.2375
0	1	0	0	1	1	0	1.0250	1	1	0	0	1	1	0	0.2250
0	1	0	0	1	1	1	1.0125	1	1	0	0	1	1	1	0.2125
0	1	0	1	0	0	0	1.0000	1	1	0	1	0	0	0	0.2000
0	1	0	1	0	0	1	0.9875	1	1	0	1	0	0	1	0.1875
0	1	0	1	0	1	0	0.9750	1	1	0	1	0	1	0	0.1750
0	1	0	1	0	1	1	0.9625	1	1	0	1	0	1	1	0.1625
0	1	0	1	1	0	0	0.9500	1	1	0	1	1	0	0	0.1500
0	1	0	1	1	0	1	0.9375	1	1	0	1	1	0	1	0.1375
0	1	0	1	1	1	0	0.9250	1	1	0	1	1	1	0	0.1250
0	1	0	1	1	1	1	0.9125	1	1	0	1	1	1	1	0.1125
0	1	1	0	0	0	0	0.9000	1	1	1	0	0	0	0	0.1000
0	1	1	0	0	0	1	0.8875	1	1	1	0	0	0	1	0.0875
0	1	1	0	0	1	0	0.8750	1	1	1	0	0	1	0	0.0750
0	1	1	0	0	1	1	0.8625	1	1	1	0	0	1	1	0.0625
0	1	1	0	1	0	0	0.8500	1	1	1	0	1	0	0	0.0500
0	1	1	0	1	0	1	0.8375	1	1	1	0	1	0	1	0.0375
0	1	1	0	1	1	0	0.8250	1	1	1	0	1	1	0	0.0250
0	1	1	0	1	1	1	0.8125	1	1	1	0	1	1	1	0.0125
0	1	1	1	0	0	0	0.8000	1	1	1	1	0	0	0	0
0	1	1	1	0	0	1	0.7875	1	1	1	1	0	0	1	0
0	1	1	1	0	1	0	0.7750	1	1	1	1	0	1	0	0
0	1	1	1	0	1	1	0.7625	1	1	1	1	0	1	1	0
0	1	1	1	1	0	0	0.7500	1	1	1	1	1	0	0	0
0	1	1	1	1	0	1	0.7375	1	1	1	1	1	0	1	0
0	1	1	1	1	1	0	0.7250	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	0.7125	1	1	1	1	1	1	1	Off

Suspend Mode

When the processor enters low-power deeper sleep mode, the IMVP-6.5 CPU sets the VID DAC code to a lower output voltage and drives DPRSLPVR high. The MAX17030/MAX17036 respond by slewing the internal target voltage to the new DAC code, switching to single-phase operation, and letting the output voltage gradually drift down to the deeper sleep voltage. During the transition, the MAX17030/MAX17036 blank both the upper and lower PWRGD and $\overline{CLKEN}$ thresholds until 20µs after the internal target reaches the deeper sleep voltage. Once the 20µs timer expires, the MAX17030/MAX17036 reenable the lower PWRGD and $\overline{CLKEN}$ threshold, but keep the upper threshold blanked.

Output-Voltage-Transition Timing

At the beginning of an output-voltage transition, the MAX17030/MAX17036 blank both PWRGD thresholds, preventing the PWRGD open-drain output from changing states during the transition. The controller enables the lower PWRGD threshold approximately 20µs after the slew-rate controller reaches the target output voltage, but the upper PWRGD threshold is enabled only if the controller remains in forced-PWM operation. If the controller enters pulse-skipping operation, the upper PWRGD threshold remains blanked. The slew rate (set by resistor R_{TIME}) must be set fast enough to ensure that the transition can be completed within the maximum allotted time.

The MAX17030/MAX17036 automatically control the current to the minimum level required to complete the transition. The total transition time depends on R_{TIME}, the voltage difference, and the accuracy of the slew-rate controller (C_{SLEW} accuracy). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit. For all dynamic VID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{(dV_{TARGET}/dt)}$$

where $dV_{TARGET}/dt = 12.5mV/\mu s \times 71.5k\Omega/R_{TIME}$ is the slew rate, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See TIME Slew-Rate Accuracy in the *Electrical Characteristics* for slew-rate limits. For soft-start and shutdown, the controller automatically reduces the slew rate to 1/4.

The average inductor current per phase required to make an output-voltage transition is:

$$I_L \cong \frac{C_{OUT}}{\eta_{TOTAL}} \times (dV_{TARGET}/dt)$$

where dV_{TARGET}/dt is the required slew rate, C_{OUT} is the total output capacitance, and η_{TOTAL} is the number of active phases.

Deeper Sleep Transitions

When DPRSLPVR goes high, the MAX17030/MAX17036 immediately disable phases 2 and 3 (DH2, DL2 forced low, PWM3 three-state, $\overline{DRSKP}$ low), and enter pulse-skipping operation (see Figures 5 and 6). If the VIDs are set to a lower voltage setting, the output drops at a rate determined by the load and the output capacitance. The internal target still ramps as before, and PWRGD remains blanked high impedance until 20µs after the output voltage reaches the internal target. Once this time expires, PWRGD monitors only the lower threshold:

- **Fast C4E Deeper Sleep Exit:** When exiting deeper sleep (DPRSLPVR pulled low) while the output voltage still exceeds the deeper sleep voltage, the MAX17030/MAX17036 quickly slew (50mV/µs min regardless of R_{TIME} setting) the internal target voltage to the DAC code provided by the processor as long as the output voltage is above the new target. The controller remains in skip mode until the output voltage equals the internal target. Once the internal target reaches the output voltage, phase 2 is enabled. The controller blanks PWRGD and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 5.
- **Standard C4 Deeper Sleep Exit:** When exiting deeper sleep (DPRSLPVR pulled low) while the output voltage is regulating to the deeper sleep voltage, the MAX17030/MAX17036 immediately activate all enabled phases and ramp the output voltage to the LFM DAC code provided by the processor at the slew rate set by R_{TIME}. The controller blanks PWRGD and $\overline{CLKEN}$ (forced high impedance) until 20µs after the transition is completed. See Figure 6.

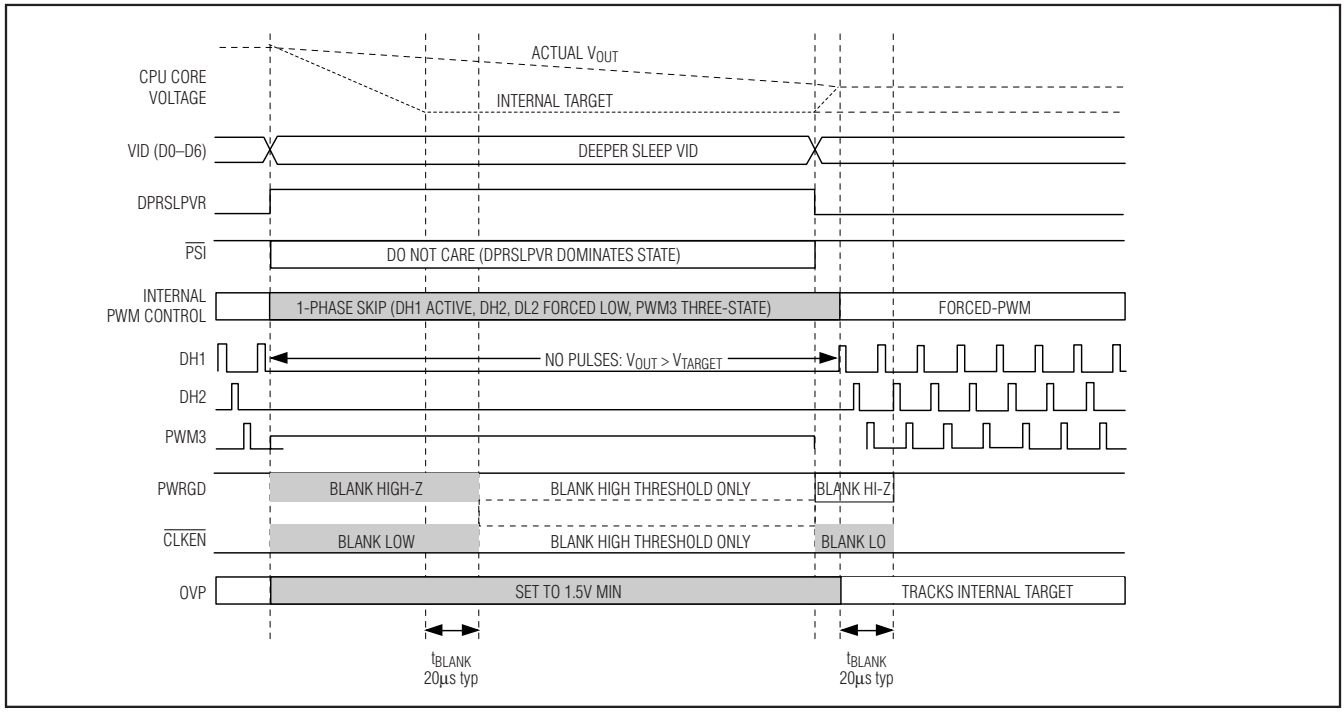


Figure 5. C4E (C4 Early Exit) Transition

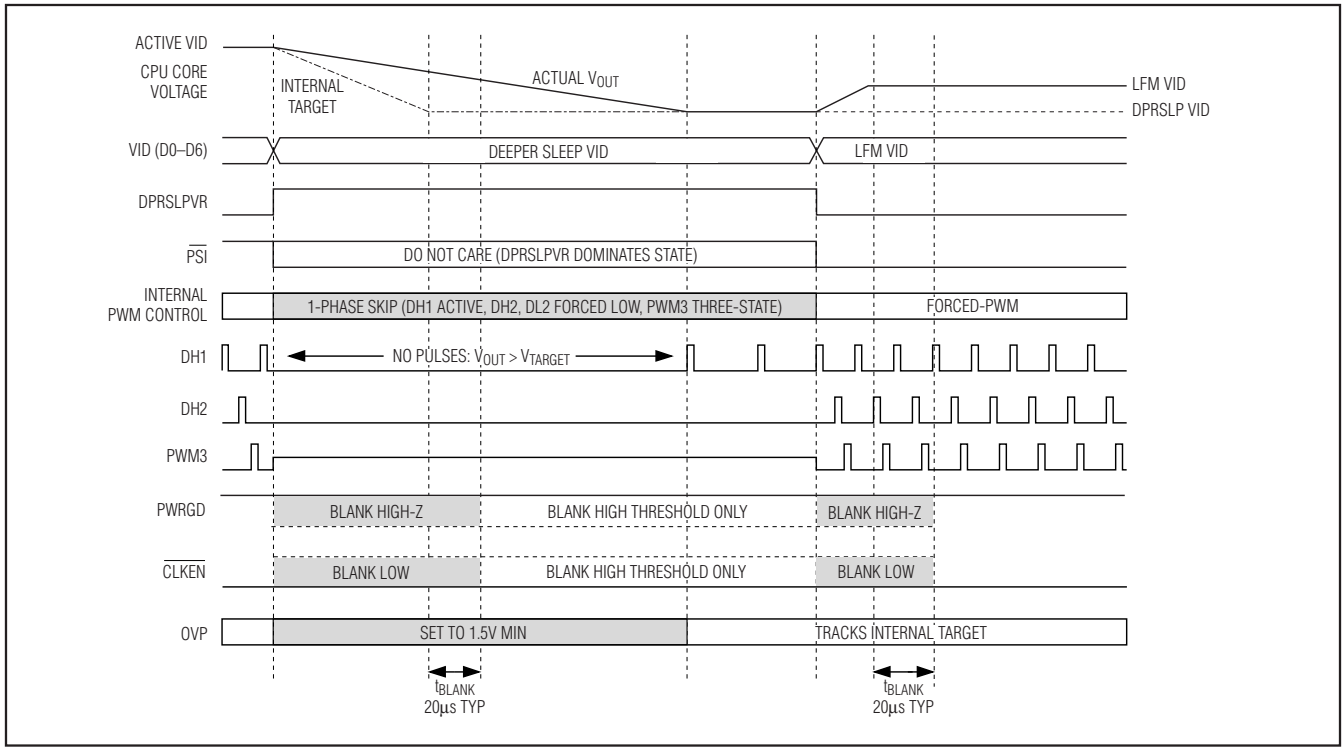


Figure 6. Standard C4 Transition

$\overline{PSI}$ Transitions

When $\overline{PSI}$ is pulled low, the MAX17030/MAX17036 immediately disable phase 3 (PWM3 three-state, $\overline{DRSKP}$ forced low) and enter 2-phase PWM operation (see Figure 7). When $\overline{PSI}$ is pulled high, the MAX17030/MAX17036 enable phase 3.

Forced-PWM Operation (Normal Mode)

During soft-shutdown and normal operation—when the CPU is actively running (DPRSLPVR = low, Table 5)—the MAX17030/MAX17036 operate with the low-noise, forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparators of all active phases, forcing the low-side gate-drive waveforms to constantly be the complement of the high-side gate-drive waveforms. This keeps the switching frequency constant and allows the inductor current to reverse under light loads, providing fast, accurate negative output-voltage transitions by quickly discharging the output capacitors.

Forced-PWM operation comes at a cost: the no-load +5V bias supply current remains between 10mA to 50mA per phase, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light-load conditions, the processor can switch the controller to a low-power pulse-skipping control scheme by entering suspend mode.

$\overline{PSI}$ determines how many phases are active when operating in forced-PWM mode (DPRSLPVR = low). When $\overline{PSI}$ is pulled low, phases 1 and 2 remain active but phase 3 is disabled (PWM3 three-state, $\overline{DRSKP}$ forced low).

Light-Load Pulse-Skipping Operation (Deeper Sleep)

During soft-start and normal operation when DPRSLPVR is pulled high, the MAX17030/MAX17036 operate with a single-phase pulse-skipping mode. The pulse-skipping mode enables the driver's zero-crossing comparator, so the controller pulls DL1 low when its current-sense inputs detect "zero" inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output.

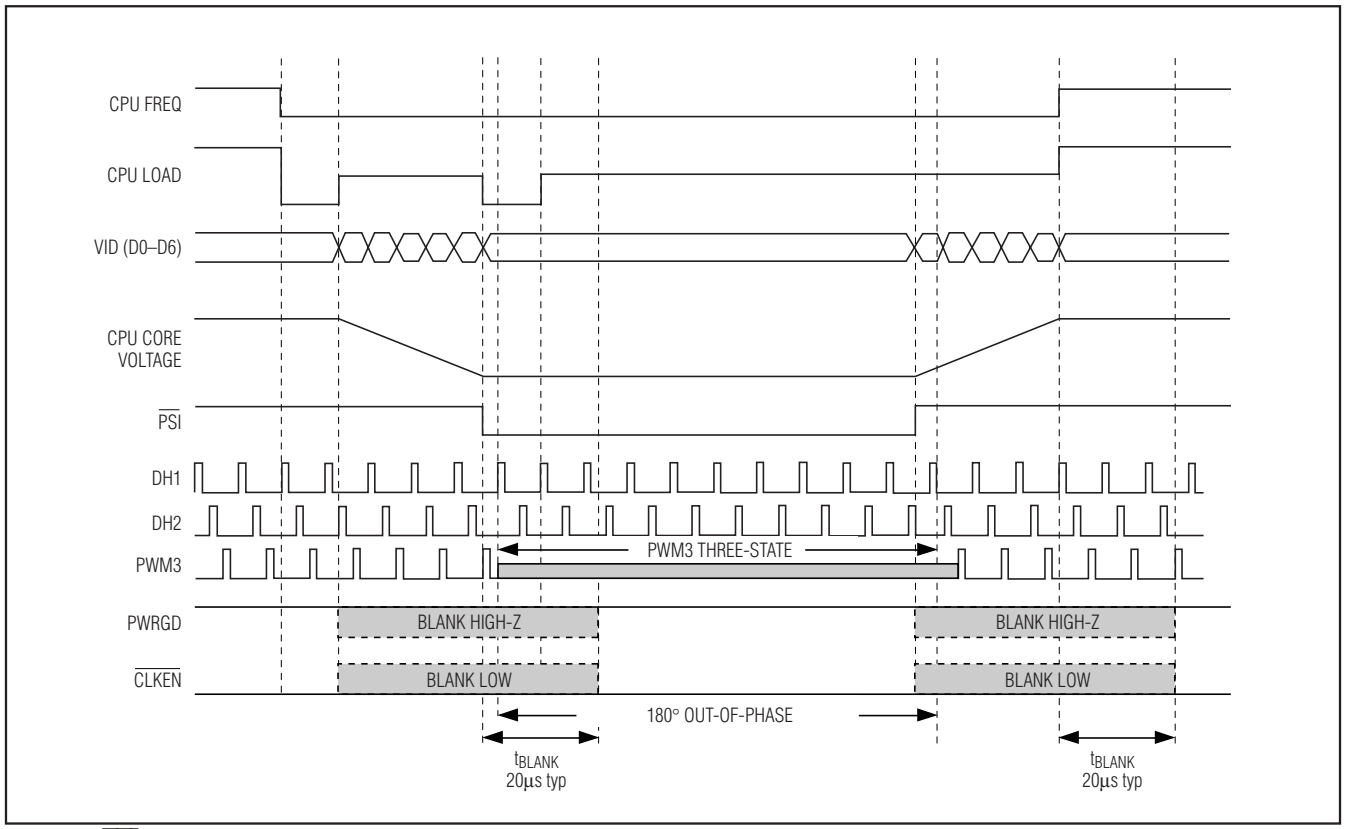


Figure 7. $\overline{PSI}$ Transition

When pulse-skipping, the controller blanks the upper PWRGD and CLKEN thresholds. Upon entering pulse-skipping operation, the controller temporarily sets the OVP threshold to 1.5V, preventing false OVP faults when the transition to pulse-skipping operation coincides with a VID code change. Once the error amplifier detects that the output voltage is in regulation, the OVP threshold tracks the selected VID DAC code. The MAX17030/MAX17036 automatically use forced-PWM operation during soft-start and soft shutdown, regardless of the DPRSLPVR and PSI configuration.

Automatic Pulse-Skipping Switchover

In skip mode (DPRSLPVR = high), an inherent automatic switchover to PFM takes place at light loads (Figure 8). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across the low-side MOSFETs. Once V_{LX} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics*), the comparator forces DL low. This mechanism causes the threshold between pulse-skipping PFM and non-skipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 8). For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The total load-current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \left(\frac{T_{SW} V_{OUT}}{L}\right)\left(\frac{V_{IN} - V_{OUT}}{2 \times V_{IN}}\right)$$

Power-Up Sequence (POR, UVLO)

The MAX17030/MAX17036 are enabled when SHDN is driven high (Figure 9). The reference powers up first. Once the reference exceeds its undervoltage-lockout (UVLO) threshold, the internal analog blocks are turned on and masked by a 150µs one-shot delay. The PWM controller then begins switching.

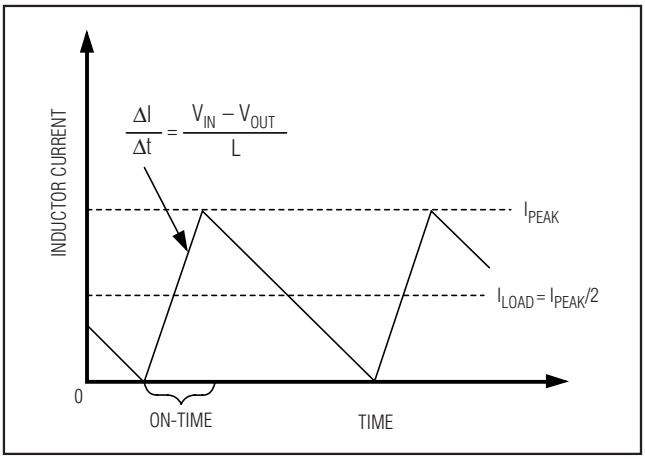


Figure 8. Pulse-Skipping/Discontinuous Crossover Point

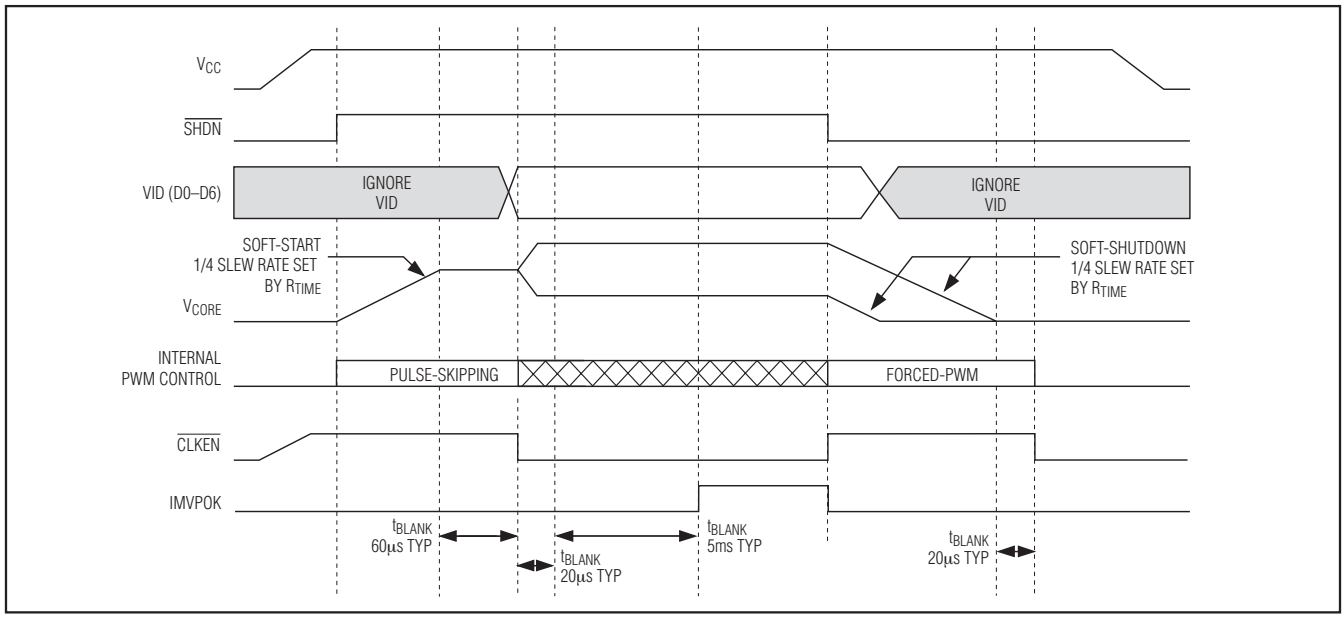


Figure 9. Power-Up and Shutdown Sequence Timing Diagram

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the controller for operation. The V_{CC} UVLO circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller, V_{CC} is above 4.25V, and $\overline{SHDN}$ driven high. With the reference in regulation, the controller ramps the output voltage to the boot voltage (1.1V) at 1/4 the slew rate set by R_{TIME}:

$$t_{TRAN(START)} = \frac{4V_{BOOT}}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt = 12.5mV/µs x 71.5kΩ/R_{TIME} is the slew rate. The soft-start circuitry does not use a variable current limit, so full output current is available immediately. $\overline{CLKEN}$ is pulled low approximately 60µs after the MAX17030/MAX17036 reach the boot voltage. At the same time, the MAX17030/MAX17036 slew the output to the voltage set at the VID inputs at the programmed slew rate. PWRGD becomes high impedance approximately 5ms after $\overline{CLKEN}$ is pulled low. The MAX17030/MAX17036 automatically operate in pulse-skipping mode during soft-start, and use forced-PWM operation during soft-shutdown, regardless of the DPRSLPVR and $\overline{PSI}$ configuration.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions, and shuts down immediately. DH and DL are forced low, and CSNI 10Ω discharge FET is enabled.

Shutdown

When $\overline{SHDN}$ goes low, the MAX17030/MAX17036 enters low-power shutdown mode. PWRGD is pulled low immediately, and the output voltage ramps down at 1/4 the slew rate set by R_{TIME}:

$$t_{TRAN(SHDN)} = \frac{4V_{OUT}}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt = 12.5mV/µs x 71.5kΩ/R_{TIME} is the slew rate. After the output voltage drops to 12.5mV, the MAX17030/MAX17036 shut down completely—the drivers are disabled (DL1 and DL2 driven low, PWM3 is three-state, and $\overline{DRSKP}$ low), the reference turns off, 10Ω CSNI discharge FET is turned on, and the supply current drops below 1µA.

When an undervoltage fault condition activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle V_{CC} power below 0.5V.

Current Monitor (IMON)

The MAX17030/MAX17036 include a unidirectional transconductance amplifier that sources current proportional to the positive current-sense voltage. The IMON output current is defined by:

$$I_{IMON} = G_{m(IMON)} \times \Sigma(V_{CSP} - V_{CSN})$$

where $G_{m(IMON)}$ = 1.6mS (typ) and the IMON current is unidirectional (sources current out of IMON only) for positive current-sense values. For negative current-sense voltages, the IMON current is zero.

Connect an external resistor between IMON and GNDS to create the desired IMON gain based on the following equation:

$$R_{IMON} = 0.9V/(I_{MAX} \times R_{SENSE(MIN)} \times G_{m(IMON\_MIN)})$$

where I_{MAX} is defined in the Current Monitor section of the Intel IMVP-6.5 specification and based on discrete increments (10A, 20A, 30A, 40A, etc.), $R_{SENSE(MIN)}$ is the **minimum** effective value of the current-sense element (sense resistor or inductor DCR) that is used to provide the current-sense voltage, and $G_{m(IMON\_MIN)}$ is the **minimum** transconductance amplifier gain as defined in the *Electrical Characteristics*.

The IMON voltage is internally clamped to a maximum of 1.1V (typ), preventing the IMON output from exceeding the IMON voltage rating even under overload or short-circuit conditions. When the controller is disabled, IMON is pulled to ground.

The transconductance amplifier and voltage clamp are internally compensated, so IMON cannot directly drive large capacitance values. To filter the IMON signal, use an RC filter as shown in Figure 1.

Temperature Comparator ($\overline{VRHOT}$)

The MAX17030/MAX17036 also feature an independent comparator with an accurate threshold (V_{HOT}) that tracks the analog supply voltage (V_{HOT} = 0.3V_{CC}). This makes the thermal trip threshold independent of the V_{CC} supply voltage tolerance. Use a resistor- and thermistor-divider between V_{CC} and GND to generate a voltage-regulator overtemperature monitor. Place the thermistor as close to the MOSFETs and inductors as possible.

Fault Protection (Latched)

Output Overvoltage Protection

The overvoltage-protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX17030/MAX17036 continuously monitor the output for an overvoltage fault. An OVP fault is detected if the output voltage exceeds the set VID DAC voltage by more than 300mV, or the fixed 1.5V (typ) threshold

during a downward VID transition in skip mode. During pulse-skipping operation (DPRSLPVR = high), the OVP threshold tracks the VID DAC voltage as soon as the output is in regulation; otherwise, the fixed 1.5V (typ) threshold is used.

When the OVP circuit detects an overvoltage fault while in multiphase mode (DPRSLPVR = low, $\overline{PSI}$ = high), the MAX17030/MAX17036 immediately force DL1 and DL2 high, PWM3 low, and $\overline{DRSKP}$ high; and pull DH1 and DH2 low. This action turns on the synchronous-rectifier MOSFETs with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output low. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

When an overvoltage fault occurs while in 1-phase operation (DPRSLPVR = high, or $\overline{PSI}$ = low), the MAX17030/MAX17036 immediately force DL1 high and pull DH1 low. DL2 and DH2 remain low as phase 2 was disabled. DL2 does not react.

Overvoltage protection can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Output Undervoltage Protection

If the MAX17030/MAX17036 output voltage is 400mV below the target voltage, the controller activates the shutdown sequence and sets the fault latch. Once the output voltage ramps down to 12.5mV, it forces the DL1 and DL2 low and pulls DH1 and DH2 low, three-states PWM3, and sets $\overline{DRSKP}$ low 10Ω CSNI discharge FET is turned on. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

UVP can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Thermal-Fault Protection

The MAX17030/MAX17036 feature a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latch and forces the DL1 and DL2 low and pulls DH1 and DH2 low, three-states PWM3, sets $\overline{DRSKP}$ low, and enables 10Ω CSNI discharge FET on. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

Thermal shutdown can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

No-Fault Test Mode

The latched fault-protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a "no-fault" test mode is provided to disable the fault protection—overvoltage protection, undervoltage protection, and thermal shutdown. Additionally, the test mode clears the fault latch if it has been set. The no-fault test mode is entered by forcing 11V to 13V on $\overline{SHDN}$.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH) source 2.7A and sink 2.2A, and the low-side gate drivers (DL) source 2.7A and sink 8A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET drivers are powered by internal boost switch charge pumps at BST_, while the DL_ synchronous-rectifier drivers are powered directly by the 5V bias supply (V_{DD}).

Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

A low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates is required for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17030/MAX17036 interprets the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The DL low on-resistance of 0.25Ω (typ) helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to V_{IN}. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold to prevent shoot-through currents:

$$V_{GS(TH)} > V_{IN(MAX)}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Adding a 4700pF between DL and power ground (C_{NL} in Figure 10), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

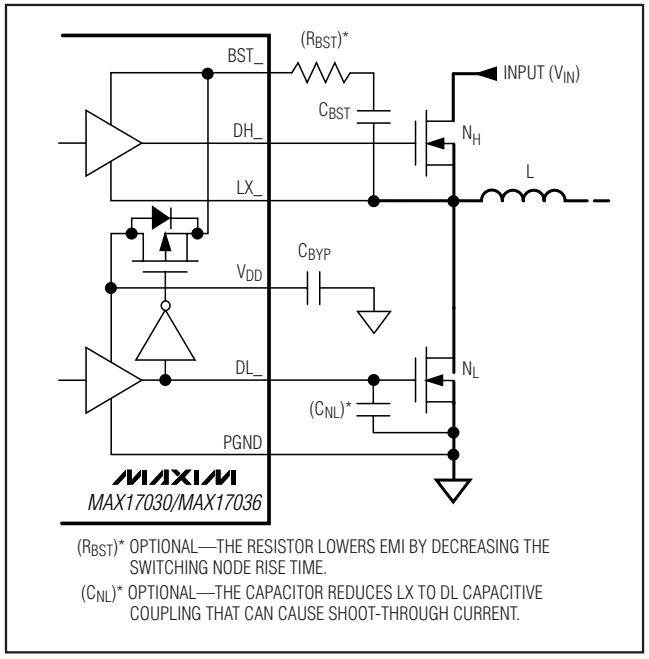


Figure 10. Gate Drive Circuit

Shoot-through currents can also be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 10). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

Multiphase Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

  For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{\eta_{TOTAL}}$$

  where η_{TOTAL} is the total number of active phases.
- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 30% and 50% ripple current. for a multiphase core regulator, select an LIR value of ~0.4.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \eta_{TOTAL}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where η_{TOTAL} is the total number of phases.

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Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{\eta_{TOTAL}}\right)\left(1+\frac{LIR}{2}\right)$$

Output Capacitor Selection

Output capacitor selection is determined by the controller stability requirements, and the transient soar and sag requirements of the application.

Output Capacitor ESR

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For multiphase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN} f_{SW} L}{(V_{IN} - \eta_{TOTAL} V_{OUT}) V_{OUT}}\right] V_{RIPPLE}$$

where η_{TOTAL} is the total number of active phases and f_{SW} is the switching frequency per phase. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{EFF} C_{OUT}}$$

and:

$$R_{EFF} = R_{ESR} + R_{DROOP} + R_{PCB}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent series resistance, R_{DROOP} is the voltage-positioning gain, and R_{PCB} is the parasitic board resistance between the output capacitors and sense resistors.

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, SANYO POSCAP, and Panasonic SP capacitors in widespread use at the time of publication have typical ESR zero frequencies below 50kHz. In the standard application circuit, the ESR needed to support a $30mV_{P-P}$ ripple is 30mV/(40A x 0.3) = 2.5mΩ. Four 330µF/2.5V Panasonic SP (type SX) capacitors in parallel provide 1.5mΩ (max) ESR. With a 2mΩ droop and 0.5mΩ PCB resistance, the typical combined ESR results in a zero at 30kHz.

Ceramic capacitors have a high ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. When using only ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value favors high switching-frequency operation with small inductor values to minimize the energy transferred from inductor to capacitor during load-step recovery.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output-voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple.

However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast 10% to 90% max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. For a dual-phase controller, the worst-case output sag voltage can be determined by:

$$V_{SAG} \approx \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2}{2\eta_{TOTAL} C_{OUT} V_{OUT}} \times \frac{T_{MIN}}{\left[KT_{SW} - T_{MIN}\right]}$$

and:

$$T_{MIN} = t_{ON} + t_{OFF(MIN)}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics*), T_{SW} is the programmed switching period, and η_{TOTAL} is the total number of active phases. K = 66% when N_{PH} = 3, and K = 100% when N_{PH} = 2. V_{SAG} must be less than the transient droop $\Delta I_{LOAD(MAX)} \times R_{DROOP}$.

The capacitive soar voltage due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2\eta_{TOTAL} C_{OUT} V_{OUT}}$$

where η_{TOTAL} is the total number of active phases. The actual peak of the soar voltage is dependent on the time where the decaying ESR step and rising capacitive soar is at its maximum. This is best simulated or measured. For the MAX17036 with transient suppression, contact Maxim directly for application support to determine the output capacitance requirement.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The multiphase Quick-PWM controllers operate out-of-phase, reducing the RMS input. For duty cycles less than $100\%/\eta_{OUTPH}$ per phase, the I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{\eta_{TOTAL} V_{IN}}\right)\sqrt{\eta_{TOTAL} V_{OUT}\left(V_{IN} - \eta_{TOTAL} V_{OUT}\right)}$$

where η_{TOTAL} is the total number of out-of-phase switching regulators. The worst-case RMS current requirement occurs when operating with $V_{IN} = 2\eta_{TOTAL}V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}/\eta_{TOTAL}$. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters.

High-Side MOSFET Power Dissipation

The conduction loss in the high-side MOSFET (N_H) is a function of the duty factor, with the worst-case power dissipation occurring at the minimum input voltage:

$$PD\ (NH\ Resistive) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

where η_{TOTAL} is the total number of phases.

Calculating the switching losses in the high-side MOSFET (N_H) is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (NH\ Switching) = \left(\frac{V_{IN} I_{LOAD} f_{SW}}{\eta_{TOTAL}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS} V_{IN}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (2.2A typ).

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The optimum high-side MOSFET trades the switching losses with the conduction ($R_{DS(ON)}$) losses over the input voltage range. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Low-Side MOSFET Power Dissipation

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (NL\ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit can be overdesigned to tolerate:

$$I_{LOAD} = \eta_{TOTAL}\left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}\right)$$

$$= \eta_{TOTAL} I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good-size heatsink to handle the overload power dissipation.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two thermally enhanced 8-pin SOs), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems might occur (see the *MOSFET Gate Drivers* section).

The optional Schottky diode (D_L) should have a low forward voltage and be able to handle the load current per phase during the dead times.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (1) FDS6298 n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single FDS6298 has a maximum gate charge of 19nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{1 \times 10nC}{200mV} = 0.05\mu F$$

Selecting the closest standard value; this example requires a 0.1µF ceramic capacitor.

Current Limit and Slew-Rate Control (TIME and ILIM)

TIME and ILIM are used to control the slew rate and current limit. TIME regulates to a fixed 2.0V. The MAX17030/MAX17036 use the TIME source current to set the slew rate (dV_{TARGET}/dt). The higher the source current, the faster the output-voltage slew rate:

$$dV_{TARGET}/dt = 12.5mV/\mu s \times \left(\frac{71.5k\Omega}{R_{TIME}}\right)$$

where R_{TIME} is the sum of resistance values between TIME and ground.

The ILIM voltage determines the valley current-sense threshold. When ILIM = V_{CC}, the controller uses the 22.5mV preset current-limit threshold. In an adjustable design, ILIM is connected to a resistive voltage-divider connected between TIME and ground. The differential voltage between TIME and ILIM sets the current-limit threshold (V_{LIMIT}), so the valley current-sense threshold:

$$V_{LIMIT} = \frac{V_{TIME} - V_{ILIM}}{10}$$

This allows design flexibility since the DCR sense circuit or sense resistor does not have to be adjusted to meet the current limit as long as the current-sense voltage never exceeds 50mV. Keeping V_{LIMIT} between 20mV to 40mV leaves room for future current-limit adjustment.

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{VALLEY} > I_{LOAD(MAX)}\left(1 - \frac{LIR}{2}\right)$$

where:

$$I_{VALLEY} = \frac{V_{LIMIT}}{R_{SENSE}}$$

where R_{SENSE} is the sensing resistor or effective inductor DCR.

Voltage Positioning and Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the output capacitance and processor's power-dissipation requirements. The MAX17030/MAX17036 use a transconductance amplifier to set the transient and DC output voltage droop (Figure 3) as a function of the load. This adjustability allows flexibility in the selected current-sense resistor value or inductor DCR, and allows smaller current-sense resistance to be used, reducing the overall power dissipated.

Steady-State Voltage Positioning

Connect a resistor (R_{FB}) between FB and V_{OUT} to set the DC steady-state droop (load line) based on the required voltage-positioning slope (R_{DROOP}):

$$R_{FB} = \frac{R_{DROOP}}{R_{SENSE}G_{m(FB)}}$$

where the effective current-sense resistance (R_{SENSE}) depends on the current-sense method (see the *Current Sense* section), and the voltage positioning amplifier's transconductance ($G_{m(FB)}$) is typically 400µS as defined in the *Electrical Characteristics* table. The controller sums together the input signals of the current-sense inputs (CSP_, CSN_).

When the inductors' DCR is used as the current-sense element ($R_{SENSE} = R_{DCR}$), each current-sense input should include an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Refer to the MAX17030 Evaluation Kit specification for a layout example and follow these guidelines for good PCB layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) Connect all analog grounds to a separate solid copper plane, which connects to the ground pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, FB, and GNDS bypass capacitors.
3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCB (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
4) Keep the high current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
5) CSP_ and CSN_ connections for current limiting and voltage positioning must be made using Kelvin sense connections to guarantee the current-sense accuracy.
6) When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
7) Route high-speed switching nodes away from sensitive analog areas (FB, CSP_, CSN_, etc.).

Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50mils to 100mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST diodes and capacitors, V_{DD} bypass capacitor) together near the controller IC.

4) Make the DC-DC controller ground connections as shown in the standard application circuits. This diagram can be viewed as having four separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the GND pin and V_{DD} bypass capacitor go; the master's analog ground plane, where sensitive analog components, the master's GND pin and V_{CC} bypass capacitor go; and the slave's analog ground plane, where the slave's GND pin and V_{CC} bypass capacitor go. The master's GND plane must meet the GND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the GND plane only at a single point directly beneath the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from GND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.

5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 TQFN-EP	T4055-2	**21-0140**