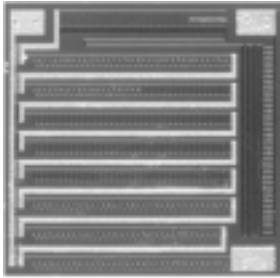


Thin Film Voltage Divider Resistors



Product may not be to scale

FEATURES

- Variable ratios
- Chip size: 0.058 inch square
- Resistor material: tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Moisture resistant

The ATA voltage divider is a versatile two-resistor tapped chip whose R_A/R_B ratio can be specified within the values of 1:1 to 20:1. These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The ATAs are 100% electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

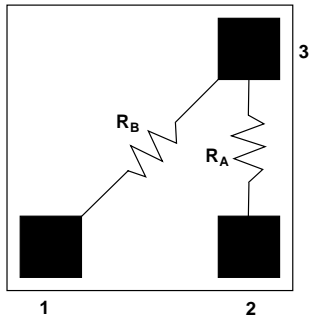
Vishay EFI ATA voltage divider resistor-ratio chips are designed for the tight ratio tolerances generally required in amplifier feedback circuits. The great range of ratio choices makes them specially suitable for this application.

TEMPERATURE COEFFICIENT OF RESISTANCE VALUES AND TOLERANCES	
Resistance ($R_A + R_B$)	25k Ω
Tolerances ($R_A + R_B$)	$\pm 5\%$
Greatest ratio (R_A/R_B)	20:1
TCR	$\pm 50\text{ppm}/^\circ\text{C}$

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR tracking between R_A and R_B	$\pm 5\text{ppm}/^\circ\text{C}$
Noise, MIL-STD-202, Method 308	- 35dB typical
Moisture resistance, MIL-STD-202, Method 106	$\pm 0.5\%$ maximum $\Delta R/R$
Stability, 1000 hours, + 125°C, 25mW	$\pm 0.25\%$ maximum $\Delta R/R$
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	$\pm 0.1\%$ maximum $\Delta R/R$
High temperature exposure + 150°C, 100 hours	$\pm 0.2\%$ maximum $\Delta R/R$
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C (derated to zero at 175°C)	50mW per resistor
5 x rated power short-time overload, + 25°C, 5 seconds	$\pm 0.1\%$ maximum $\Delta R/R$

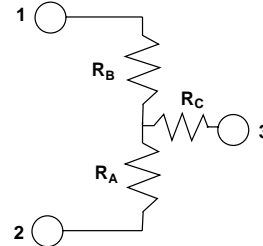
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CONFIGURATIONS



Shaded areas represent bonding pads.

$$\text{ATTENUATOR FACTOR} = \frac{R_A}{R_A + R_B}$$



Any ratio R_A/R_B from 1 to 20 is available to $\pm 0.05\%$

R_C is a parasitic resistor approximately 5Ω in value, which does not effect the performance of the device when it is used into a high impedance load.

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.058 x 0.058 \pm 0.003 (1.47 x 1.47 \pm 0.076mm)
Chip thickness	0.010 \pm 0.002 (0.254 \pm 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO ₂
Resistor material	Tantalum nitride, self-passivating
Bonding pads	0.005 x 0.005 (0.127 x 0.127mm)
Number of top pads	3
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTION: Gold back for eutectic die attach
Contact Applications Engineer

ATTENUATION TABLE

PART # ATA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	RATIO ACCURACY	TEMPERATURE TRACKING
RATIO R_A/R_B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	$\pm 0.05\%$	$\pm 5\text{ppm}/^\circ\text{C}$ maximum $\pm 2\text{ppm}/^\circ\text{C}$ typical
ATTENUATOR FACTOR $R_B/R_A + R_B$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	$\pm 0.025\%$ to $\pm 0.048\%$	$\pm 2.5\text{ppm}/^\circ\text{C}$ to $\pm 4.8\text{ppm}/^\circ\text{C}$ maximum $\pm 1\text{ppm}/^\circ\text{C}$ to $\pm 2\text{ppm}/^\circ\text{C}$ typical
ATTENUATOR FACTOR $R_A/R_A + R_B$	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	$\pm 0.025\%$ to $\pm 0.0025\%$	$\pm 2.5\text{ppm}/^\circ\text{C}$ to $\pm 0.25\text{ppm}/^\circ\text{C}$ maximum $\pm 1\text{ppm}/^\circ\text{C}$ to $\pm 0.15\text{ppm}/^\circ\text{C}$ typical

*Depends on ratio

ORDERING INFORMATION

Example: 100% visualled, 25kΩ, $\pm 5\%$, $\pm 100\text{ppm}/^\circ\text{C}$ TCR, Ratio = 19.0, Aluminum Pads, Class H

P/N:	W	ATA	003	1900	B	J
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RATIO VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 X = Sample, visually inspected loaded in matrix trays (4% AQL)		003 = Class H 005 = Class K	Use first 4 significant digits of the ratio RA/RB - Any ratio between 1 to 20	C = 0.001 B = 0.01	J = 5.0%

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